Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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Contact us

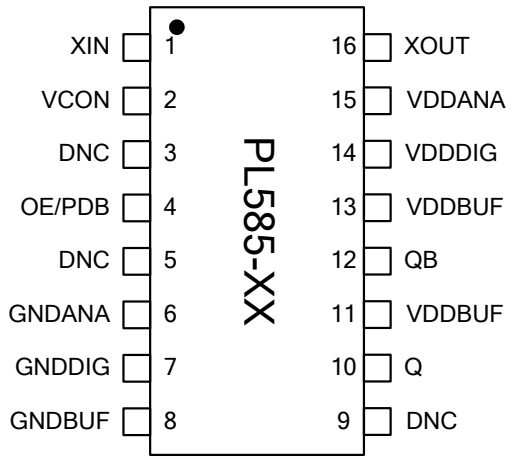
Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

19MHz to 800MHz Low Phase-Noise VCXO

FEATURES

- < 0.5ps RMS phase jitter (12kHz to 20MHz) at 622.08MHz (LVPECL/LVDS)
- 30ps max peak to peak period jitter
- Ultra Low-Power Consumption
  - < 90mA @622MHz PECL output
  - <10µA at Power Down (PDB) Mode
- Input Frequency:
  - Fundamental Crystal: 19MHz to 44MHz
- Output Frequency:
  - 19MHz to 800MHz output.
- Output types: LVPECL, LVDS, or LVCMOS.
- High Linearity VCXO: <10% linearity
- Pullability: ±150 ppm
- Programmable OE input polarity,
  - Programmable Hi-Z or Active Low disabled state (CMOS output only)
- Power Supply: 3.3V, ±10%
- Operating Temperature Ranges:
  - Commercial: 0°C to 70°C
  - Industrial: -40°C to 85°C
- Available in TSSOP package

PIN CONFIGURATION



TSSOP-16L

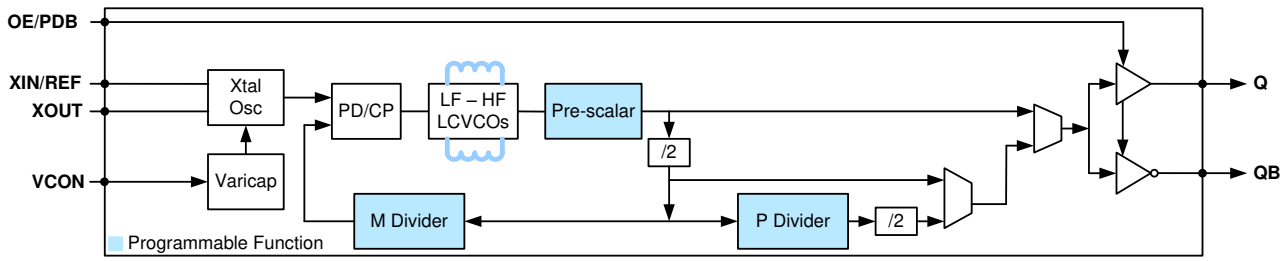
DESCRIPTION

The PL585 is a Dual LC core monolithic IC VCXO, capable of maintaining sub-picoseconds RMS phase jitter, while covering a wide frequency output range up to 800MHz, without the use of external components. The high performance and high frequency output is achieved using a low cost fundamental crystal of between 19MHz and 44 MHz. The PL585 is designed to address the demanding requirements of high performance applications such Fiber Channel, serial ATA, Ethernet, SAN, SONET/SDH, etc.

OUTPUT ENABLE CONTROL

OE Options (Programmable)	OE	State
Conventional Polarity	0 (Default)	Output enabled
	1	Tri-state
Reverse Polarity	0	Tri-state
	1 (Default)	Output enabled

BLOCK DIAGRAM



PIN ASSIGNMENT

Name	Pin #	Type	Description
XIN	1	I	Crystal input connection.
VCON	2	I	Analog voltage control pin.
DNC	3, 5, 9	-	Do Not Connect.
OE/PDB	4	I	This pin may be programmed as output enable (OE), or power-down (PDB) pin. This pin incorporates an Internal pull-up resistor of 60KΩ for OE, and PDB, operations.
GND_ANA	6	P	GND connection for analog circuitry.
GND_DIG	7	P	GND connection for digital circuitry.
GND_BUF	8	P	GND connection for buffer circuitry.
Q	10	O	True Output buffer.
QB	12	O	Complementary Output buffer.
VDD_BUF	11, 13	P	VDD connection for buffer circuitry.
VDD_DIG	14	P	VDD connection for digital circuitry.
VDD_ANA	15	P	VDD connection for analog circuitry.
XOUT	16	P	Output connection to crystal.

OPTION SELECTION TABLE

PL585 is a fully programmable VCXO IC. However, for ordering convenience, the following part numbers have been created for when simple multiplication is used, for your convenience. When other features of the IC are exercised (i.e. reverse polarity on OE, power down, etc.), another 3-digit code is used to identify the functionality.

Input Crystal Frequency Range (MHz)	Multiplication Factor	Output Frequency Range (MHz)		Part #
		Low Limit	High Limit	
33.750000 ~ 40.000000	X20	675.00	800.00	PL585-P8-020
33.333333 ~ 42.187500	X16	533.33	675.00	PL585-P8-168
32.142857 ~ 38.095238	X14	450.00	533.33	PL585-P8-148
33.333333 ~ 37.500000	X12	400.00	450.00	PL585-P8-128
33.750000 ~ 40.000000	X10	337.50	400.00	PL585-P8-108
33.333333 ~ 42.187500	X8	266.67	337.50	PL585-P8-088
32.142857 ~ 38.095238	X7	225.00	266.67	PL585-P8-078
33.333333 ~ 37.500000	X6	200.00	225.00	PL585-P8-068
33.750000 ~ 40.000000	X5	168.75	200.00	PL585-P8-058
33.333333 ~ 42.187500	X4	133.33	168.75	PL585-P8-048
32.142857 ~ 38.095238	X3.5	112.50	133.33	PL585-P8-358
33.333333 ~ 37.500000	X3	100.00	112.50	PL585-P8-038
33.750000 ~ 40.000000	X2.5	84.375	100.00	PL585-P8-258
32.812500 ~ 42.187500	X2	65.625	84.375	PL585-P8-028

Common functionality for packaged parts in the above table: OE function active high polarity. Please inform your Sales representative for active low OE functionality.

FUNCTIONAL DESCRIPTION

PL585 family of products is an advanced, programmable LCVCO VCXO IC that is designed to meet the most stringent performance specifications for phase noise, jitter, and power consumption.

There are two main types of VCOs, a) Ring Oscillator, b) LC Tank oscillator. An LCVCO is made up of LC tank oscillator. Although a Ring Oscillator has very good performance, and has a good tuning range, its phase noise and jitter performance, in particular at higher frequencies, degrades.

On the other hand, an LCVCO has an outstanding phase noise and jitter performance, even at higher frequencies. PL585 family of products takes advantage of this state of the art technology, and incorporates the LC tank on-chip, for optimal performance.

PL585 family of products exhibit very low phase noise/phase jitter and peak to peak jitter, wide tuning range, and very low-power. All members of the PL585 family accept a low-cost fundamental crystal input of 19MHz to 44MHz, and its flexible core is capable of producing any output frequency between 19MHz to 800MHz.

PLL Programming

The PLL in the PL585 family is fully programmable. Micrel programming software is used to configure and program the IC.

OE (Output Enable)

The OE pin in PL585 family, through programming, can be configured to support OE pin activation with a logic '1' or logic '0', to provide you with the desired enable polarity.

OE Options (Programmable)	OE	State
Conventional Polarity	0 (Default)	Output enabled
	1	Tri-state
Reverse Polarity	0	Tri-state
	1 (Default)	Output enabled

In addition, The OE feature can be programmed to allow the output to float (Hi Z), or to operate in the 'Active low' mode, for CMOS outputs. The programming control for the OE options is shown below:

OE Pin	Osc	PLL	Output
0	On	On	Hi Z
	On	On	Active '0' (CMOS Only)
1	Normal Operation (Default)		

Note: Typical enable time is <50ns plus one clock period.

The OE pin incorporates a 60KΩ resistor to either pull-up or pull-down to the default state when the OE pin is left open.

Power-Down Control (PDB)

When activated, this programmable feature 'Disables the VCO, the oscillator circuitry, counters, and all other active circuitry. PDB activation disables all outputs and the IC consumes <15µA of power, in the power down mode, to conserve power. The PDB input incorporates a 10MΩ pull up resistor for normal operating condition.

The PDB feature can be programmed to allow the output to float (Hi Z), or to operate in the 'Active low' mode, in CMOS output. The logic for PDB is shown below:

PDB Pin	Osc.	PLL	Output
0	Off	Off	Hi Z
	Off	Off	Active '0' (CMOS Only)
1	Normal Operation (Default)		

Note: Typical enable time is <10ms.

ELECTRICAL SPECIFICATIONS

1. ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature (industrial temperature)*	T_{AI}	-40	85	°C
Ambient Operating Temperature (commercial temperature)	T_{AC}	0	70	°C
Junction Temperature	T_J		125	°C
ESD Protection, Human Body Model		2		kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permane nt damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

2. GENERAL ELECTRICAL SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, Dynamic	I_{DDQ}	LVPECL, 622.08MHz, 3.3V			90	mA
Supply Current, PDB Enabled		PDB = 0, 3.3V			10	uA
Output Enable Time	t_{OE}	OE logic 0 to logic 1, Ta=25° C. Add one clock period to this measurement for a usable clock output.			50	ns
Power Up Time	T_{PU}	PDB logic 0 to logic 1, Ta=25° C.			10	ms
Operating Voltage	V_{DD}		2.97	3.3	3.63	V
Power Up Ramp Rate	t_{PU}	Time for V_{DD} to reach 90% V_{DD}. Power ramp must be monotonic.	0.1		100	ms
Auto-Calibration Time	t_{AC}	At power up			10	ms
Output Clock Duty Cycle		@ 50% of output waveform	45	50	55	%

3. VOLTAGE CONTROLLED CRYSTAL OSCILLATOR

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VCXO Pullability		VCON=1.65V, ±1.65V XTAL C_1>10fF and C_0/C_1<250		±150		ppm
VCXO Tuning Characteristic				100		ppm/V
Pull Range Linearity					10	%
VCON Pin Input Impedance			10			MΩ
VCON Modulation BW		0V ≤ VCON ≤ 3.3V, -3dB	18			kHz

4. CRYSTAL SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Crystal Resonator Frequency	F_{XIN}	Parallel Fundamental Mode	19		44	MHz
Crystal Cload	$C_{L\_Crystal}$	V_{DD} = 3.3V, VCON = 1.65V		8.5		
Shunt Capacitance	$C_{0\_Crystal}$				3.5	pF
Crystal Pullability	C_0/C_1	AT cut	250			--
Recommended ESR	R_E	AT cut , up to 40MHz			45	Ω
		AT cut , up to 44MHz			40	Ω

5. JITTER SPECIFICATIONS

PARAMETERS	FREQUENCY	CONDITIONS	MIN	TYP	MAX	UNITS
RMS Phase Jitter	622.08MHz	12kHz to 20MHz, XIN=38.88MHz		0.5		ps
Period Jitter, Pk-to-Pk	622.08MHz	10K cycles, LVPECL (-88) XIN=38.88MHz		25		ps
	212.5MHz	10K cycles, LVCMOS (-27), XIN=26.5625MHz		35		

6. PHASE NOISE SPECIFICATIONS

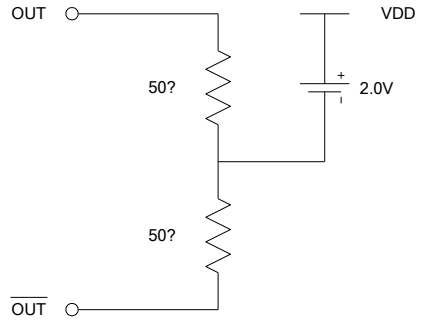
PARAMETERS	Freq. (MHz)	@ 10Hz	@ 100Hz	@ 1KHz	@ 10KHz	@ 100KHz	@ 1MHz	@ 10MHz	UNITS
Phase Noise, relative to carrier (typical)	155.52	-56	-86	-112	-123	-127	136	147	dBc/Hz
	622.08	-47	-77	-101	-111	-114	-127	-145	

Note: Phase Noise measured at VCON = 1.65V

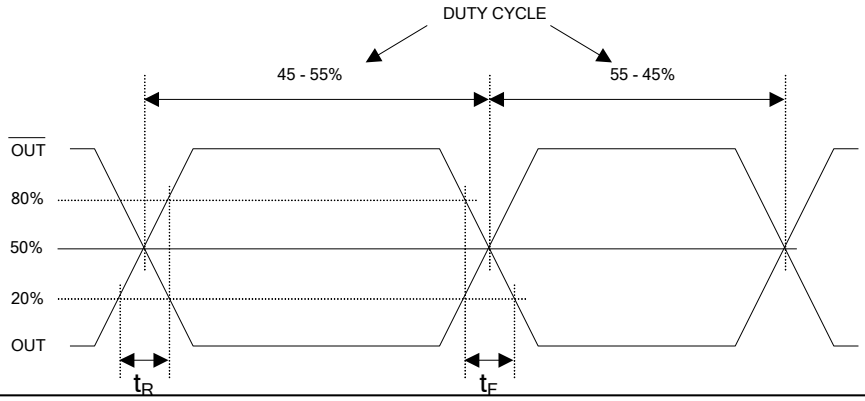
7. LVPECL OUTPUTS (Q, QB)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH}	Q, QB Standard LVPECL Termination, V_{DD} = 3.3V	2.275	2.350	2.420	V
Output Low Voltage	V_{OL}		1.490	1.600	1.680	V
Output Frequency	F_{out}	3.3V	19		800	MHz
Output Rise, Fall Times	t_r, t_f	20% - 80% of output waveform		300	500	ps
Output Voltage Swing	V_{pp}	Q, QB	550	800	930	mV

LVPECL Levels Test Circuit



LVPECL Transistion Time Waveform



LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

- Keep traces short!

- Trace = Inductor. With a capacitive load this equals ringing!

- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).

- Design long traces (<1 inch) as “striplines” or “microstrips” with defined impedance.

- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the V_{DD} pin(s) to limit noise from the power supply

- Multiple V_{DD} pins should be decoupled separately for best performance.

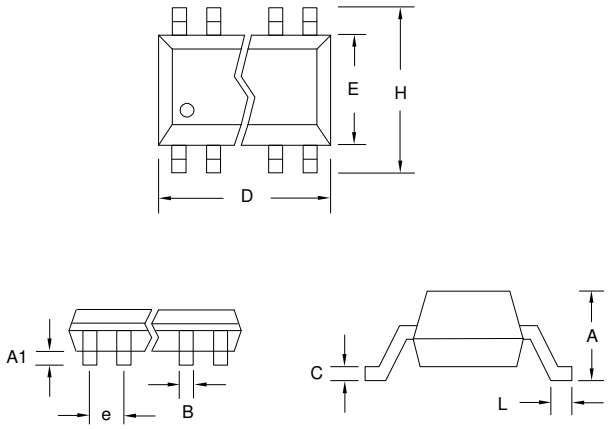
- Addition of a ferrite bead in series with V_{DD} can help prevent noise from other board sources

- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1μF for designs using frequencies < 50MHz and 0.01μF for designs using frequencies > 50MHz.

PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

TSSOP-16L

Symbol	Dimension in MM	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
b	0.19	0.30
C	0.09	0.20
D	4.90	5.10
E	4.30	4.50
H	6.20	6.60
L	0.45	0.75
e	0.65 BSC	



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER
The order number for this device is a combination of the following:
Part number, Package type, Thickness and Operating temperature range

PL585-XX-XXX XX

Part Number Programming Code

Packaging Option

Temperature Range
C = Commercial (0°C to 70°C)
I = Industrial (-45°C to +85°C)

Part Number/Order Number	Marking†	Package Option
PL585-XX-XXXOC	P585-XX XXX(I) LLLLL	16-Pin TSSOP (Tube)
PL585-XX-XXOC-R		16-Pin TSSOP (Tape and Reel)

† **Marking Notes:**
1) The "I" after the 3 digit programming code will be marked for Industrial Temperature grade products only. Commercial grade products will not have a character in this position.