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**Low Phase Noise, LVPECL VCXO (for 75MHz to 125MHz Fundamental Crystals)**

**FEATURES**

- Advanced non multiplier VCXO Design for High Performance Crystal Oscillators
- Input/Output Range: 75MHz to 125MHz
- Very Low Phase Noise: <-150dBc at 100KHz
- Very low Phase Jitter: 120fs RMS at 125MHz
- High Pull Range: ±125ppm
- Linearity: <5%
- Integrated Variable Capacitors
- Complementary LVPECL Outputs
- Power Supply: 3.3V ±10%
- Available in Die or Wafer Form

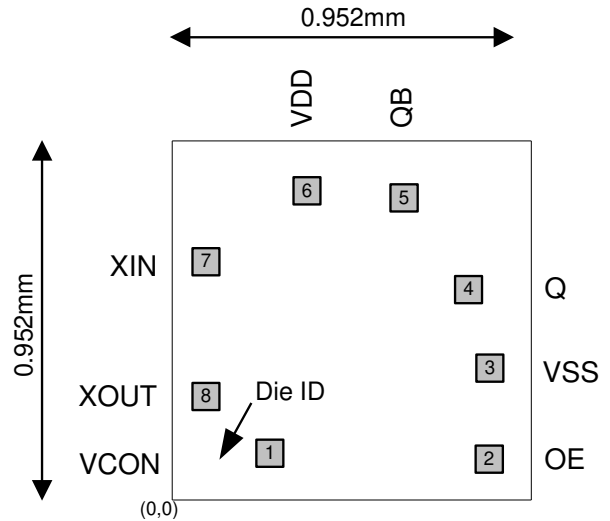
**DESCRIPTION**

The PL586-15/-18 is a non-multiplier VCXO IC specifically designed to pull fundamental mode crystals from 75MHz to 125MHz. This IC achieves a typical pull range of ±125ppm with 5% linearity. The phase noise performance, with <120fs phase jitter, makes this an ideal solution for all high end clocking applications such as SONET, WiMax, CPRI, OBSAI, Fiber Channel, and any application where performance and quality are required.

**DIE SPECIFICATIONS**

Name	Value
Size	952 micron x 952 micron
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	8 mil

**DIE CONFIGURATION**



**OUTPUT ENABLE LOGIC PL586-15**

OE State (Pad 4)	Output Buffers State
0	Outputs Tri-Stated
1 (Default)	Outputs Enabled

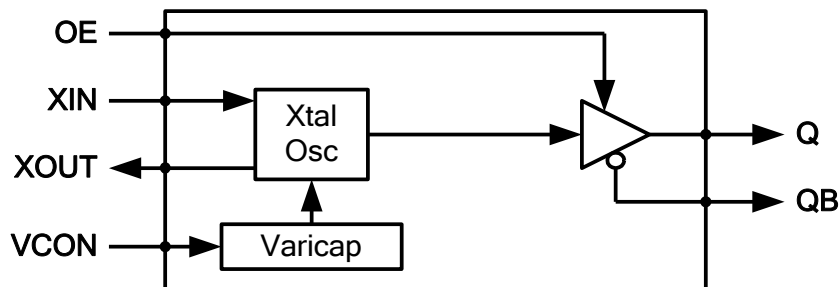
\* Internal 60KΩ pull-up resistor

**OUTPUT ENABLE LOGIC PL586-18**

OE State (Pad 4)	Output Buffers State
0 (Default)	Outputs Enabled
1	Outputs Tri-Stated

\* Internal 60KΩ pull-down resistor

**BLOCK DIAGRAM**



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**PAD ASSIGNMENT**

Pad #	Name	X ( $\mu\text{m}$ )*	Y ( $\mu\text{m}$ )*	Description
1	VCON	-194	-365	Voltage Control input
2	XOUT	-372	-190	Crystal output connection
3	XIN	-372	158	Crystal input connection
4	VDD	-117	329	V <sub>DD</sub> connection
5	QB	140	315	Complementary LVPECL output
6	Q	315	75	LVPECL output
7	VSS	373	-127	GND connection
8	OE	373	-373	Output enable pin. Internal pull up (-15) or pull down (-18).

\* **Note:** Referenced to center of the die.

**ELECTRICAL SPECIFICATIONS**
**1. Absolute Maximum Ratings**

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V <sub>DD</sub>		4.6	V
Input Voltage, DC	V <sub>I</sub>	V <sub>SS</sub> -0.5	V <sub>DD</sub> +0.5	V
Output Voltage, DC	V <sub>O</sub>	V <sub>SS</sub> -0.5	V <sub>DD</sub> +0.5	V
Storage Temperature	T <sub>S</sub>	-65	150	°C
Ambient Operating Temperature	T <sub>A</sub>	-40	85	°C
HBM ESD Protection		2,000		V

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. \*Operating temperature is guaranteed by design. Parts are tested to commercial grade only.



**Low Phase Noise, LVPECL VCXO (for 75MHz to 125MHz Fundamental Crystals)**
**2. Voltage Control Crystal Oscillator**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Pullability *		XTAL $C_1 = 6.6\text{fF}$ , $C_0/C_1 = 260$ $0\text{V} \leq \text{VCON} \leq V_{DD}$ (at $25^\circ\text{C}$ )		$\pm 110$		ppm
		XTAL $C_1 = 8.0$ , $C_0/C_1 = 250$ $0\text{V} \leq \text{VCON} \leq V_{DD}$ (at $25^\circ\text{C}$ )		$\pm 125$		ppm
Varicap Control Range *		$\text{VCON} = 0$ to $V_{DD}$	0		3.3	V
Linearity *		$0.0\text{V} \leq \text{VCON} \leq 3.3\text{V}$		4		%
		$0.3\text{V} \leq \text{VCON} \leq 3.0\text{V}$		3		%
VCON Input Impedance *		DC Input resistance	10			$\text{M}\Omega$
VCON Modulation BW *		$0\text{V} \leq \text{VCON} \leq V_{DD}$ , -3dB		30		kHz

Note: Parameters denoted with an asterisk (\*) represent nominal characterization data and are not production tested to any specific limits.

**3. Crystal Specifications**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	$F_{XIN}$	Fundamental Mode, AT cut	75		125	MHz
Crystal Loading Rating	$C_{L(xtal)}$	$\text{VCON} = 1.65\text{V}$		8		pF
Shunt Capacitance	$C_0$				3.0	pF
Recommended ESR	$R_E$	$C_0 \leq 3.0\text{pF}$ , up to 105MHz			25	$\Omega$
		$C_0 \leq 2.0\text{pF}$			25	$\Omega$
		$C_0 \leq 1.5\text{pF}$			30	$\Omega$

**4. General Electrical Specifications**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$I_{DD}$	Standard LVPECL Loading (See LVPECL Levels Test Circuit, page 4)			50	mA
Operating Voltage	$V_{DD}$		2.97	3.3	3.63	V
Output Clock Duty Cycle		@ $V_{DD} = 1.3\text{V}$ (See LVPECL Transition Time Waveform, page 4)	45	50	55	%
Short Circuit Current				$\pm 50$		mA

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**5. Jitter Specifications**

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period Jitter RMS	At 77.76MHz, with capacitive decoupling between V <sub>DD</sub> and GND. Over 10,000 cycles		2.5		ps
Period Jitter pk-to-pk			20		
Integrated Jitter RMS at 77.76MHz	Integrated 12 kHz to 20 MHz		200		fs
Integrated Jitter RMS at 125MHz	Integrated 12 kHz to 20 MHz		120		fs

**6. Phase Noise Specifications**

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	@1MHz	@10MHz	UNITS
Phase Noise, relative to carrier	77.76MHz	-69	-99	-126	-147	-155	-156	-157	dBc/Hz

Note: Phase Noise measured at VCON = 0.3V to 3.0V.

**7. LVPECL Electrical Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output High Voltage	V <sub>OH</sub>	R <sub>L</sub> = 50 Ω to (V <sub>DD</sub> - 2V) (see figure)	V <sub>DD</sub> - 1.025	V <sub>DD</sub> - 0.950	V <sub>DD</sub> - 0.880	V
Output Low Voltage	V <sub>OL</sub>		V <sub>DD</sub> - 1.810	V <sub>DD</sub> - 1.700	V <sub>DD</sub> - 1.620	V

**8. LVPECL Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t <sub>r</sub>	@20/80% of output waveform			300	ps
Clock Fall Time	t <sub>f</sub>	@80/20% of output waveform			300	ps

