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Low Phase Noise, LVPECL VCXO (for 120MHz to 125MHz Fundamental Crystals)

FEATURES

- Advanced non multiplier VCXO Design for High Performance Crystal Oscillators
- Input/Output Range: 120MHz to 125MHz
- Phase Noise Optimized for 122.88MHz: -70dBc @10Hz, -154dBc @100kHz
- Very low Phase Jitter: 110fs RMS
- High Pull Range: ± 110 ppm
- Linearity: <5%
- Integrated Variable Capacitors
- Complementary LVPECL Outputs
- Power Supply: 3.3V $\pm 10\%$
- Available in Die or Wafer Form

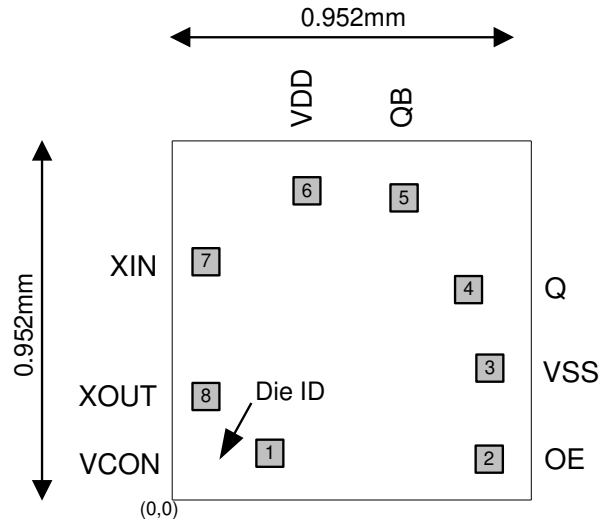
DESCRIPTION

The PL586-25/-28 is a non-multiplier VCXO IC specifically designed to pull fundamental mode crystals from 120MHz to 125MHz. This IC achieves a typical pull range of ± 110 ppm with <5% linearity. The phase noise performance is optimized for close-in performance and with 110fs phase jitter, makes this an ideal solution for all high end clocking applications such as SONET, WiMax, CPRI, OBSAI, Fiber Channel, and any application where performance and quality are required.

DIE SPECIFICATIONS

| Name | Value |
|----------------|-------------------------|
| Size | 952 micron x 952 micron |
| Reverse side | GND |
| Pad dimensions | 80 micron x 80 micron |
| Thickness | 8 mil |

DIE CONFIGURATION



OUTPUT ENABLE LOGIC PL586-25

| OE State (Pad 4) | Output Buffers State |
|------------------|----------------------|
| 0 | Outputs Tri-Stated |
| 1 (Default) | Outputs Enabled |

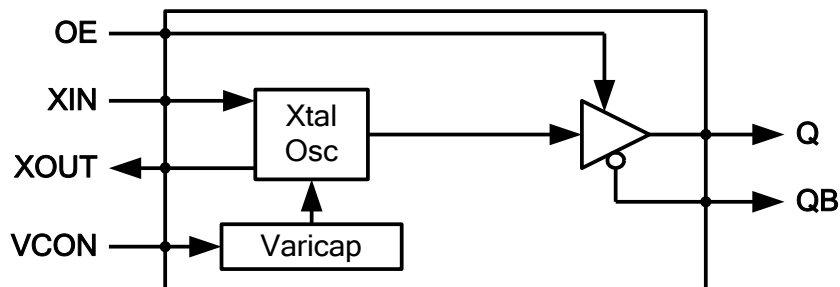
* Internal 60K Ω pull-up resistor

OUTPUT ENABLE LOGIC PL586-28

| OE State (Pad 4) | Output Buffers State |
|------------------|----------------------|
| 0 (Default) | Outputs Enabled |
| 1 | Outputs Tri-Stated |

* Internal 60K Ω pull-down resistor

BLOCK DIAGRAM



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PAD ASSIGNMENT

| Pad # | Name | X (μm)* | Y (μm)* | Description |
|-------|------|----------------------|----------------------|---|
| 1 | VCON | -194 | -365 | Voltage Control input |
| 2 | OE | 373 | -373 | Output enable pin. Internal pull up (-25) or pull down (-28). |
| 3 | VSS | 373 | -127 | GND connection |
| 4 | Q | 315 | 75 | LVPECL output |
| 5 | QB | 140 | 315 | Complementary LVPECL output |
| 6 | VDD | -117 | 329 | V _{DD} connection |
| 7 | XIN | -372 | 158 | Crystal input connection |
| 8 | XOUT | -372 | -190 | Crystal output connection |

* **Note:** Referenced to center of the die.

ELECTRICAL SPECIFICATIONS
1. Absolute Maximum Ratings

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|-------------------------------|-----------------|----------------------|----------------------|-------|
| Supply Voltage | V _{DD} | | 4.6 | V |
| Input Voltage, DC | V _I | V _{SS} -0.5 | V _{DD} +0.5 | V |
| Output Voltage, DC | V _O | V _{SS} -0.5 | V _{DD} +0.5 | V |
| Storage Temperature | T _S | -65 | 150 | °C |
| Ambient Operating Temperature | T _A | -40 | 85 | °C |
| HBM ESD Protection | | 2,000 | | V |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

Low Phase Noise, LVPECL VCXO (for 120MHz to 125MHz Fundamental Crystals)
2. Voltage Control Crystal Oscillator

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---------------------------|---------------|--|------|-----------|------|------------------|
| VCXO Stabilization Time * | $T_{VCXOSTB}$ | From power valid | | | 10 | ms |
| VCXO Pullability * | | XTAL $C_1 = 6.6\text{fF}$, $C_0/C_1 = 260$ $0\text{V} \leq V_{CON} \leq V_{DD}$ (at 25°C) | | ± 110 | | ppm |
| Varicap Control Range * | | $V_{CON} = 0$ to V_{DD} | 0 | | 3.3 | V |
| Linearity * | | $0.0\text{V} \leq V_{CON} \leq 3.3\text{V}$ | | 4 | | % |
| | | $0.3\text{V} \leq V_{CON} \leq 3.0\text{V}$ | | 2.5 | | % |
| VCON Input Impedance * | | DC Input resistance | 10 | | | $\text{M}\Omega$ |
| VCON Modulation BW * | | $0\text{V} \leq V_{CON} \leq V_{DD}$, -3dB | | 30 | | kHz |

Note: Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

3. Crystal Specifications

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|-----------------------------|---------------|---|------|------|------|----------|
| Crystal Resonator Frequency | F_{XIN} | Fundamental Mode, AT cut | 120 | | 125 | MHz |
| Crystal Loading Rating | $C_{L(xtal)}$ | $V_{CON} = 1.65\text{V}$ | | 8 | | pF |
| Shunt Capacitance | C_0 | | | | 3.0 | pF |
| Motional Capacitance | C_1 | Recommended for at least $\pm 100\text{ppm}$ Frequency Pulling | 6.0 | | | fF |
| Recommended ESR | R_E | $C_0 \leq 3.0\text{pF}$ | | | 19 | Ω |
| | | $C_0 \leq 2.5\text{pF}$ | | | 21 | Ω |
| | | $C_0 \leq 2.0\text{pF}$ | | | 22 | Ω |

4. General Electrical Specifications

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|-------------------------|----------|---|------|----------|------|-------|
| Supply Current | I_{DD} | Standard LVPECL Loading (See LVPECL Levels Test Circuit, page 4) | | | 50 | mA |
| Operating Voltage | V_{DD} | | 2.97 | 3.3 | 3.63 | V |
| Output Clock Duty Cycle | | @ $V_{DD} = 1.3\text{V}$ (See LVPECL Transition Time Waveform, page 4) | 45 | 50 | 55 | % |
| Short Circuit Current | | | | ± 50 | | mA |

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5. Jitter Specifications

| PARAMETERS | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|------------------------------------|--|------|------|------|-------|
| Period Jitter RMS | At 122.88MHz, with capacitive decoupling between V _{DD} and GND. Over 10,000 cycles | | 2.5 | | ps |
| Period Jitter pk-to-pk | | | 20 | | |
| Integrated Jitter RMS at 122.88MHz | Integrated 12 kHz to 20 MHz | | 110 | | fs |

6. Phase Noise Specifications

| PARAMETERS | FREQUENCY | @10Hz | @100Hz | @1kHz | @10kHz | @100kHz | @1MHz | UNITS |
|----------------------------------|-----------|-------|--------|-------|--------|---------|-------|--------|
| Phase Noise, relative to carrier | 122.88MHz | -70 | -98 | -125 | -145 | -155 | -156 | dBc/Hz |

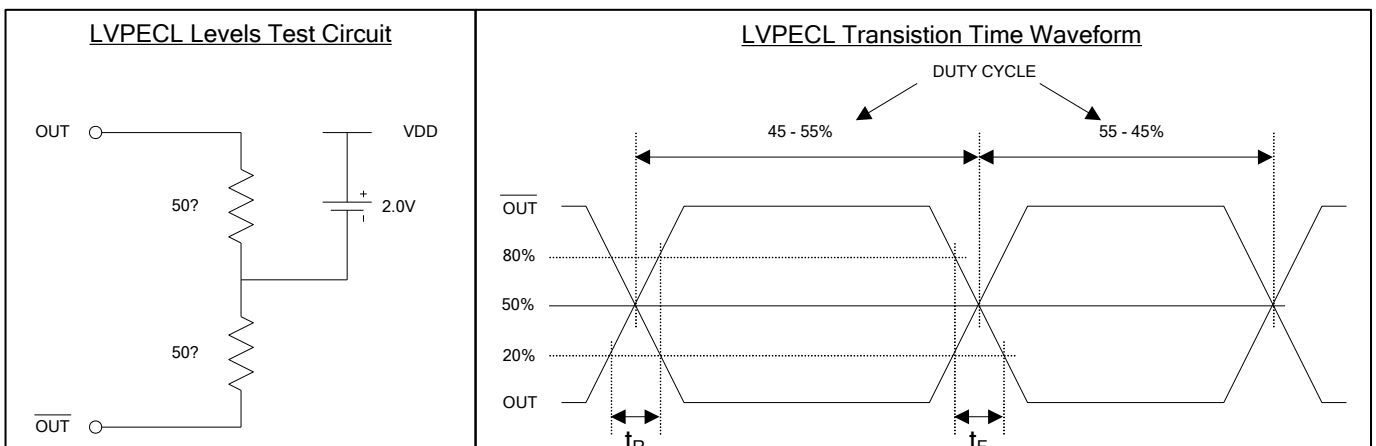
Note: Phase Noise measured at VCON = 0.3V to 3.0V.

7. LVPECL Electrical Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---------------------|-----------------|---|-------------------------|-------------------------|-------------------------|-------|
| Output High Voltage | V _{OH} | R _L = 50 Ω to (V _{DD} - 2V) (see figure) | V _{DD} - 1.025 | V _{DD} - 0.950 | V _{DD} - 0.880 | V |
| Output Low Voltage | V _{OL} | | V _{DD} - 1.810 | V _{DD} - 1.700 | V _{DD} - 1.620 | V |

8. LVPECL Switching Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|-----------------|----------------|----------------------------|------|------|------|-------|
| Clock Rise Time | t _r | @20/80% of output waveform | | | 300 | ps |
| Clock Fall Time | t _f | @80/20% of output waveform | | | 300 | ps |





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ORDERING INFORMATION

For part ordering, please contact our Sales Department:

2180 Fortune Drive, San Jose, CA 95131, USA

Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER

The order number for this device is a combination of the following:

Part number, Package type and Operating temperature range

Part Number PL586-2X XX

Packaging Option

D = Die

W = Wafer

Temperature Range

C=Commercial (0°C to 70°C)

| Order Number | Packaging |
|--------------------------|-------------------|
| PL586-25DC PL586-28DC | Die – Waffle Pack |
| PL586-25WC PL586-28WC | Wafer |

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