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With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

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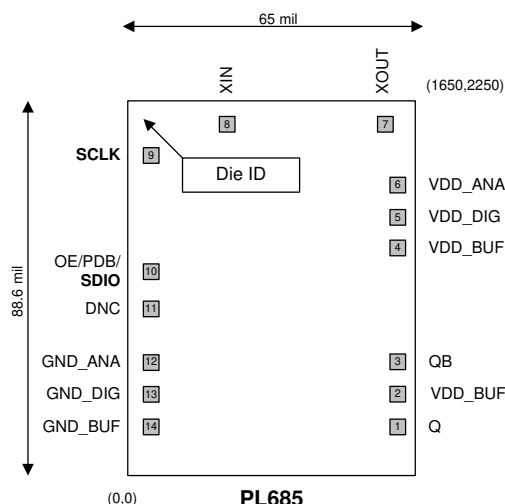
## 19MHz to 250MHz Low Phase-Noise XO PAD CONFIGURATION

### FEATURES

- < 0.6ps RMS phase jitter (12kHz to 20MHz) at 155.52MHz
- 30ps max peak to peak period jitter
- 8bit Switch Capacitor for  $\pm 50$ PPM crystal CLoad tuning
  - Load Capacitance Tuning Range: 8pF to 12pF
- Ultra Low-Power Consumption
  - < 90 mA @155MHz PECL output
  - < 10 $\mu$ A at Power Down (PDB) Mode
- Input Frequency:
  - Fundamental Crystal: 19MHz to 40MHz
- Output Frequency:
  - 19MHz to 250MHz output.
- Output types: LVPECL.
- Programmable OE input polarity selection.
- Power Supply: 3.3V,  $\pm 10\%$
- Operating Temperature Ranges:
  - Commercial: 0°C to 70°C
  - Industrial: -40°C to 85°C
- Available in Die or Wafer

### DESCRIPTION

The PL685-28 is a Dual LC core monolithic IC clock, capable of maintaining sub-1ps RMS phase jitter, while covering a wide frequency output range up to 250MHz, without the use of external components. The high performance and high frequency output is achieved using a low cost fundamental crystal of between 19MHz and 40 MHz. The PL685-28 is designed to address the demanding requirements of high performance applications such as Fiber Channel, serial ATA, Ethernet, SAN, SONET/SDH, etc.



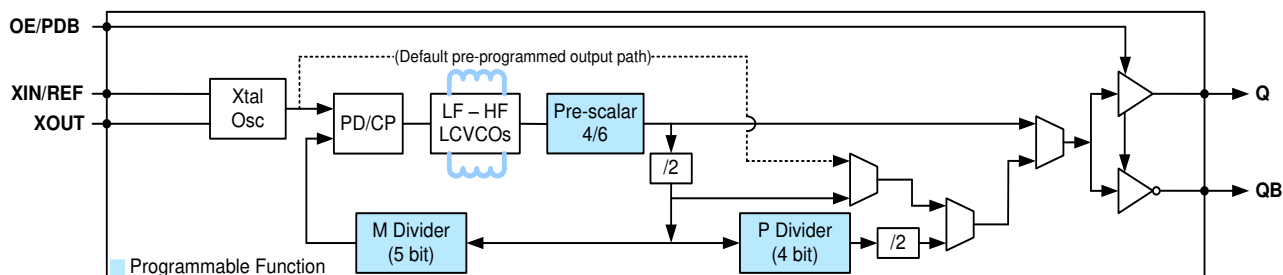
### DIE SPECIFICATIONS

| Name           | Value                 |
|----------------|-----------------------|
| Size           | 65 x 88.6 mil         |
| Reverse side   | GND                   |
| Pad dimensions | 80 micron x 80 micron |
| Thickness      | 8 mils                |

### OUTPUT ENABLE CONTROL

| OE Select (Programmable) | OE          | State          |
|--------------------------|-------------|----------------|
| 0                        | 0 (Default) | Output enabled |
|                          | 1           | Tri-state      |
| 1 (Default)              | 0           | Tri-state      |
|                          | 1 (Default) | Output enabled |

### BLOCK DIAGRAM



**19MHz to 250MHz Low Phase-Noise XO****PAD ASSIGNMENT**

| Name        | Pad # | X (μm) | Y (μm) | Description                                                                                                                                                                                                                                              |
|-------------|-------|--------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Q           | 1     | 1551   | 220    | Output buffer                                                                                                                                                                                                                                            |
| VDD_BUF     | 2     | 1551   | 448    | VDD connection for buffer circuitry                                                                                                                                                                                                                      |
| QB          | 3     | 1551   | 676    | Output buffer                                                                                                                                                                                                                                            |
| VDD_BUF     | 4     | 1551   | 1390   | VDD connection for buffer circuitry                                                                                                                                                                                                                      |
| VDD_DIG     | 5     | 1551   | 1552   | VDD connection for digital circuitry                                                                                                                                                                                                                     |
| VDD_ANA     | 6     | 1551   | 1790   | VDD connection for analog circuitry                                                                                                                                                                                                                      |
| XOUT        | 7     | 1503   | 2156   | Output connection to crystal                                                                                                                                                                                                                             |
| XIN         | 8     | 630    | 2156   | Crystal input connection                                                                                                                                                                                                                                 |
| SCLK        | 9     | 99     | 2060   | The serial interface uses this pin for the serial clock input (SCLK), during programming.                                                                                                                                                                |
| OE/PDB/SDIO | 10    | 99     | 1256   | This pin may be programmed as output enable (OE), or power-down (PDB) pin.<br>The serial interface uses this pin for the serial data input (SDIO) during programming. This pin incorporates an Internal pull-up resistor of 60KΩ for OE, PDB operations. |
| DNC         | 11    | 99     | 970    | Do not connect                                                                                                                                                                                                                                           |
| GND_ANA     | 12    | 99     | 700    | GND connection for analog circuitry                                                                                                                                                                                                                      |
| GND_DIG     | 13    | 99     | 532    | GND connection for digital circuitry                                                                                                                                                                                                                     |
| GND_BUF     | 14    | 99     | 364    | GND connection for buffer circuitry                                                                                                                                                                                                                      |

**19MHz to 250MHz Low Phase-Noise XO****FUNCTIONAL DESCRIPTION**

PL685 family of products is an advanced, programmable LCVCO clock IC that is designed to meet the most stringent performance specifications for phase noise, jitter, and power consumption.

There are two main types of VCOs, a) Ring Oscillator, b) LC Tank oscillator. An LCVCO is made up of an LC tank oscillator. Although a Ring Oscillator has very good performance, and has a good tuning range, its phase noise and jitter performance, in particular at higher frequencies, degrades.

On the other hand, an LCVCO has an outstanding phase noise and jitter performance, even at higher frequencies. PL685 family of products takes advantage of this state of the art technology, and incorporates the LC tank on-chip, for optimal performance.

PL685 family of products exhibit very low phase noise/phase jitter and peak to peak jitter, wide tuning range, and very low-power. All members of the PL685 family accept a low-cost fundamental crystal input of 19MHz to 40MHz or a reference clock input of up to 800MHz and its flexible core is capable of producing any output frequency between 19MHz to 800MHz. The PL685-28 specifically is limited to 250MHz. See the PL685-88 for operation up to 800MHz.

**PLL Programming**

The PLL in the PL685 family is fully programmable. The PLL is equipped with a Prescaler to divide down the VCO frequency, and a 5-bit VCO frequency feedback loop divider (M-Counter). The output of the PLL is transferred to a 4-bit post VCO divider (P-Counter), to achieve the desired output frequency.

**OE (Output Enable)**

The OE pin in PL685 family, through programming, can be configured to support OE pin activation with a logic '1' or logic '0', to provide you with the desired enable polarity.

| OE Select<br>(Programmable) | OE          | State          |
|-----------------------------|-------------|----------------|
| 0                           | 0 (Default) | Output enabled |
|                             | 1           | Tri-state      |
| 1 (Default)                 | 0           | Tri-state      |
|                             | 1 (Default) | Output enabled |

The OE pin incorporates a 60K $\Omega$  resistor to either pull-up or pull-down to the default state when the OE pin is left open.

## 19MHz to 250MHz Low Phase-Noise XO

### ELECTRICAL SPECIFICATIONS

#### 1. ABSOLUTE MAXIMUM RATINGS

| PARAMETERS                                              | SYMBOL   | MIN  | MAX          | UNITS |
|---------------------------------------------------------|----------|------|--------------|-------|
| Supply Voltage                                          | $V_{DD}$ |      | 4.6          | V     |
| Input Voltage, dc                                       | $V_I$    | -0.5 | $V_{DD}+0.5$ | V     |
| Output Voltage, dc                                      | $V_O$    | -0.5 | $V_{DD}+0.5$ | V     |
| Storage Temperature                                     | $T_S$    | -65  | 150          | °C    |
| Ambient Operating Temperature (industrial temperature)* | $T_{AI}$ | -40  | 85           | °C    |
| Ambient Operating Temperature (commercial temperature)  | $T_{AC}$ | 0    | 70           | °C    |
| Junction Temperature                                    | $T_J$    |      | 125          | °C    |
| ESD Protection, Machine Model                           |          | 200  |              | V     |
| ESD Protection, Human Body Model                        |          | 2    |              | kV    |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. \*Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

#### 2. GENERAL ELECTRICAL SPECIFICATIONS

| PARAMETERS                             | SYMBOL    | CONDITIONS                                                                                                                   | MIN  | TYP | MAX  | UNITS |
|----------------------------------------|-----------|------------------------------------------------------------------------------------------------------------------------------|------|-----|------|-------|
| Supply Current, Dynamic                | $I_{DDQ}$ | LVPECL, 155.52MHz, 3.3V                                                                                                      |      |     | 90   | mA    |
| Supply Current, Dynamic<br>PDB Enabled |           | PDB = 0, 3.3V                                                                                                                |      |     | 10   | uA    |
| Output Enable Time                     | $t_{OE}$  | OE logic 0 to logic 1, $T_a=25^\circ\text{C}$ .<br>Add one clock period to this<br>measurement for a usable clock<br>output. |      |     | 50   | ns    |
| Power Up Time                          | $T_{PU}$  | PDB logic 0 to logic 1, $T_a=25^\circ\text{C}$                                                                               |      |     | 10   | ms    |
| Operating Voltage                      | $V_{DD}$  |                                                                                                                              | 2.97 | 3.3 | 3.63 | V     |
| Power Up Ramp Rate                     | $t_{PU}$  | Time for $V_{DD}$ to reach 90% $V_{DD}$ .<br>Power ramp must be monotonic.                                                   | 0.1  |     | 100  | ms    |
| Auto-Calibration Time                  | $t_{AC}$  | At power up                                                                                                                  |      |     | 10   | ms    |
| Output Clock Duty Cycle                |           | @ $V_{DD} - 1.3V$                                                                                                            | 45   | 50  | 55   | %     |

## 19MHz to 250MHz Low Phase-Noise XO

### 4. CRYSTAL SPECIFICATIONS

| PARAMETERS                  | SYMBOL           | CONDITIONS                     | MIN | TYP | MAX | UNITS    |
|-----------------------------|------------------|--------------------------------|-----|-----|-----|----------|
| Crystal Resonator Frequency | $F_{XIN}$        | Parallel Fundamental Mode      | 19  |     | 40  | MHz      |
| Crystal Cload               | $C_{L\_Crystal}$ | $V_{DD} = 3.3V$ , programmable | 8   |     | 12  | pF       |
| Shunt Capacitance           | $C_{0\_Crystal}$ |                                |     |     | 3.5 | pF       |
| Recommended ESR             | $R_E$            | AT cut                         |     |     | 50  | $\Omega$ |

### 5. JITTER SPECIFICATIONS

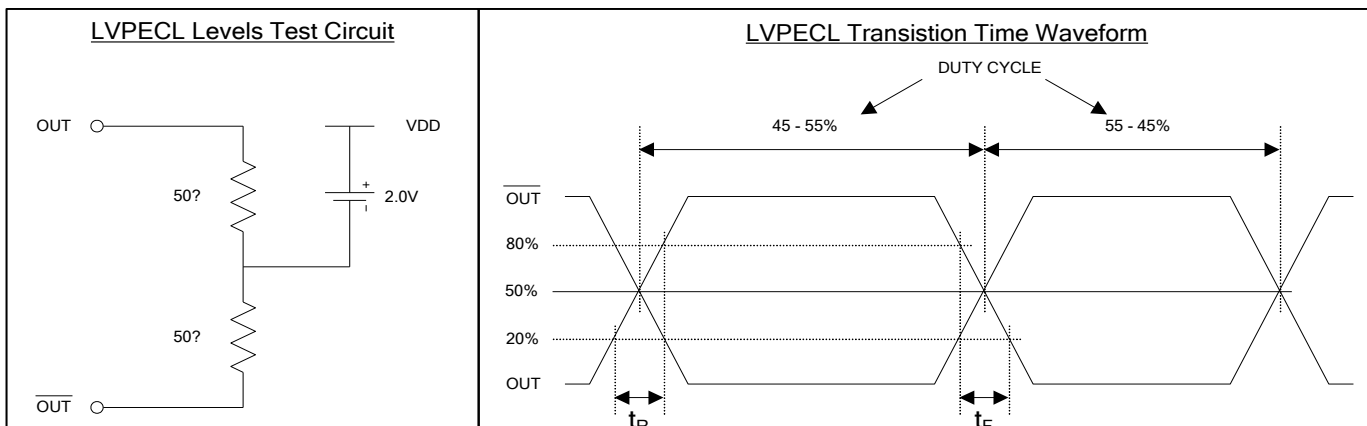
| PARAMETERS              | FREQUENCY | CONDITIONS                     | MIN | TYP  | MAX | UNITS |
|-------------------------|-----------|--------------------------------|-----|------|-----|-------|
| RMS Phase Jitter        | 155.52MHz | 10kHz to 20MHz, $XIN=38.88MHz$ |     | 0.56 |     | ps    |
| Period Jitter, Pk-to-Pk | 155.52MHz | 10K cycles, $XIN=38.88MHz$     |     | 30   |     | ps    |

### 6. PHASE NOISE SPECIFICATIONS

| PARAMETERS                                 | Freq.<br>(MHz) | @<br>10Hz | @<br>100Hz | @<br>1KHz | @<br>10KHz | @<br>100KHz | @<br>1MHz | @<br>10MHz | UNITS  |
|--------------------------------------------|----------------|-----------|------------|-----------|------------|-------------|-----------|------------|--------|
| Phase Noise, relative to carrier (typical) | 155.52         | -58       | -95        | -119      | -124       | -129        | 135       | 148        | dBc/Hz |

### 7. LVPECL OUTPUTS (Q, QB)

| PARAMETERS              | SYMBOL     | CONDITIONS                                               | MIN   | TYP   | MAX   | UNITS |
|-------------------------|------------|----------------------------------------------------------|-------|-------|-------|-------|
| Output High Voltage     | $V_{OH}$   | Q, QB<br>Standard LVPECL Termination,<br>$V_{DD} = 3.3V$ | 2.275 | 2.350 | 2.420 | V     |
| Output Low Voltage      | $V_{OL}$   |                                                          | 1.490 | 1.600 | 1.680 | V     |
| Output Frequency        | $F_{out}$  | 3.3V                                                     | 19    |       | 250   | MHz   |
| Output Rise, Fall Times | $t_r, t_f$ | 20% - 80% of $Q_{pp}/QB_{pp}$                            |       | 200   | 300   | ps    |
| Output Voltage Swing    | $V_{pp}$   | Q, QB                                                    | 550   | 800   | 900   | mV    |



**19MHz to 250MHz Low Phase-Noise XO****ORDERING INFORMATION**

**For part ordering, please contact our Sales Department:**

2180 Fortune Drive, San Jose, CA 95131, USA

Tel: (408) 944-0800 Fax: (408) 474-1000

**PART NUMBER**

The order number for this device is a combination of the following:  
Part number, Package type, Thickness and Operating temperature range

**Part Number** PL685-28 XX

**Packaging Option** \_\_\_\_\_

D = Die

W = Wafer

**Temperature Range** \_\_\_\_\_

C=Commercial (0°C to 70°C)

| Order Number P/N | Output Frequency Range | Packaging Option  |
|------------------|------------------------|-------------------|
| <b>PECL</b>      |                        |                   |
| PL685-28DC       | ≤250MHz                | Waffle Pack (Die) |
|                  |                        |                   |
| PL685-28WC       | ≤250MHz                | Wafer             |

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