Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

News & Views
Second Quarter, May 2000
Newsletter for Altera Customers

Altera Announces the Nios Processor for Embedded Systems Development

Altera is a leader in providing the key elements required for successful system-on-a-programmable-chip (SOPC) designs, including high performance, full-featured devices, integrated development tools, and a comprehensive portfolio of intellectual property (IP). Recognizing the importance of microprocessors in SOC designs, Altera has established itself as the preeminent source of processor IP through strong partnerships with industry leaders. Altera now enhances this processor IP selection with Excalibur™ embedded processor programmable logic device (PLD) solutions. Consisting of both hard and soft core technologies that integrate RISC processors into PLDs, the Excalibur embedded processor solutions offer the widest range of capabilities and the high performance of dedicated hardware implementation. With the introduction of the Excalibur embedded processor PLD solutions, designers can reap all the benefits of SOPC design.

Advantages of SOPC

The strengths of SOC design include higher integration and increased system performance. SOPC designs add additional benefits such as programmability and fast time-to-market, with the flexibility of PLDs. With these programmable devices, a designer can implement several different iterations of a system in hardware in a fraction of the time required to implement a custom component version. This flexibility allows designers to not only develop a product in a shorter amount of time, but to explore different system architectures and feature sets to deliver the best possible combination in their product. By fully integrating the processor into the PLD design flow, the Excalibur solutions give system designers unprecedented freedom to determine which functions should be executed in software and which would benefit the most from dedicated hardware implementation.

Excalibur Solutions

The Altera Excalibur solutions consist of the following families:

- The Nios™ family of soft core embedded processors—a configurable 16- or 32-bit embedded RISC processor
- The ARM®-based embedded processor family—an ARM9 Thumb® embedded processor core with 32-bit architecture and a 32-bit RISC engine
- The MIPS-based® embedded processor family—a MIPS 4Kc™ embedded processor core with 32-bit architecture and R4000™ TLB and privileged-mode extensions.

The first Excalibur embedded processor PLD solution is the Nios family, a 16- or 32-bit embedded RISC soft core processor that is easily configured to meet several different demands, and rapidly integrated into any Altera-based design. Although the Nios embedded processors are initially optimized for APEX™ devices, they

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Introducing the Excalibur Development Kit Featuring Nios

The Development Kit that Gets You on the Cutting Edge

The Nios™ soft core embedded processor, the first of Altera's new Excalibur™ embedded processor solutions to ship, delivers just what you need to create system-on-a-programmable-chip (SOPC) designs.

EXCALIBUR™

This new flexible embedded processor solution offers a 32-bit configuration, up to 50 MIPS performance, and an equivalent volume price point of $5. The development kit is available now with everything you need to get started.

A Complete Solution for Only $995

This Excalibur Development Kit contains:

- Nios Configurable RISC Embedded Processor Core and Peripherals
- Quartus™ Programmable Logic Development Software
- GNUPro® C/C++ Compiler and Debugger from Cygnus®, a Red Hat® Company
- ByteBlasterMV™ Download Cable
- Development Board Including an APEX™ EP20K200E Device
- Reference Design and Documentation

Free Hands-on Workshops

Intensive three-hour workshops, starting in June, will teach you how to create an SOPC design using the Nios soft core embedded processor in an APEX device. You will develop and compile C code, then execute and troubleshoot it on the development board. You will also learn about the GNUPro Compiler and Debugger from Cygnus, a Red Hat company, included in the Excalibur Development Kit.

Register Now!

To reserve your space at the **FREE** Excalibur workshop nearest you, or to find out more about this revolutionary development system, visit Altera's web site at **http://www.altera.com/workshop**.

Win a Free Excalibur Development Kit!

Each workshop will feature a drawing for a free Excalibur Development Kit. You must be present to win, so sign up today.

ALTERA®

The Programmable Solutions Company®

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Ken Lau, Publisher
Greg Steinke,
Technical Editor
101 Innovation Drive
San Jose, CA 95134
Tel: (408) 544-7000
Fax: (408) 544-7809
n_v@altera.com

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will also be available for other Altera device architectures, including ACEX™ devices for low-cost implementations and future device families for enhanced performance. The hard core Excalibur solutions are based on ARM and MIPS Technologies, Inc. processors. They are implemented in Altera's APEX architecture, and will provide high-performance, embedded peripherals within royalty-free, off-the-shelf products. The Excalibur solutions are ideal for many embedded applications, including computer peripherals, industrial and automotive control, image processing, set-top boxes, and other communications applications. Figure 1 shows the families of the Excalibur embedded processor solution and their relative performance levels. Figure 2 shows the roadmap for future Nios embedded processors.

Figure 1. Excalibur Embedded Processor Solutions

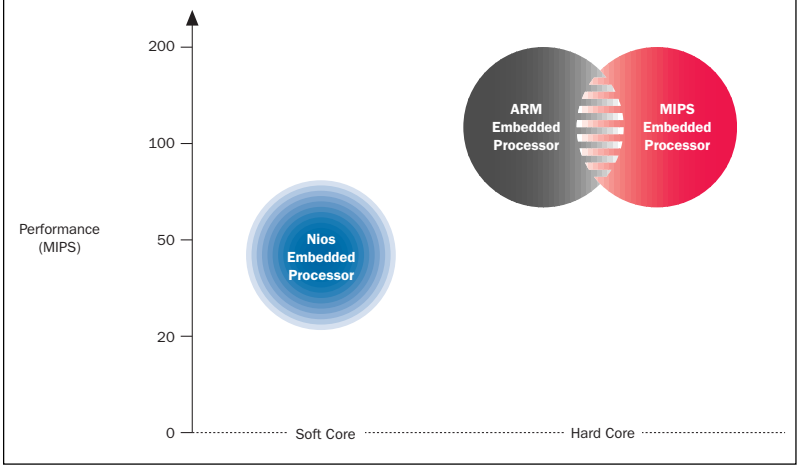


Figure 2. Nios Roadmap

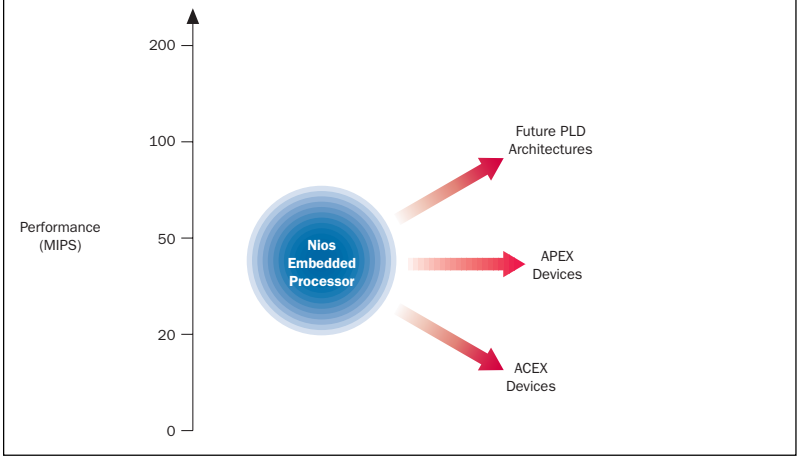


Table 1. Nios Configurations & Resource Usage in an EP20K100E Device

Nios Configuration	Data Width	Address Width	% of Total LEs	% of Total ESBs *(1)*	MHz	Cost of Implementation
16 bit	16	16	25	8 to 40	50	$10
32 bit	32	32	33	15 to 77	48	$13

Note:
(1) Based on register file size.

The Nios Family of Configurable Soft Core Embedded Processors

The Nios family of embedded processors is the first 16- or 32-bit processor core to be designed specifically for programmable logic implementation, and as a result, can perform at speeds up to 50 million instructions per second (MIPS). Designed with a five-stage pipeline that executes one instruction per clock cycle, the Nios family is also user-configurable for meeting different embedded design needs, supporting a 16- or 32-bit data width and a register file depth ranging from 32 to 512 general-purpose registers (for more information on the Nios architecture, see on page 20). Besides performance and configurability, Nios processors are also optimized for PLD resource efficiency, resulting in a lower-cost implementation than most off-the-shelf processors. Nios can be configured in many ways to suit different applications. Table 1 illustrates two Nios configurations, their speed and resource utilizations, and resulting costs.

Nios Development Environment

The Nios processor is more than the latest generation of processor IP optimized for programmable logic. Altera also provides all the elements necessary for a designer to develop a Nios-based system. Nios users can integrate the Nios embedded processor into their Altera designs with the MegaWizard® Plug-In. The MegaWizard Plug-In is a menu-driven application that allows users to specify the parameters they desire for their Nios embedded processor. Based on those parameters, the MegaWizard Plug-In Manager generates a netlist description of the specific Nios embedded processor that can be integrated into any Altera design via the Quartus™ development system.

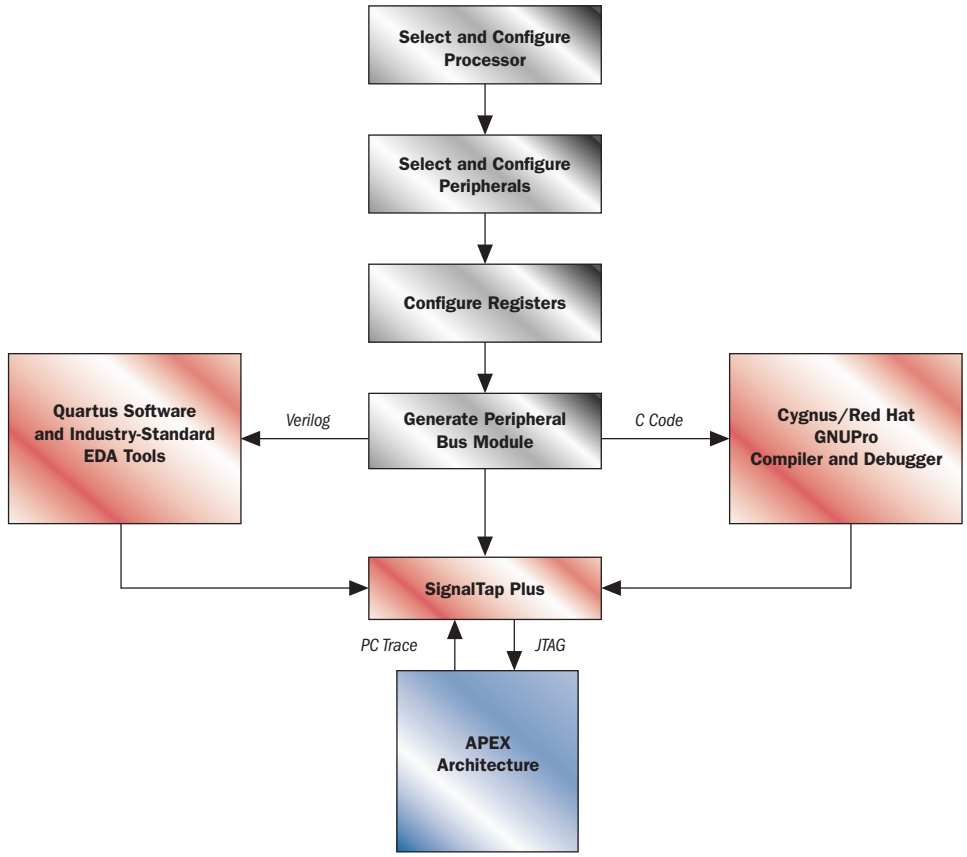
Several peripherals are also available for use with the Nios family of embedded processors, including a universal asynchronous receiver/transmitter (UART), a timer/counter, a memory controller (SRAM, ROM, and FLASH), and a parallel I/O (PIO) module. Any of these can be easily integrated into a user's design along with their unique Nios configuration. For coding support, Altera has partnered with Cygnus®, a Red Hat® company, to provide the powerful yet familiar GNU®-based C/C++ compiler and assembler. A source-level debugger accesses the device through a serial port, providing run control and access to the memory and register file. Figure 3 shows the development flow for the Excalibur embedded processor PLD solution.

Excalibur Development Kit, Featuring Nios

To support the Nios family of soft core embedded processors, Altera offers the Excalibur Development Kit, featuring the Nios embedded processor, which contains all the software and hardware components a designer needs to begin using the Nios embedded processor immediately. The kit includes the following items:

- Nios soft-core embedded processor
- C/C++ compiler, assembler, debugger, and documentation
- Nios peripherals (UART, memory interface, timer/counter, and PIO module)
- Quartus development software (supports APEX devices and SignalTap™ embedded logic analysis)
- ByteBlasterMV™ download cable
- Development board (including an APEX EP20K200E device, SRAM/FLASH, expansion/prototype connectors, and processor trace port)
- Software drivers (UART, timer/counter, and PIO module)
- SOPC reference design
- Nios user manual and programmer reference manual

Figure 3. Excalibur Workflow Simplifies SOPC Designs



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Altera Announces the Nios Processor for Embedded Systems Development, continued from page 5

Licensing and Availability

The Nios embedded processor is the first member of the Excalibur solutions and is available now. The ARM- and MIPS-based members of the Excalibur family will be available as royalty-free standard products in the fourth quarter of 2000. Designers can use the Nios embedded processor to develop Nios-based designs free of charge. Products that ship with the Nios embedded processor are subject to a zero-cost license which is available on-line at the Altera web site (**http://www.altera.com**). The Excalibur Development Kit is now available and contains information on obtaining a product license. You can also contact your local Altera sales office or representative or visit Altera's web site. For more detailed information on developing with the Nios family, attend one of the free Nios workshops scheduled worldwide (see "Sign Up Now for Free Excalibur Workshops" below for more information).

Altera & Red Hat Form Partnership to Provide Development Software for Nios

Nios™

Altera and Red Hat®, Inc. worked together to provide Altera users with a powerful and complete software development environment for the Nios™ family of soft core embedded processors. Through close collaboration, they created a suite of the GNUPro® embedded system tools, including a C/C++ compiler, assembler and debugger, specifically optimized to support the Nios instruction set. This suite of tools from Cygnus®, a Red Hat® company, is included in the Excalibur™ Development Kit, along with all the other components needed to begin using the Nios embedded processor immediately.

"Our work with Red Hat signifies our commitment to deliver a robust and open development platform for embedded systems designers," said Cliff Tong, VP of Corporate Marketing. "With the Excalibur Development Kit featuring the Nios embedded processor, Altera provides a valuable integrated platform for hardware and software codevelopment."

"Cygnus and Red Hat are well known in the embedded systems industry as one of the most highly-respected providers of tools and operating systems," added Mike Phipps, Director of Marketing at Altera. "With Red Hat's backing, our users get familiar and dependable tools that are fully supported, tested and certified."

Altera and Red Hat will continue their future support of the Nios embedded processor with a port of eCos, the embedded configurable real time operating system.

APEX

Eight APEX 20KE Devices Now Shipping

Four more APEX™ 20KE devices have been released, making a total of eight APEX 20KE devices now shipping: EP20K60E, EP20K100E, EP20K200E, EP20K300E, EP20K400E, EP20K600E, EP20K1000E, and EP20K1500E devices. These devices are available in many advanced packages, including FineLine BGA™ packages. The remaining APEX 20KE devices are scheduled to ship in the third quarter of 2000. Software support is currently available in the Quartus™ software version 2000.05 for all devices except the EP20K30E device (see Table 1).

True-LVDS Support in APEX 20KE Devices

Altera® APEX 20KE devices now offer the True-LVDS™ solution with a data transfer rate up to 840 megabits per second (Mbps) per channel. This specification exceeds the widely accepted low-voltage differential signaling (LVDS) standard data transfer rate of 624 Mbps. The APEX 20KE programmable LVDS bandwidth is now 26.8 gigabits per second (Gbps).

5.0-V Tolerant APEX 20K & APEX 20KE Devices

The APEX 20K device family has been enhanced to provide a 5.0-V tolerant I/O buffer, providing full compliance with the 5.0-V peripheral component interconnect (PCI) specification. These 5.0-V tolerant devices are now shipping.

You can use APEX 20KE devices with an additional external resistor to make these devices 5.0-V tolerant and provide flexibility for system design. The technical details for this improvement are described in the *5.0-V Tolerance in APEX 20KE Devices White Paper* on the Altera web site (**http://www.altera.com**).

Table 1. APEX 20KE Device & Quartus Software Support Availability

Device	Package	Software Support Availability
EP20K30E	144-pin TQFP *(1)*	Q3 2000
	144-pin FineLine BGA	Q3 2000
	208-pin PQFP *(1)*	Q3 2000
	324-pin FineLine BGA	Q3 2000
EP20K60E	144-pin TQFP	Now
	144-pin FineLine BGA	Now
	208-pin PQFP	Now
	240-pin PQFP	Now
	324-pin FineLine BGA	Now
	356-pin BGA *(1)*	Now
EP20K100E	144-pin TQFP	Now
	144-pin FineLine BGA	Now
	208-pin PQFP	Now
	240-pin PQFP	Now
	324-pin FineLine BGA	Now
	356-pin BGA	Now
EP20K160E	144-pin TQFP	Now
	208-pin PQFP	Now
	240-pin PQFP	Now
	356-pin BGA	Now
	484-pin FineLine BGA	Now
EP20K200E	208-pin PQFP	Now
	240-pin PQFP	Now
	356-pin BGA	Now
	484-pin FineLine BGA	Now
	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K300E	240-pin RQFP *(1)*	Now
	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K400E	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K600E	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now
EP20K1000E	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now
EP20K1500E	652-pin BGA	Now
	1,020-pin FineLine BGA	Now

Note:
(1) TQFP: thin quad flat pack, PQFP: plastic quad flat pack, BGA: ball-grid array, RQFP: power quad flat pack

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APEX 20K Product Transition

Altera is migrating the 2.5-V EP20K400 device from a 0.25-µm process to a 0.22-µm process. Information regarding this device migration can be found in process change notification (PCN) 0005, available on the Altera web site.

ACEX

ACEX 1K Devices Shipping Now

ACEX 1K devices are now shipping in all packages in the 30,000, 50,000, and 100,000 gate densities.

ACEX™ 1K devices are now shipping in all packages in the 30,000, 50,000, and 100,000 gate densities (see Table 2). These cost-optimized devices are especially well suited for low-cost, high-performance communications applications, and can be used to attain the lowest cost per programmable logic device (PLD) for high-volume designs.

Table 2. ACEX 1K Device Offerings

Device	Package	Availability
EP1K10	100-pin TQFP	August 2000
	144-pin TQFP	August 2000
	208-pin PQFP	August 2000
	256-pin FineLine BGA	August 2000
EP1K30	144-pin TQPF	Now
	208-pin PQFP	Now
	256-pin FineLine BGA	Now
EP1K50	144-pin TQFP	Now
	208-pin PQFP	Now
	256-pin FineLine BGA	Now
	484-pin FineLine BGA	Now
EP1K100	208-pin PQFP	Now
	256-pin FineLine BGA	Now
	484-pin FineLine BGA	Now

ACEX 1K devices provide full phase-locked loop (PLL) capability for ClockLock™ and ClockBoost™ features in every -1 and -2 speed grade device, embedded dual-port RAM, and full 64-bit, 66-MHz PCI compliance. Developed on an innovative 0.22-µm/0.18-µm hybrid process, and featuring a 2.5-V core operating voltage, ACEX 1K devices offer an ideal combination of cost, performance, and features.

Full software support for ACEX 1K devices is available from the MAX+PLUS® II software version 9.6. In addition, a wide range of ACEX-optimized intellectual property (IP) functions can now be found at the Altera IP MegaStore™ online store.

ACEX 2K Devices Coming Soon

The 1.8-V ACEX 2K device family will be released soon. These devices range from 20,000 to 150,000 typical gates and provide additional benefits in cost and performance for high-volume communications designs. These devices also offer a feature set that includes enhanced PLL capabilities, advanced I/O standard support, and dual-port embedded RAM. ACEX 2K device support will be available from the Quartus software in the second half of 2000.

FLEX

All FLEX 10KE Devices Available

All EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E, and EPF10K200S devices are now shipping in -1, -2, and -3 speed grades. These devices are fabricated on a 0.22-µm process and have a programmable input buffer delay for full 64-bit, 66-MHz PCI compliance.

FLEX® 10KE devices are offered with the PLL feature in -1 and -2 speed grades to reduce clock skew and allow clock multiplication. These devices have an "X" suffix in the ordering code (e.g., EPF10K100EQC208-1X). To assist designers in implementing their projects in FLEX 10KE devices, the MAX+PLUS II software offers design support for all device package options. Table 3 shows all of the 2.5-V FLEX 10KE device packages and speed grades.

FLEX 10K Product Transitions

2.5-V EPF10K50E and EPF10K200E devices have migrated from a 0.25-µm process to a 0.22-µm process. All other members of the FLEX 10KE family are already manufactured on a 0.22-µm process. EPF10K50V devices are migrating from a 0.30-µm, 3-layer-metal

Table 3. FLEX 10KE Devices

Device	Offerings	Speed Grade
EPF10K30E	144-pin TQFP	-1, -2, -3
	208-pin PQFP	-1, -2, -3
	256-pin FineLine BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X
EPF10K50S	144-pin TQFP	-1, -2, -3
	208-pin PQFP	-1, -2, -3
	240-pin PQFP	-1, -2, -3
	256-pin FineLine BGA	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X
EPF10K100E	208-pin PQFP	-1, -2, -3
	240-pin PQFP	-1, -2, -3
	256-pin FineLine BGA	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X
EPF10K130E	240-pin PQFP	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	600-pin BGA	-1, -2, -3
	672-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X
EPF10K200S	240-pin RQFP	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	600-pin BGA	-1, -2, -3
	672-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X

process to a 0.30-µm, 4-layer-metal process in September 2000. Table 4 outlines the process migration schedule and lists the reference documentation associated with this migration. You can download these documents from the Customer Notifications page on the Altera web site at **http://www.altera.com.**

FLEX 10KE Industrial-Temperature Devices

All FLEX 10KE devices are now available in industrial-temperature grades. Table 5 lists the industrial-temperature FLEX 10KE devices.

Table 4. FLEX 10K Device Migration

Device	Core Voltage (V)	Date	Reference	Process (µm)
EPF10K10A	3.3	Done	PCN 9810	0.30
EPF10K30A	3.3	Done	PCN 9810	0.30
EPF10K50V	3.3	Done	PCN 9810	0.30 *(1)*
		Sept. 2000	PCN 9915	0.30 *(2)*
EPF10K100A	3.3	Done	PCN 9810	0.30
EPF10K10	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K20	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K30	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K50	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K50E	2.5	Done	PCN 9911	0.22
EPF10K200E	2.5	Done	PCN 9911	0.22

Notes:
(1) 3-layer metal process.
(2) 4-layer metal process.

Table 5. FLEX 10KE Industrial-Temperature Device Availability

Device	Availability
EPF10K30EQI208-2	Now
EPF10K30EFI256-2	Now
EPF10K50ETI144-2	Now
EPF10K50EQI240-2	Now
EPF10K50EFI256-2	Now
EPF10K50SQI208-2	Now
EPF10K50SBI356-2	Now
EPF10K50SFI484-2	Now
EPF10K100EQI208-2	Now
EPF10K100EFI256-2	Now
EPF10K100EFI484-2	Now
EPF10K130EQI240-2	Now
EPF10K130EBI356-2	Now
EPF10K130EFI484-2	Now
EPF10K200EBI600-2	Now
EPF10K200SRI240-2	Now
EPF10K200SBI356-2	Now
EPF10K200SFI672-2	Now

All FLEX 10KE devices are now available in industrial-temperature grades.

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MAX

MAX 7000A Devices

The feature-rich MAX® 7000A devices support enhanced in-system programmability (ISP), MultiVolt™ I/O pins, hot-socketing capability and pin compatibility with the industry-standard MAX 7000 devices. 3.3-V MAX 7000A devices range from 32 to 512 macrocells with propagation delays as fast as 4.5 ns. All MAX 7000A devices are available in industrial-temperature grades. Table 6 shows MAX 7000A device commercial package and speed-grade options.

MAX 7000B devices feature enhanced ISP, MultiVolt I/O pins, and pin compatibility with the industry standard MAX 7000 devices.

Table 6. MAX 7000AE Commercial-Temperature Devices

Device	Package	Speed Grade
EPM7032AE	44-pin PLCC *(1)*	-4, -7, -10
	44-pin TQFP	-4, -7, -10
EPM7064AE	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
	49-pin Ultra FineLine BGA *(2)*	-4, -7, -10
	100-pin TQFP	-4, -7, -10
	100-pin FineLine BGA	-4, -7, -10
EPM7128AE	84-pin PLCC	-5, -7, -10
	100-pin TQFP	-5, -7, -10
	100-pin PQFP	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	169-pin Ultra FineLine BGA	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7256AE	100-pin TQFP	-5, -7, -10
	100-pin FineLine BGA	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	208-pin PQFP	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7512AE	144-pin TQFP	-5, -7, -10, -12
	208-pin PQFP	-5, -7, -10, -12
	256-pin BGA	-5, -7, -10, -12
	256-pin FineLine BGA	-5, -7, -10, -12

Notes:
(1) PLCC: plastic J-lead chip carrier.
(2) Ultra FineLine BGA packages are Altera's 0.8-mm pitch BGA packages.

MAX 7000B Devices Support Advanced I/O Standards

With support for advanced I/O standards such as Gunning transceiver logic plus (GTL+) and stub-series terminated logic for 2.5 V (SSTL-2) and 3.3-V SSTL-3, MAX 7000B devices offer a flexible solution to design requirements. 2.5-V MAX 7000B devices range from 32 to 512 macrocells with propagation delays as fast as 3.5 ns. Additionally, MAX 7000B devices feature enhanced ISP, MultiVolt I/O pins, and pin compatibility with the industry-standard MAX 7000 devices. Table 7 shows all commercial package and speed grade options. Contact your Altera sales representative for device availability.

Table 7. MAX 7000B Commercial-Temperature Devices

Device	Package	Speed Grade
EPM7032B	44-pin PLCC	-3, -5, -7
	44-pin TQFP	-3, -5, -7
	48-pin TQFP	-3, -5, -7
	49-pin Ultra FineLine BGA *(1)*	-3, -5, -7
EPM7064B	44-pin PLCC	-3, -5, -7
	44-pin TQFP	-3, -5, -7
	48-pin TQFP	-3, -5, -7
	49-pin Ultra FineLine BGA	-3, -5, -7
	100-pin TQFP	-3, -5, -7
	100-pin FineLine BGA	-3, -5, -7
EPM7128B	49-pin Ultra FineLine BGA	-4, -7, -10
	100-pin TQFP	-4, -7, -10
	100-pin FineLine BGA	-4, -7, -10
	144-pin TQFP	-4, -7, -10
	169-pin Ultra FineLine BGA	-4, -7, -10
	256-pin FineLine BGA	-4, -7, -10
EPM7256B	100-pin TQFP	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	169-pin Ultra FineLine BGA	-5, -7, -10
	208-pin PQFP	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7512B	100-pin TQFP	-5, -6, -7, -10
	144-pin TQFP	-5, -6, -7, -10
	169-pin Ultra FineLine BGA	-5, -6, -7, -10
	208-pin PQFP	-5, -6, -7, -10
	256-pin BGA	-5, -6, -7, -10
	256-pin FineLine BGA	-5, -6, -7, -10

Note:
(1) Ultra FineLine BGA packages are Altera's 0.8-mm pitch BGA packages.

MAX 7000S Family

5.0-V MAX 7000S devices offer features such as 5-ns speed grades, in-system programming, an open-drain output option, and IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry in devices with 128 or more macrocells. All MAX 7000S devices are available in industrial-temperature grades. Table 8 shows the packages and speed grades available in the commercial-temperature grade.

Table 8. Commercial-Temperature MAX 7000S Devices

Device	Package	Speed Grade
EPM7032S	44-pin PLCC	-5, -6, -7, -10
	44-pin TQFP	-5, -6, -7, -10
EPM7064S	44-pin PLCC	-5, -6, -7, -10
	44-pin TQFP	-5, -6, -7, -10
	84-pin PLCC	-5, -6, -7, -10
	100-pin TQFP	-5, -6, -7, -10
EPM7128S	84-pin PLCC	-6, -7, -10, -15
	100-pin TQFP	-6, -7, -10, -15
	100-pin PQFP	-6, -7, -10, -15
	160-pin PQFP	-6, -7, -10, -15
EPM7160S	84-pin PLCC	-6, -7, -10
	100-pin TQFP	-6, -7, -10
	160-pin PQFP	-6, -7, -10
EPM7192S	160-pin PQFP	-7, -10, -15
EPM7256S	208-pin PQFP	-7, -10, -15

MAX 3000A Devices

MAX 3000A devices are the ideal low-cost ISP solution for designers looking for high performance at a low price-per-macrocell cost. 3.3-V product-term-based MAX 3000A devices are targeted for high-volume, low-cost designs. These devices have an enhanced ISP feature set and range in density from 32 to 256 macrocells (see Table 9) with propagation delays as fast as 4.5 ns.

Table 9. MAX 3000A Devices

Device	Package	Speed Grade
EPM3032A	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
EPM3064A	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
	100-pin TQFP	-4, -7, -10
EPM3128A	100-pin TQFP	-5, -7, -10
	144-pin PQFP	-5, -7, -10
EPM3256A	144-pin TQFP	-6, -7, -10
	208-pin PQFP	-6, -7, -10

CONFIGURATION

4-Mbit Configuration Device Coming Soon

The new 4-Mbit EPC4E configuration device is scheduled for release in the third quarter of 2000. This device will be offered in a 44-pin and 100-pin TQFP packages as well as a 0.8-mm, 144-pin Ultra FineLine BGA package. A new 9-Mbit EPC9E configuration device is also being developed and is slated for release in the third quarter of 2000. A single EPC4E device will configure a 400,000-gate EP20K400E device, and a single EPC9E device will configure a 1-million-gate EP20K1000E device.

These new devices will include features such as faster configuration times and parallel configuration. Additionally, you can use a single device to configure several APEX or FLEX devices in parallel to further speed configuration time.

TOOLS

Quartus Software Version 2000.05 Available Now

The Quartus software version 2000.05 is shipping to all customers with a current subscription in a single upgrade package that includes the MAX+PLUS II software version 9.6, Synopsys FPGA *Express*-Altera version 3.4 synthesis software, and Exemplar Logic LeonardoSpectrum-Altera version 1999.j synthesis software. Version 2000.05 of the Quartus software provides significant performance and fitting improvements for large designs. It also provides support for the device packages shown in Table 10 in addition to the device packages supported in version 2000.03.

Quartus Operating System Update

The Quartus software version 2000.05 supports the operating systems listed in Table 11.

Support for the Windows 2000 and the HP-UX 11.0 operating systems will be added later this year.

continued on page 12

Devices & Tools, continued from page 11

The MAX+PLUS II software version 9.6 is shipping to all customers with current subscriptions and features support for the new ACEX 1K device family.

Table 10. New Devices Supported by Quartus Version 2000.05

Support	Device	Package
Full Compilation, Simulation and Programming Support	EP20K100	356-pin BGA
	EP20K100E	324-pin FineLine BGA
	EP20K200 (1)	356-pin BGA
	EP20K200E	652-pin BGA, 672-pin FineLine BGA
	EP20K300E (1)	240-pin PQFP, 652-pin BGA, 672-pin FineLine BGA
	EP10K600E (1)	672-pin FineLine BGA
	EP20K1000E	652-pin BGA
Compilation, Simulation, and Pin-Out Support Only	EP20K160E (1)	144-pin TQFP, 208-pin PQFP, 240-pin PQFP, 356-pin BGA, 484-pin FineLine BGA
	EP20K1500E (1)	652-pin BGA, 1,020-pin FineLine BGA

Note:
(1) The Quartus software version 2000.05 supports these devices with and without PLLs.

Table 11. Quartus Operating System Support

Platform	Operating System
PC	Windows 98, Windows NT
UNIX	Solaris 2.6, HP-UX 10.20

MAX+PLUS II Software Version 9.6 Now Shipping

The MAX+PLUS II software version 9.6 is shipping to all customers with current subscriptions and features support for the new ACEX 1K device family. The ACEX 1K family is Altera's new mid-range density, look-up table (LUT)-based PLD family offering the low cost and high performance necessary for price-sensitive communications applications. For a complete list of new device support in the MAX+PLUS II software version 9.6, see Table 12.

MAX+PLUS II Version 9.62 is Now Available on the Altera Web Site

The MAX+PLUS II software version 9.62 update for the PC platform adds full support and advanced pin-out support for the devices listed in Table 13. This update also includes several software improvements to the Quartus fitter, timing model changes, and EPM7128B and EPM7256B device programming. This software update is available by opening the Software Tools menu on the left of the Altera web site and selecting MAX+PLUS II Updates.

If you are using the MAX+PLUS II BASELINE or E+MAX™ development system, you can eleminate problems by using version 9.62 of the MAX+PLUS II BASELINE and E+MAX software, which are now available.

Table 12. New Devices Supported by MAX+PLUS II Version 9.6

Support	Device	Package
Full Compilation, Simulation and Programming Support	EPM7128B	100-pin FineLine BGA, 256-pin FineLine BGA
	EPM7256B	100-pin TQFP, 144-pin TQFP, 208-pin PQFP, 256-pin FineLine BGA
	EP1K30	144-pin TQFP, 208-pin PQFP, 256-pin FineLine BGA
	EP1K50	144-pin TQFP, 208-pin PQFP, 256–pin FineLine BGA, 484-pin FineLine BGA
	EP1K100	208-pin PQFP, 256-pin FineLine BGA, 484-pin FineLine BGA
Compilation, Simulation, and Pin-Out Support Only	EPM7128B	49-pin Ultra FineLine BGA, 169-pin Ultra FineLine BGA
	EPM7256B	169-pin Ultra FineLine BGA
	EPM7512B	169-pin Ultra FineLine BGA
	EPM7064AE	49-pin Ultra FineLine BGA
	EPM7128AE	169-pin Ultra FineLine BGA

Table 13. Additional Devices Supported in MAX+PLUS II Version 9.62

Support	Device
Full Support	EPM7128BFC256, EPM7256BFC256, EPM7512BQC208
Advanced Pin-Out Support	EP1K10TC100, EP1K10TC144, EP1K10QC208, EP1K10FC256, EPM7032BUC49, EPM7064BUC49

Renewal Price Promotion for Customers on Active Subscription

For a limited time, all Altera customers with current subscriptions will receive a 10% discount off of the renewal subscription list price as long as the renewal subscription is ordered before their current subscription expires. This offer is valid to all customers on active subscription. The renewal ordering code can be used to renew FIXEDPC, FLOATPC, or FLOATNET subscriptions.

The 10% discount applies to orders received on or before the subscription expiration date. A renewal subscription extends the subscription by 12 months from the existing expiration date. Customers do not lose any months on their existing subscription by renewing early.

You will receive updates for both the Quartus and MAX+PLUS II software for an additional 12 months after your current subscription was set to expire. You also receive world-class synthesis and simulation software with the renewal of your subscription. For synthesis, Synopsys FPGA *Express*-Altera and Exemplar Logic LeonardoSpectrum-Altera is included with your renewal. You will also receive Model Technology Model*Sim*-Altera for behavioral HDL simulation and test bench support. By renewing a subscription before it expires, you are guaranteed to receive the latest version of the Quartus and MAX+PLUS II software without interruption and gain access to world class synthesis and simulation software.

License Files for OEM World-Class Synthesis & Simulation Tools Available Today

Altera has entered into OEM agreements with Synopsys and Mentor Graphics to provide Altera customers with world-class synthesis and simulation products. Altera is shipping the Synopsys FPGA *Express* version 3.4 and Exemplar Logic LeonardoSpectrum Level 1 version 1999.1j synthesis software to all customers with current subscriptions. Model Technology Model*Sim*-Altera simulation software will be shipping to customers shortly.

Visit the Altera web site to request a license file to enable any or all of the OEM software tools. A license file will be e-mailed directly to you to enable these synthesis and simulation capabilities for use with the Altera software. FPGA *Express* is only available for the PC platform, working with FIXEDPC and FLOATPC products. The LeonardoSpectrum and Model*Sim* software for Altera are available for PCs and UNIX workstations in fixed or floating configurations.

Synopsys FPGA *Express* for Altera supports mixed-HDL synthesis for VHDL and Verilog designs. The feature set of the FPGA *Express* software that Altera ships is identical to the standard FPGA *Express* software. However, FPGA *Express* software only targets Altera devices.

For LeonardoSpectrum license files, you can request either VHDL or Verilog support for each Altera subscription, but not both—you can only have support for one HDL per Altera subscription. The LeonardoSpectrum Level 1 for Altera and Level 2 software tools do not support mixed-HDL synthesis. The LeonardoSpectrum Level 1 synthesis tool provided by Altera includes all the features of the LeonardoSpectrum Level 2 configuration, but only allows designers to target Altera devices.

Altera has entered into OEM agreements with Synopsys and Mentor Graphics to provide Altera customers with world-class synthesis and simulation products.

The Model*Sim*-Altera simulation software consists of the Model*Sim* PE GUI features including the standard HDL debugging environment and Tcl scripting capability supporting Altera libraries for gate-level simulation. You can request either VHDL or Verilog HDL support within the ModelSim software for each Altera subscription, but not both. The Model*Sim*-Altera software tools do not support mixed-HDL simulation.

You can indefinitely use versions of the Synopsys FPGA *Express* software for Altera received during your active subscription. However, you cannot enable versions of FPGA *Express* released after your subscription expires. This is identical to the licensing for the Quartus and MAX+PLUS II software.

License files for Exemplar Logic LeonardoSpectrum and Model Technology Model*Sim* software provided by Altera are set to expire 15 months from the date of the license request. These products will no longer operate after expiration. However, you can request a new license and extend the expiration for another 15 months as long as your subscription remains active.

Improving Quartus Design Performance

The Quartus™ software version 2000.02 and higher introduces new and improved timing-driven compilation algorithms for core and I/O performance as well as more capability for cliques. In most cases, push-button performance in the Quartus software can achieve desired requirements for core f_{MAX} and I/O timing. Many additional techniques can be used to achieve even better performance in APEX™ designs with the Quartus software, including:

- Timing-driven compilation
- Cliques and other logic options
- Back-annotation and manual placement

Timing-Driven Compilation

The Quartus software is very flexible, and offers a large number of options that can be set within. You can set a global timing-driven compilation target for the entire design, or several timing-driven compilation target settings, one for each individual clock domain (if several exist in the design). Individual clock settings usually provide better f_{MAX} results (and are required for multiple clock domain analysis and hold-time validation). For optimal results, experiment with both global and individual settings.

In the Quartus software version 2000.02 and higher, you can either select **Normal compilation** or **Extra effort**. The **Extra effort** setting usually provides better f_{MAX} results, but may increase compile times (up to 2×). In either case, you should set the target f_{MAX} about 10% higher than required and vary the target until you find the best results. If you set the target too high, though, you may over-constrain the Quartus software, producing slower results.

Cliques and Other Logic Options

You can use options and settings in the Quartus software to improve results, including cliques, the **Speed vs. Area** setting, and the **Auto-Global Memory Control Signals** setting.

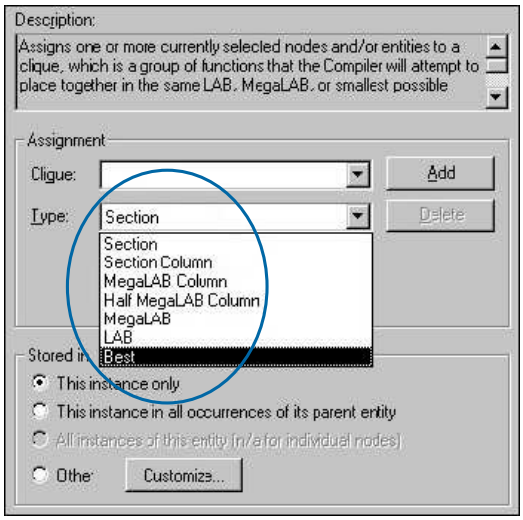
Cliques

Version 2000.02 and higher of the Quartus software provides cliques of different target sizes, controlling how tightly you pack the logic. Target areas can be as small as a logic array block (LAB) or up to half of the device.

You can use cliques with timing-driven compilation on or off. Altera recommends that you enable timing-driven compilation with hierarchical-based cliques based on your knowledge of your design. All cliques (except Best cliques, see Figure 1) are considered hard assignments that may create complications if they cannot be met. You may get a no-fit result if too much logic is placed into too small an area (i.e., placing 12 logic cells into one LAB). If you are unsure of the size of cliqued logic, use the Best clique type, which allows the Quartus software to modify the size of the clique target as needed.

After the initial compilation results with timing-driven compilation and hierarchical cliques, you

Figure 1. Clique Selection in Assignment Organizer



can analyze critical paths, determine logic common between multiple critical paths, and apply a clique to place logic cells closer together (see Figure 2).

You should add cliques only when your design performance is much slower than what is required; avoid assigning logic haphazardly into cliques without verifying that logic cells are not placed into multiple cliques of the same size. This can add more logic into the original clique size, which may result in a no-fit.

Settings

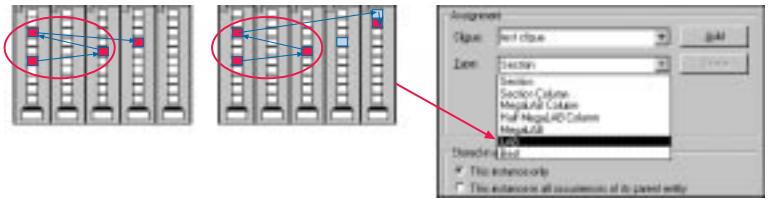
The settings you make affect the performance results in the Quartus software. Two significant settings are:

- **Speed vs. Area:** You can set the **Optimization Technique** option in the **Option & Parameter Settings** (Project menu) to either **Speed** to optimize the design for performance (tight routing, redundant logic for fanout) or **Area** to optimize device space (loose routing, minimal/optimized logic). You can use this option for all HDL files, although it is most effective on Altera Hardware Description Language (AHDL) Text Design Files (**.tdf**) and Block Design Files (**.bdf**). You should synthesize Verilog HDL and VHDL designs with other third-party EDA synthesis tools.
- **Auto-Global Memory Control Signals:** You may improve your design's performance by turning this setting off. This setting is enabled by default and instructs the Quartus software to use global-control interconnect lines whenever possible for memory control signals. However, this may slow memory performance if internally-generated control signals are not able to drive memory blocks directly without using the global control lines. Extra delay is incurred when routing onto global control lines prior to the memory blocks.

Back-Annotation & Manual Placement

Your timing-driven compilation targets, cliques, and options and settings may bring your design performance close to required specifications, but they may not be enough. You can then back-annotate the design results and placement,

Figure 2. Cliquing Common Logic Cells



manually moving logic yourself to speed up your design. Back-annotation can be very powerful because it:

- Allows you to maintain fitting results from one version of the Quartus software to other versions of the Quartus software, either older or newer
- Can improve fitting time (from hours down to minutes), since the Quartus software devotes less time with logic placement
- Locks down specific parts of the design, maintaining speed in those portions of the design

One drawback is that if the design changes significantly, some or most of the back-annotated assignments may be lost due to re-synthesis and renaming of node names.

The following indicators can help you determine if you should back-annotate your design:

- Is the design stable (will there be any more code changes)?
- Path dependencies: Is there logic common to multiple critical paths?
- Are there only a few paths that do not meet performance goals?
- Are compile times long?

If you back-annotate your design, you should consider several guidelines. In well-utilized designs (60% or higher), you should back-annotate to logic array blocks (LABs) instead of logic cells to ensure second-time fitting after logic is rearranged. You may have to demote assignments to MegaLAB™ blocks. Here are additional guidelines:

- Always ignore or disable cliques if you back-annotate your design; these new assignments will override the cliques.

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Design Tips: Improving Quartus Design Performance, continued from page 15

- Archive or back-up project files from your best compilation to date. If the next round of changes are slower than your best f_{MAX} results, you should revert back to the files from your best compilation. This is easily done if you archived the files.

The goal is to minimize the amount of interconnect delays used in the path (see Figure 3), hence consolidating logic as much as possible. Determine where critical paths cross LAB or MegaLAB boundaries. Logic cells should always be moved into LAB or MegaLAB bins, instead of specific logic cell locations. The Quartus software determines legal placement and routing for you.

Figure 3. Making LAB-Based Location Assignments

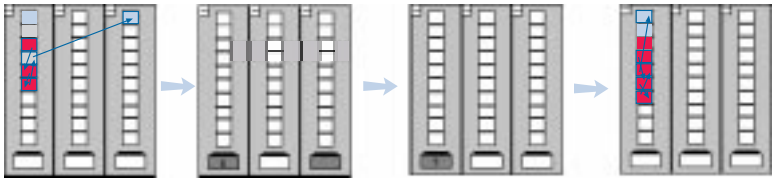


Figure 4. Increasing Path A Delay Helps Path B Timing

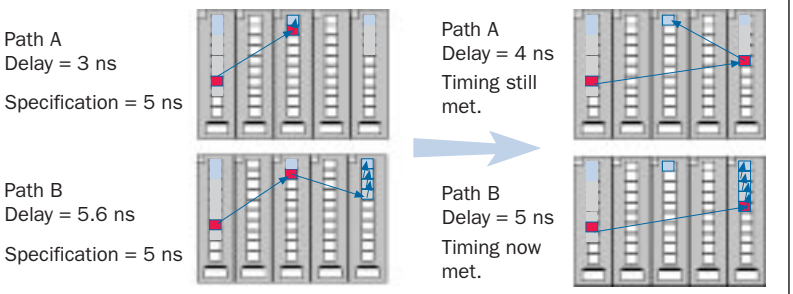
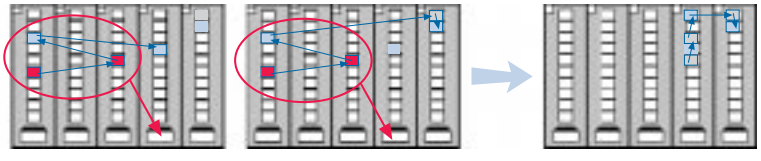


Figure 5. Assigning Common Logic Cells to LABs



To determine which cells to move, look at the cells that have the smallest fan-in and fan-out. These are the cells that will likely have the least impact to other potentially critical paths. You should avoid making other critical paths worse when moving logic cells to fix another critical path. However, in some cases, increasing the delay of some paths when fixing other critical paths can be a good tradeoff if the slowed paths are not critical. Short paths (i.e., back-to-back registers) with plenty of margin can be good candidates to balance delay (see Figure 4).

Logic common in multiple critical paths can also be resolved with manual placement. Create an efficient layout by moving logic cells that appear in several paths (e.g., control signals such as enables, address decoders, and other high fanout situations). See Figure 5. By fixing one path, you can fix several others.

Critical paths should cross MegaLAB columns as infrequently as possible (avoid using row-interconnect lines). When using the MAX+PLUS® II software for FLEX® designs, you can improve performance when you keep paths on the same row. However, this does not hold true for APEX designs and the Quartus software. Essentially, MegaLAB blocks and MegaLAB columns in APEX devices are equivalent to LABs and rows of LABs in FLEX devices. This also applies when you clique large blocks of logic together.

Summary

The Quartus software version 2000.02 and higher comes equipped to allow you to achieve performance goals in various ways. If you cannot meet performance with push-button timing-driven compilation operation, a combination of cliques, settings, back-annotation, and manual placement can often get the extra performance necessary in APEX designs. It is important to realize that there is no one "best" method to achieve performance in the Quartus software. The options that work best vary by design, but the steps outlined in this article should help improve your performance.

Sign Up Now for Free Excalibur Workshops

Intensive three-hour workshops, starting in June, will teach you how to implement the Nios™ family of soft core embedded processors in APEX™ devices. These hands-on workshops will allow you to work with the Excalibur™ Development Kit, from creating a design and running it on a development board to tracking down and correcting design errors. You will also learn about the GNUPro® compiler and debugger from Cygnus®, a Red Hat® company, which is included in the Excalibur Development Kit. Visit **http://www.altera.com/workshop** to reserve your space at a North American workshops. To sign up for free workshops outside North America, contact your local Altera representative.

North America

Arizona
- Phoenix — July 14

California
- Santa Clara — June 28
- Santa Clara — June 29
- San Diego — July 11
- Irvine — July 12
- Woodland Hills — July 13

Colorado
- Broomfield — August 25

Florida
- Tampa — July 27

Georgia
- Norcross — July 25

Illinois
- Arlington Heights — August 7
- Lisle — August 8

Maryland
- Gaithersburg — August 18

Massachusetts
- Westford — August 15

Michigan
- Livonia — August 10

Minnesota
- Minneapolis — August 9

New Jersey
- Long Branch — August 16
- Cherry Hill — August 17

New York
- Rochester — July 21

North Carolina
- Reasearch Triangle Park — July 28

Ohio
- Fairborn — August 11

Ontario, Canada
- Kanata — July 18
- Mississauga — July 19

Oregon
- Beaverton — August 29

Texas
- Richardson — August 22
- Austin — August 23

Utah
- Salt Lake City — August 31

Washington
- Bellvue — August 30

Europe

England
- London — September 12

France
- Paris — September 22

Germany
- Munich — September 15

Israel
- Tel Aviv — September 18

Italy
- Milan — September 20

Sweden
- Stockholm — September 13

Bridging the Gap: dataBLIZZARD & Reliaspan

Ultimate performance, high availability, and redundancy are three demanding requirements for the telecom industry as it heralds a new generation of communications interfaces. SBS Technologies Connectivity Products has addressed these demands with two breakthrough product lines: the dataBLIZZARD™ and Reliaspan products.

The dataBLIZZARD product family includes PCI, PCI mezzanine card (PMC), and CompactPCI formats, which will be used in medical imaging, telecommunications, and other industrial applications.

The dataBLIZZARD software is the ultimate-performance, point-to-point communications interface that enables two computers to share data at the hardware level with little or no software overhead (see Figure 1). The dataBLIZZARD peripheral component interconnect (PCI) interface that supports data sharing is flexible, providing the highest performance allowed by the PCI bus. The integrated direct memory access (DMA) engine can transfer data between systems at sustained transfer rates of 80 megabytes per second. Programmed I/O processes can be completed over the link in less than 2 µs, and data can be transferred up to 500 meters over dataBLIZZARD's gigabit fiber-optic transceivers. The dataBLIZZARD product family includes PCI, PCI mezzanine card (PMC), and CompactPCI formats, which will be used in medical imaging, telecommunications, and other industrial applications.

Reliaspan, SBS' exceptionally fast, high-throughput 64-bit expansion systems for PCI and CompactPCI computers, is designed to provide servers with I/O expansion capabilities through the addition of seven PCI or CompactPCI slots. With Reliaspan, a host server can be gracefully scaled to accommodate more PCI or CompactPCI slots, as they are needed. This is especially important for high-availability telecom and computer telephony applications that were once previously limited by the number of cards that the host could support.

Historically, SBS designed its own PCI bus interfaces, but for the dataBLIZZARD software and Reliaspan, SBS chose to move into the 64-bit, 66-MHz PCI realm via intellectual property (IP). Using a programmable logic device (PLD) with a PCI function, SBS entered the market quickly without losing design flexibility.

SBS thoroughly evaluated cores offered by six programmable logic vendors and applied the following criteria: performance, flexibility, stability features, documentation, and allowable design re-use. As a result of this evaluation, SBS selected the Altera® FLEX® 10K family to use in both the dataBLIZZARD and Reliaspan products over the six companies that had working 64-bit, 66-MHz PCI function designs. Only Altera could offer four or more base address registers—an essential feature that allowed SBS to maintain compatibility with the suite of software drivers written for earlier generation products.

William Molyneux, vice president of engineering, SBS Connectivity Products, stated that "Reliaspan and the dataBLIZZARD software represent significant breakthroughs for SBS. Both will be shipped in high volumes and will have very long product life cycles." Molyneux also affirmed that "Altera was the sole vendor with bridge experience using its core which substantially lowered our risk. Altera became more of a partner than a vendor. They made every effort to support our developments with their engineering resources."

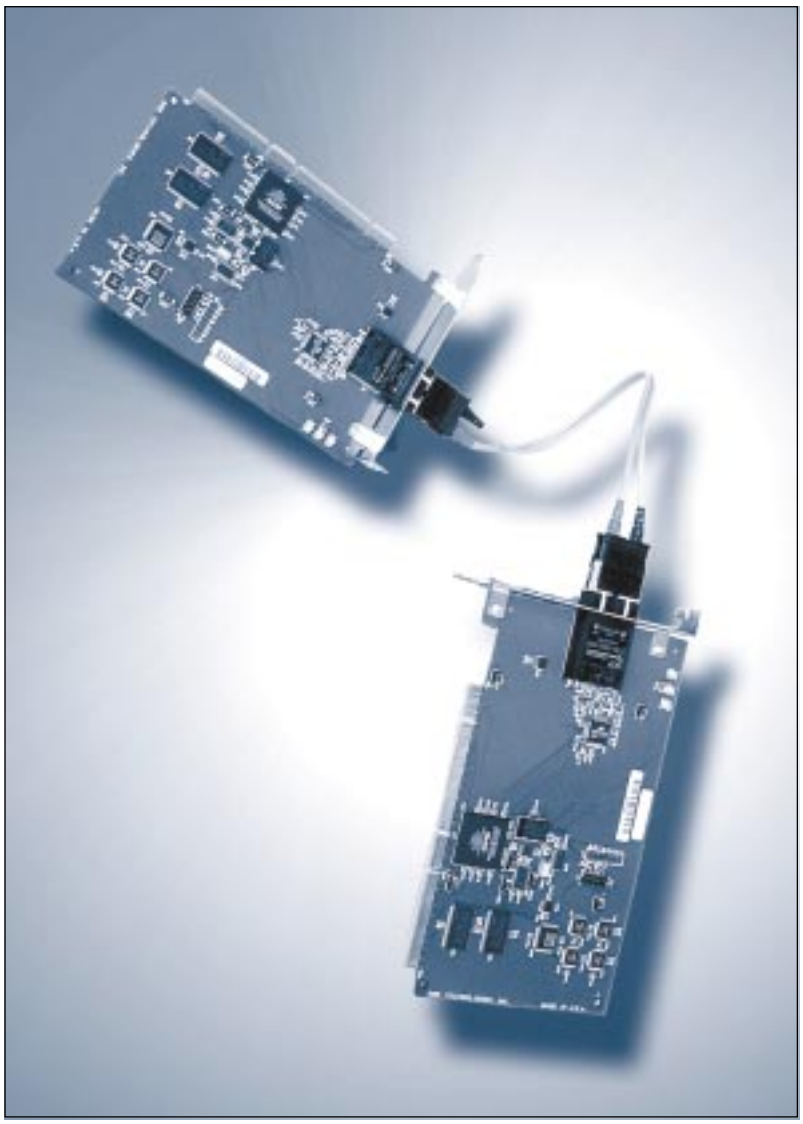
Reliaspan CompactPCI expansion systems were introduced at the Computer Telephony Exposition last March. The dataBLIZZARD family was introduced at Intel's Applied Computing Show at the end of May. Both the dataBLIZZARD software and Reliaspan have already been designed into several major OEM projects.

SBS Technologies, Inc., Connectivity Products is the premier provider of high-performance and reliable bus connectivity products that include bus bridges and bus expansion units that are designed to operate in the most demanding applications.

SBS Technologies, Inc. is a leading manufacturer of standard bus embedded computer components for VME, CompactPCI, embedded PCI and custom standalone applications. SBS product lines include CPU (Pentium and PowerPC) boards, input/output (I/O) modules, avionics modules and analyzers, bus interconnection products, expansion units, real-time networks, telemetry boards, data acquisition software, DIN-rail embedded PCs, and industrial-grade computers. SBS Technologies' embedded computer components are used in a variety of applications, such as communications, medical imaging, industrial control and flight instrumentation in the commercial and aerospace markets.

SBS Connectivity Products
1284 Corporate Center Drive
St. Paul, MN 55121-1245
(651)905-4700
http://www.sbs-cp.com

Figure 1. The dataBLIZZARD Connection



Nios Architecture & Customization

Inside the Nios Embedded Processor

As the first RISC processors developed specifically for programmable logic, the Nios™ family of soft core embedded processors contains many configurable elements to meet a wide range of needs. The block diagram in Figure 1 shows the basic elements of the Nios embedded processor. You can configure the address and data bus widths to a maximum of 32 bits. The register file, stored in embedded system blocks (ESBs), can be up to 512 words deep with a 32-bit viewable window. The Nios interrupt controller supports up to 64 internal or external sources.

Using Nios Peripherals

The Excalibur™ Development Kit, featuring the Nios embedded processor, includes several peripherals for the Nios family, including a universal asynchronous receiver/transmitter (UART), a counter/timer, memory controllers, and a parallel I/O (PIO) connection. Other peripherals, such as an SDRAM controller, SPI, PWM, 10/100 Ethernet MAC, and IDE disk controller will be released later this year. The MegaWizard® Plug-In Manager, also included, lets you connect and configure your Nios peripherals to the Nios embedded processor. Wait states, interrupt control, variable bus sizers, and address decoding are all automatically generated by the MegaWizard Plug-In Manager within the peripheral bus module (PBM), shown in Figure 2. For example, you can use the MegaWizard Plug-In Manager to specify which peripherals interrupt the Nios embedded processor; for each peripheral that does, the MegaWizard Plug-In Manager automatically assigns an address in the interrupt look-up table (LUT) and generates the corresponding interrupt control logic. You can also choose the number of wait states each peripheral needs, or allow the peripheral to generate its own wait signal for the Nios embedded processor; in either case, the MegaWizard Plug-In Manager designs the wait state generator accordingly. The MegaWizard Plug-In Manager uses bus size converters to adapt 32-bit peripherals to Nios 16-bit configurations as needed. Finally, the MegaWizard Plug-In Manager creates address decoding within the PBM to generate the necessary chip selects.

In addition to generating the PBM, the MegaWizard Plug-In Manager also defines the connection between the Nios embedded processor and the PBM, and between the PBM and the peripherals. The MegaWizard Plug-In Manager outputs a set of Verilog HDL files containing the connectivity, PBM, and Nios design that can be easily integrated into any APEX™ 20K device through the Quartus™ software.

Figure 1. Nios Block Diagram

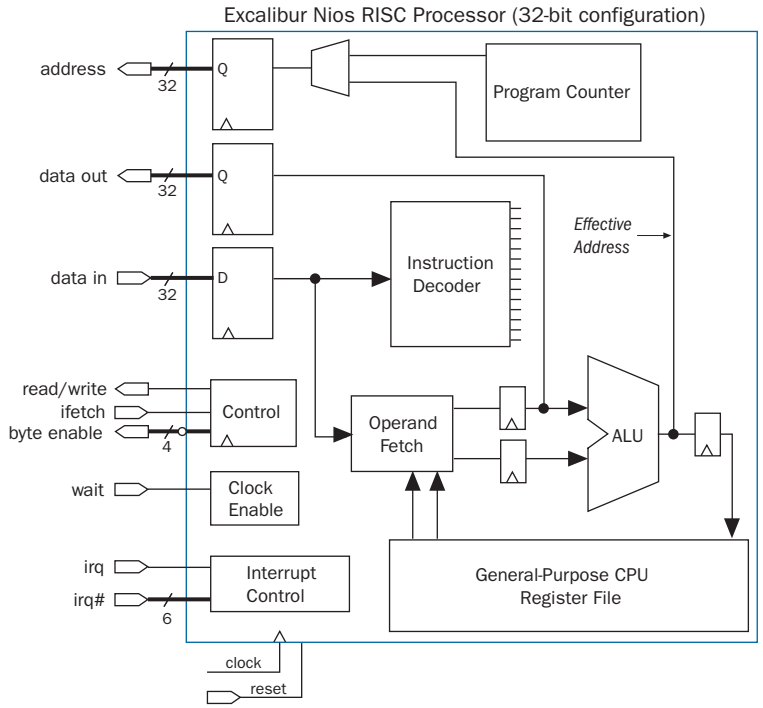
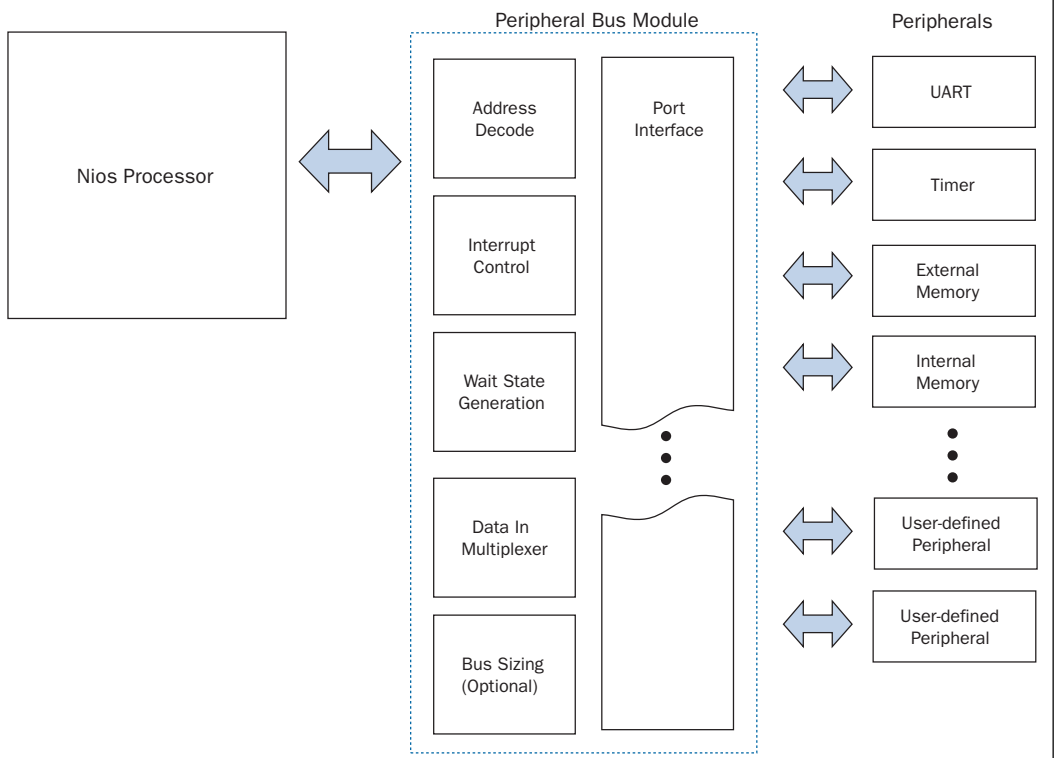


Figure 2. Nios Embedded Processor & PBM



Nios™

Customizing the Nios Embedded Processor

In addition to customization via its user-selectable parameters, you can design other peripherals to supplement the Nios embedded processor. These peripherals can be anything supported by APEX device resources, including custom memory controllers, DSP functions such as filters and FFTs, encoders/decoders, proprietary interfaces, etc. User-defined peripherals are handled the same way as Altera peripherals; you can assign interrupts and wait states using the MegaWizard Plug-In Manager, which automatically generates the necessary logic and connectivity files (users also have the choice of creating their own connections).

Current Software Versions

The Quartus™ software version 2000.05 is the latest release, and is available for the following operating systems:

- Microsoft Windows 98
- Microsoft Windows NT
- Sun Solaris version 2.6
- HP-UX version 10.20 and higher; however, HP-UX version 11.0 and higher are not yet supported

The MAX+PLUS® II software version 9.6 is available for the following operating systems:

- Microsoft Windows 95 and Windows 98
- Microsoft Windows NT version 3.51 and higher
- Sun Solaris version 2.5 and higher
- HP-UX version 10.20 and higher; however, HP-UX version 11.0 and higher are not yet supported
- AIX version 4.1 and higher

Sucessful In-System Programming Implementation

Altera supports the Jam™ Standard Test and Programming Language (STAPL) format, which allows you to program IEEE 1149.1 Joint Test Action Group (JTAG)-compliant devices independent of platform and vendor. In-system programmability (ISP) is accomplished through the 4-wire JTAG interface. In addition, Jam STAPL simplifies software support by allowing you to run the programming software in any environment: in a PC or workstation, over a network, or in an embedded environment.

To use ISP successfully, you must plan the following areas of product development:

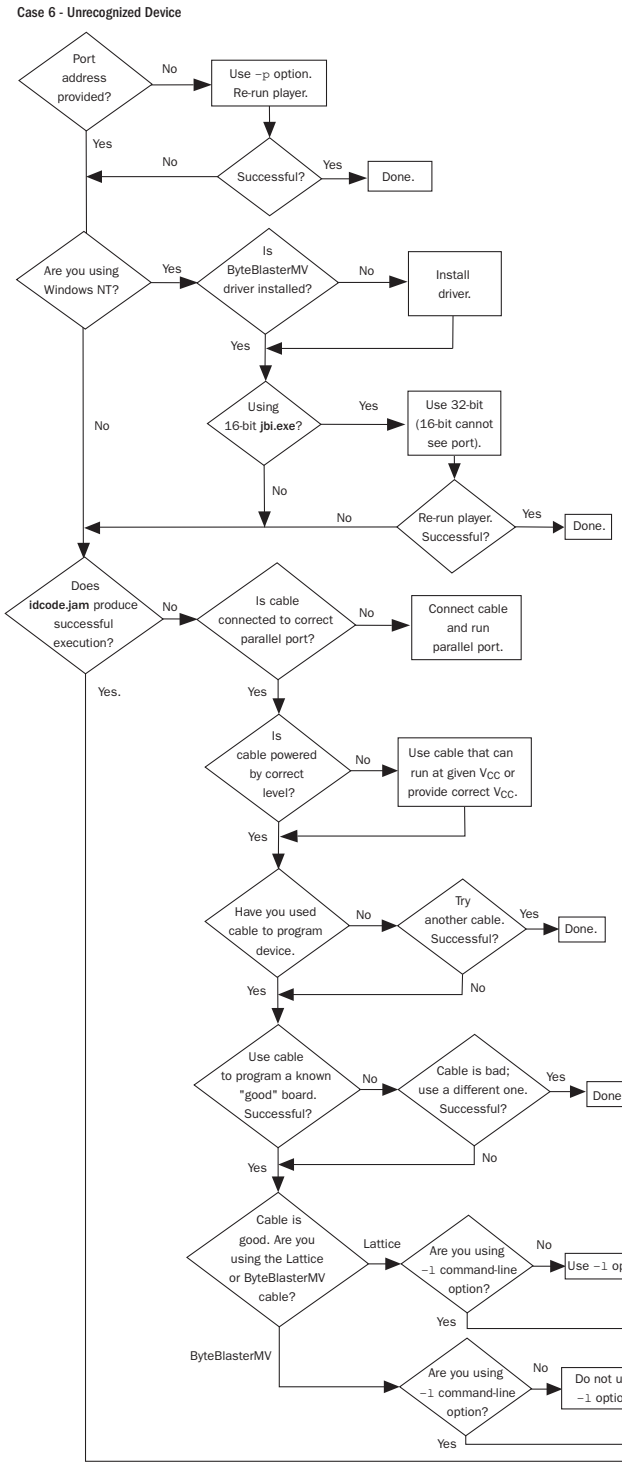
- Board Layout—connecting the JTAG chain. Treat `TCK` as a clock trace, a task often overlooked in embedded systems where `TCK` originates at a processor's general I/O pin. Lack of signal integrity on this trace is often the source of programming errors.
- Embedded Memory Requirement—for in-field upgrades. In an embedded environment, the Jam STAPL Byte-Code software requires memory to program the devices in the JTAG chain. It is important to consider this requirement before choosing memory and processors used for the in-field upgrade.

For more information on these topics see *Application Note 100 (In-System Programmability Guidelines)*, and *Application Note 122 (Using Jam STAPL for Embedded ISP & ICR)*.

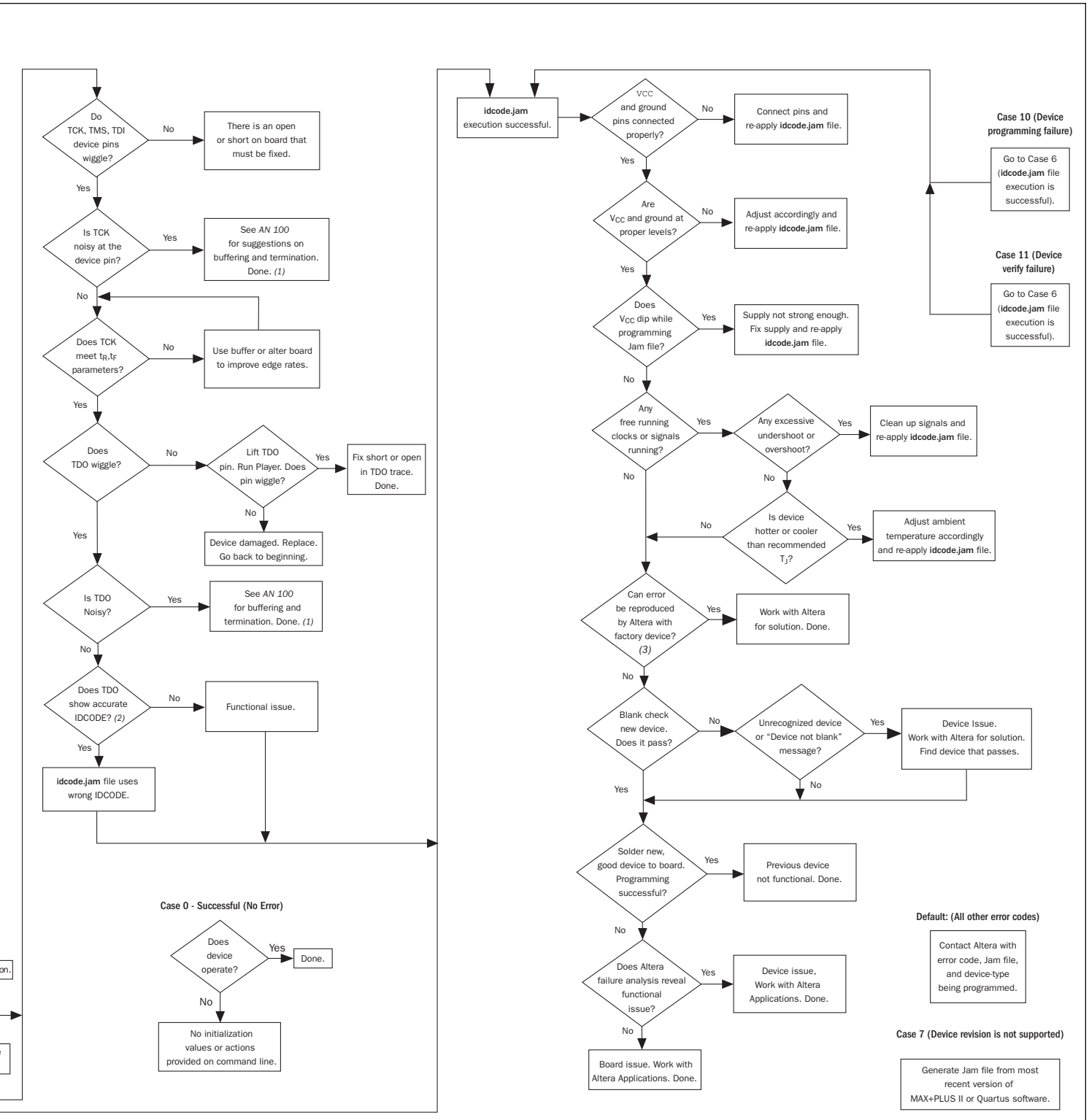
Following the steps listed in *Application Note 100* and *Application Note 122*, ISP can reduce your costs and improve product quality. If you encounter an error during programming, the flow chart shown in Figure 1 will help you determine the source of the problem.

In addition, you can download the **idcode.jam** Jam STAPL file from the Altera® FTP site: **ftp:\\ftp.altera.com\pub\misc**. Use this file to read the JTAG IDCODE out of Altera devices. If you cannot read the IDCODE, then you have a signal integrity or JTAG connectivity issue. See the flow chart in Figure 1 to determine where the problem is.

Figure 1. Jam Error Flow Chart



Notes: (1) *Application Note 100 (In-System Programmability Guidelines)*

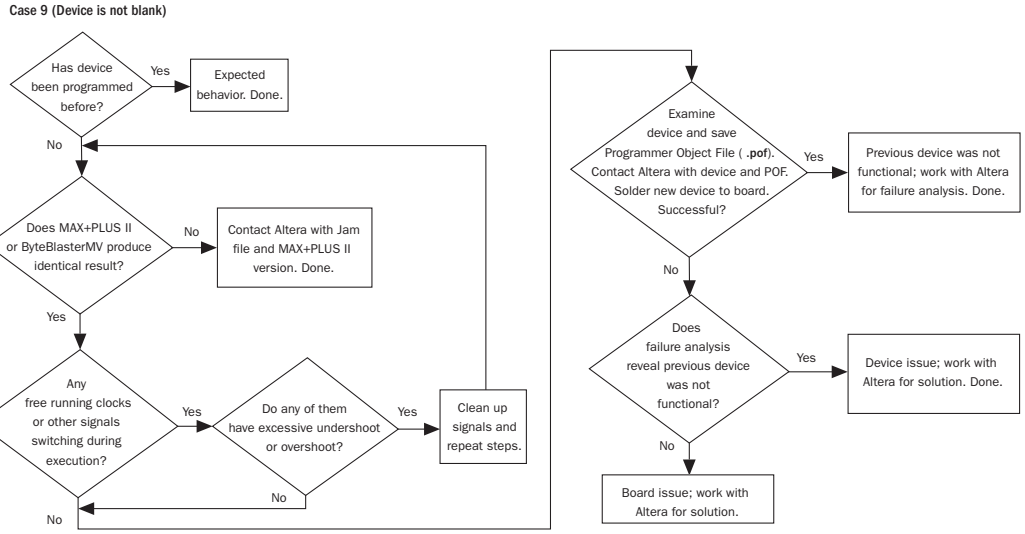


(2) See device data sheet for IDCODEs. (3) Work with local FAE or contact Altera Applications (800) 800-3753

continued on page 24

Sucessful In-System Programming Implementation, continued from page 23

Figure 1. Jam Error Flow Chart (continued)



Altera *News*

ACEX Devices Address Communications Market Need for Low-Cost Programmable Logic

The communications marketplace is experiencing rapid and dynamic growth. Increased pressures for flexibility and fast time-to-market are brought about by shortened design cycles and continually evolving standards. Programmable logic is a key to achieving a successful solution in this rapidly changing marketplace. However, for high-volume applications, the need for cost-efficiency historically restricted the use of programmable logic devices (PLDs).

Now, low-cost communications applications eagerly awaiting the programmable advantage have an attractively priced solution.

Altera has eliminated this cost barrier with the new ACEX™ device family. Now, low-cost communications applications eagerly awaiting the programmable advantage have an attractively priced solution. Furthermore, ACEX devices can meet the requirements inherent to communications systems without sacrificing performance. ACEX devices provide a low-cost, high-performance solution, ideal for ASIC and application-specific standard product (ASSP) replacement in the communications marketplace.

ACEX Applications

The need for a high-volume, low-cost programmable solution in the communications marketplace is skyrocketing as price-sensitive applications abound due to the explosive growth in the networking and telecommunications sectors. xDSL and cable modem growth rates are tremendous due to the expansion of Internet traffic, and Dataquest projections expect these modem growths to reach as high as 141% compounded annual growth rate (CAGR). ACEX devices fit perfectly into these applications, replacing blocks such as protocol and transceiver modules, which are currently implemented via ASICs or ASSPs. Remote access concentrators and access routers provide another example of the enormous potential for ACEX devices, as demand for high-speed

communication channels to satellite offices grows. Laser printers, PC peripherals, and low-cost switches provide just a few more examples of the many applications in the communications marketplace that benefit from ACEX devices.

ACEX device pricing is competitive with ASICs, freeing designers from expensive and time-consuming ASIC implementation. Additionally, all the typical benefits of PLDs over ASICs still apply, including fast time-to-market, flexibility in design and reprogrammability, advanced PLD development tools, and drop-in intellectual property (IP). ACEX devices also eliminate non-recoverable engineering (NRE) costs, the risk associated with ASIC re-spins, errors, and design changes, and time associated with the ASIC conversion process. Due to the advanced and versatile nature of the ACEX feature set, ACEX devices also eliminate specialized and inflexible ASSP implementations of design elements. You can integrate discrete phase-locked loops (PLLs), first-in first-out (FIFO) circuitry, RAM, and peripheral component interconnect (PCI) or other advanced bus interface standard interfaces within an ACEX device.

ACEX Device Families

The ACEX device families are broad-based, intended to provide programmable solutions across platforms and generations. An ongoing line of ACEX families will be introduced, beginning with the 2.5-V ACEX 1K family that is now shipping, and continuing with the 1.8-V ACEX 2K family to be released later this year. ACEX families will span a variety of processes and operating voltages, and smaller process geometries will increase performance while decreasing cost and power consumption. Future ACEX families will continue to make use of a variety of architectures and will have a range of different feature sets.

ACEX 1K Devices

The ACEX 1K family is currently available and represents the optimal union of price, performance, and features in this low-cost, 2.5-V device family. The key to the ACEX 1K device's low price is the advanced hybrid process, combining 0.22-µm transistors with 0.18-µm metal interconnect layers. This combination maintains the desired 2.5-V operating voltage while improving die size over standard 0.22-µm processes. This die size improvement provides a two-fold advantage: creating inherent cost improvements due to the large number of available die per wafer, and improving the yield at a constant defect density. In addition, the patented Altera redundancy feature ensures that even dies with impurities can be repaired and rendered fully functional, further improving yield numbers and reducing costs.

The four ACEX 1K devices range from 10,000 to 100,000 typical gates (56,000 to 257,000 maximum system gates) and deliver high performance, with typical system speeds exceeding 115 MHz. ACEX 1K devices are specifically designed to support 64-bit/66-MHz PCI compliance, ensuring compatibility with high-performance communications systems by using what has become the de facto bus standard for open systems and an emerging I/O standard for embedded applications. ACEX devices feature an embedded PLL that can simultaneously generate ClockLock and ClockBoost modified clock signals to manage on-chip clock domains, improve device utilization, and improve board-level clock management as a whole. Embedded dual-port memory blocks provide a significant enhancement as well, ensuring fast and effective RAM, ROM, dual-port RAM, or FIFOs with tremendous ease of implementation.

EP1K30, EP1K50, and EP1K100 devices are all now shipping in a wide range of advanced packages, including thin-quad flat pack (TQFP) and FineLine BGA™ packaging. EP1K10 devices will ship in the third quarter of 2000 with volume pricing beginning as low as $3.50 per device.

ACEX 2K Devices

ACEX 2K devices will be available in the second half of 2000. These devices will be based upon an advanced 0.18-µm process and will make use of Altera's process technology leadership to ensure high production yields and low costs at a 1.8-V operating voltage. ACEX 2K devices will range from 20,000 to 150,000 gates (75,000 to 400,000 maximum system gates) and will incorporate additional advanced features such as advanced I/O standards and an enhanced-capability PLL.