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With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

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# PM5370 WSE 40

## SONET/SDH Wideband Cross-Connect



Released Product Brief

### Product Highlights

- Multi-purpose SONET/SDH VT/TU and SONET/SDH STS/STM cross-connect
- With a memory-switch architecture, implements a strictly non-blocking switch that supports a VT/TU level fabric of up to 45 Gbit/s
- Supports 18 high-speed Enhanced SONET Serial Interface (ESSI) CML links each independently configurable for STS-48/STM-16 at 2.488 Gbit/s or STS-12/STM-4 at 622.08 Mbit/s operation
- Supports system frame synchronization using an external frame pulse or ESSI smart frame synchronization using the frame boundary of the receive links
- Compensates for differences in frame boundary arrival times between ingress ports using FIFOs and device level software configurable delay registers
- Each SONET STS-1 or SDH VC3/VC4-TUG3 may be independently configured as a single unit and/or as a container of VT/TUs. The contents may be switched intact or switched as VT/TUs
- Allows each SONET VT Group to be independently configured to carry VT1.5, VT2, VT3, or VT6 tributaries
- Allows each SDH TUG2 to be independently configured to carry TU11, TU12, or TU2 tributaries
- Provides a device latency of 5.62 (+/-0.17)  $\mu$ s for 2.488 Gbit/s links and 6.21 (+/-0.67)  $\mu$ s for 622 Mbit/s links

### SONET/SDH Overhead Accessibility

- Supports extraction of the transport overhead (TOH) from the ingress ports (both high and low-speed) as well as the insertion of transport overhead into the egress ports via low bandwidth two-bit 77.76 MHz interfaces

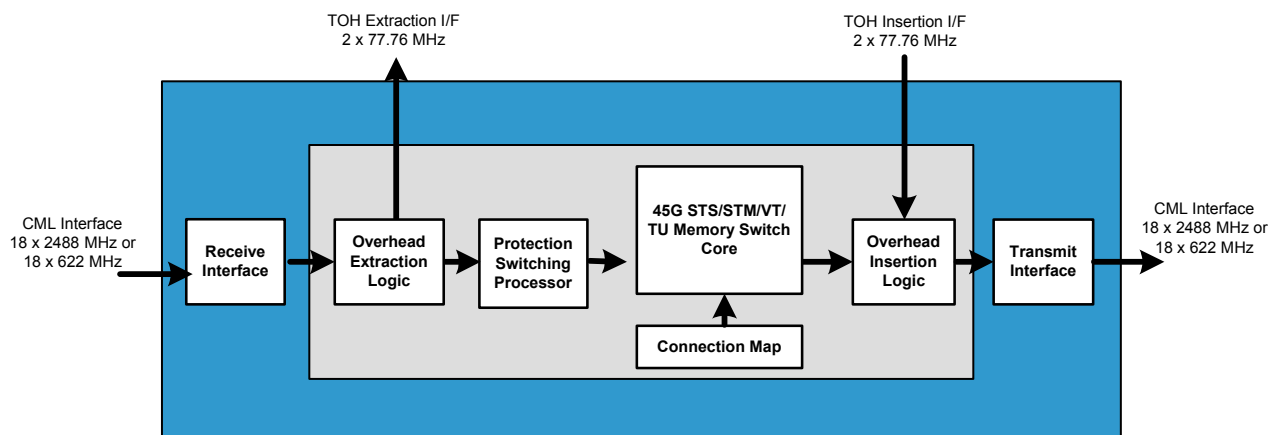
### APS Features

- Supports a hardware-based Automatic Protection Switching mechanism (MAPS) for centralized link protection control when operating with other PMC-Sierra devices such as the PM5369 TUPP 9953
- Provides fully automatic protection switching for Class 1 protection services including 1+1 protection, UPSR, SNCP, and static mesh protection services
- Provides hardware assists for Class 2 protection services including 1:N protection, BLSR-2/4, MSSPRING-2/4, and dynamic mesh protection schemes

### I/O and General

- All high-speed ingress and egress links are 1.2 V CML and are ELVDS-compatible with programmable pre-emphasis on transmit, equalization on receive, and support for both AC and DC coupled interfaces
- Each high-speed link supports SONET/SDH framed or unframed PRBS-23 or PRBS-7 generation and monitoring for off-line link verification

### Block Diagram



- Configured, controlled, and monitored using a generic 32-bit microprocessor interface
- Provides a standard 5-signal IEEE 1149.1 JTAG test port for boundary scan test purposes

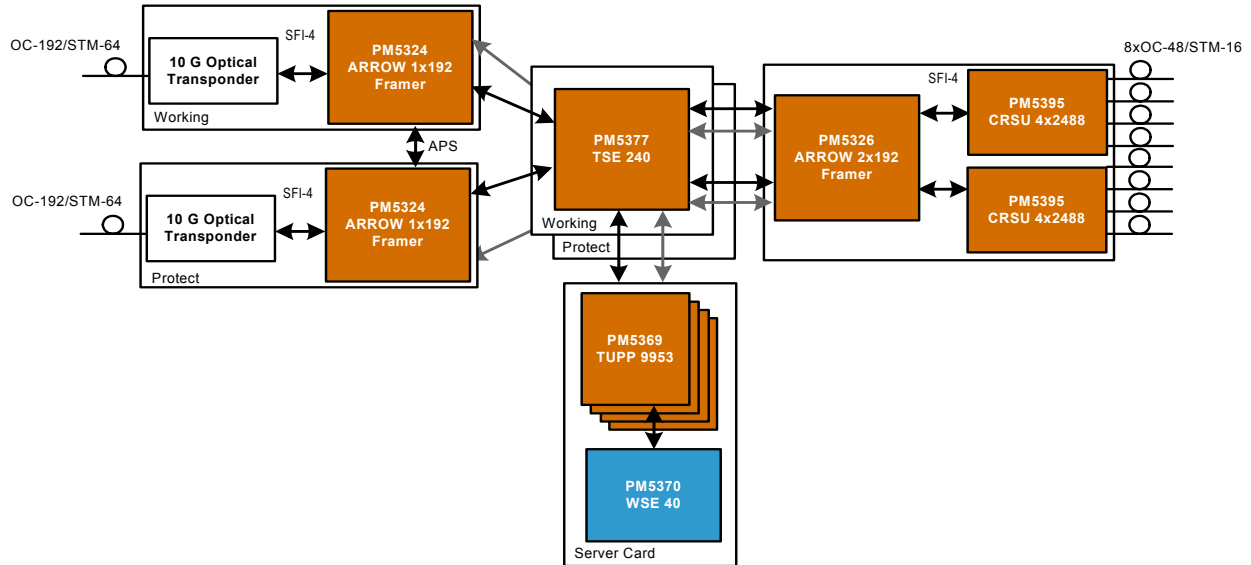
## Package

- Implemented in 1.2 V core and 2.5 V I/O 0.13µm CMOS technology. Inputs are 3.3 V tolerant
- Packaged in a 672-ball FCBGA top-hat, 27 mm x 27mm

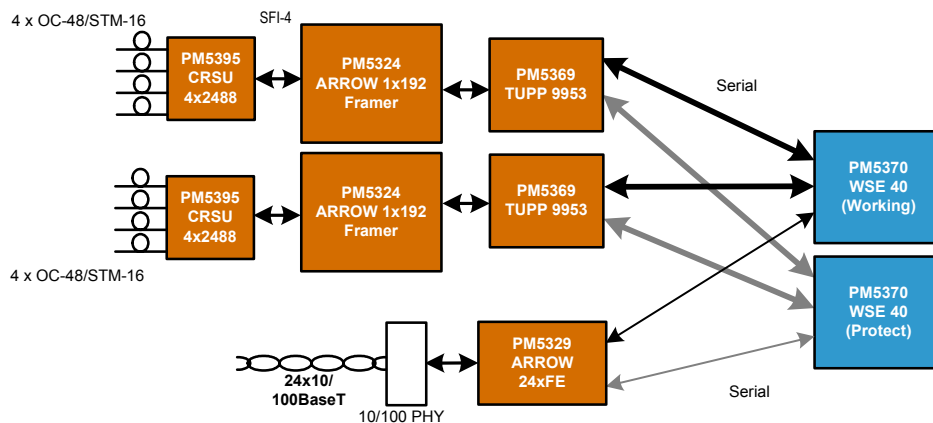
## Applications

- SONET/SDH Add-Drop Multiplexer (ADM)
- SONET/SDH Digital Cross-connect (DCC)
- Multi-service Provisioning Platform (MSPP)
- Multi-service ADM (MS-ADM)
- Multi-service Switch (MSS)
- Optical Access Mux
- Terminal Multiplexers

## OC-192/STM-64 Optical Cross-Connect with 40G VT/TU Cross-Connect Server Card



## OC-48/STM-16 VT/TU ADM/Cross-Connect



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