Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PM5397 ARROW 2xGE

Two Channel Gigabit Ethernet to SONET Mapping Device

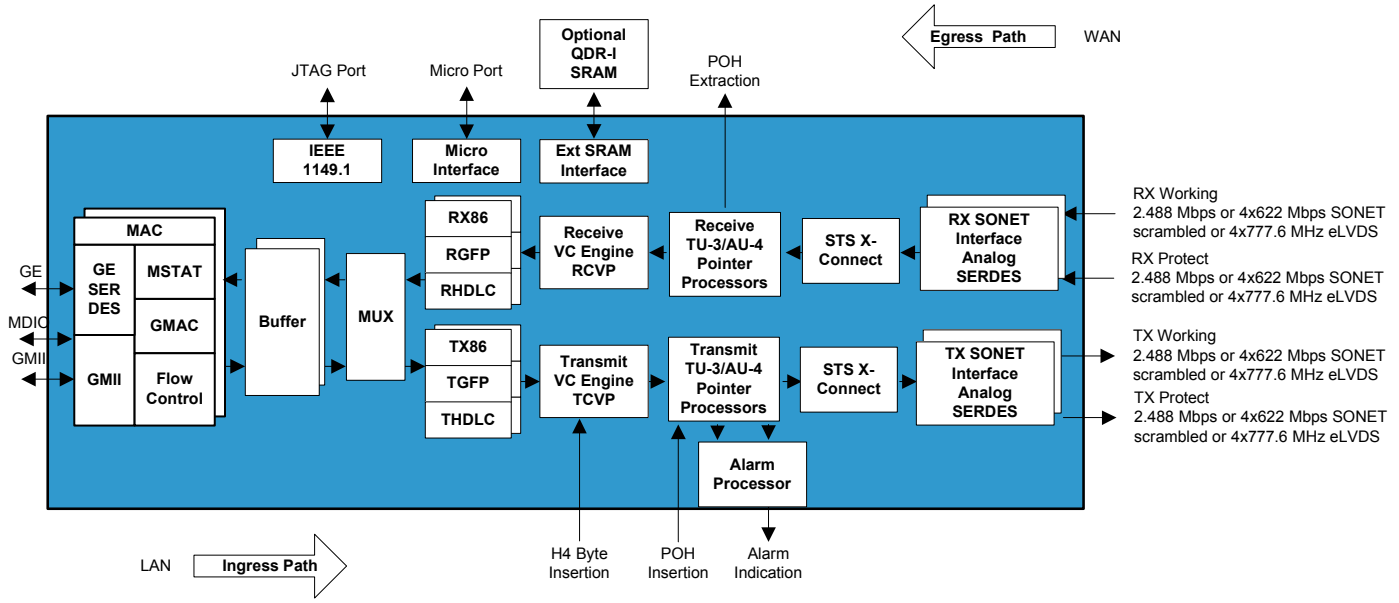
PMC-SIERRA

Preliminary Product Brief

Product Highlights

- Single chip, dual channel Gigabit Ethernet, SONET/SDH Virtual Concatenation (VC) mapper to STS-48/STM-16 using either frame mapped Generic Frame Procedure (GFP), LAPS/X.86 or BCP/PPP HDLC encapsulation.
- Provides direct IEEE 802.3 Ethernet line-side connection to optics via two internal Serializer/Deserializer (SERDES) and provides optional connection to Gigabit Ethernet physical layer devices via two GMII interfaces.
- Supports full-rate and oversubscribed data transfer of Gigabit Ethernet over SONET/SDH with STS-1/VC-3 granularity. Ethernet back-pressure prevents packet loss when SONET/SDH channel is over-subscribed.
- Provides a total of 92.8 Kbytes of Ethernet ingress buffer and a total of 28.8 Kbytes of Ethernet egress buffer per channel.
- Supports IEEE 802.3 flow control, auto-negotiation, and management statistics.
- Maps each of two channels of Gigabit Ethernet using frame mapped GFP Ethernet over SONET, LAPS/X.86 or BCP/PPP HDLC encapsulation protocol into a standards-based virtual concatenation stream consisting of between 1 to 8 STS-3c/VC-4 or between 1 to 24 STS-1/VC-3 channels. The VC-3 channels can be either TU-3 mapped or AU-3 mapped.
- Alternatively maps one Gigabit Ethernet channel into an STS-48c (STM-16/AU-4-16c) channel or maps each Gigabit Ethernet channel into either an STS-24c/STM-8, STS-12c/STM-4, STS-9c, STS-6c, STS-3c/STM-1, STS-1/STM-0, TU-3 (VC-3) channel.
- Supports on-chip virtual concatenation differential delay buffers of 125 microseconds or off-chip virtual concatenation differential delay buffers of up to 50 milli-seconds using external Quad Data Rate (QDR-I) SRAM interface.
- Interprets any legal mix of STS (AU-4/AU-3) pointer bytes (H1, H2, and H3), extracts the synchronous payload envelope(s) and processes the path overhead for the receive stream. Generates STS (AU-4/AU-3) pointer bytes (H1, H2, and H3) with offset of 0 (J1 immediately after H3 byte) or 522 (J1 immediately after the J0/Z0 bytes). Inserts the path overhead for the transmit stream.
- Interprets any legal mix of TU-3 pointer bytes (H1, H2 and H3) extracts the VC-3 synchronous payload envelope(s) and processes the path overhead (both VC-4 and VC-3 for the received data stream). Generates TU-3 pointer bytes (H1, H2 and H3) of offset 0. Inserts both the VC-4 and VC-3 path overhead bytes.
- Performs full SONET/SDH path termination, including the processing of H4, C2 and J1 bytes for virtual concatenation.
- Supports GFP Client Management and LAPS/X.86 Control Packet insertion and extraction.

Block Diagram



PMC-2000861, Issue 4

- Provides working and protect WAN side interfaces. These ports may be configured as 4 x 777.6 MHz eLVDS, 4 x 622 MHz Serial SONET/SDH eLVDS Interface, or 1 x 2.488 Gbps Serial SONET/SDH eLVDS Interface.
- Supports arbitrary assignment of STS-1 (AU-3) channels via Time Slot Interchange on working and protect WAN side interfaces.
- Supports mapping and demapping of two Gigabit Ethernet channels into a single STS-48c (STM-16/AU-4-16c) channel via a programmable 32-bit prepend field.
- Offers per-channel Ethernet side and WAN side loopbacks for system level diagnostic capability.
- Provides on-chip data recovery and clock synthesis for Gigabit Ethernet and SONET/SDH interfaces.

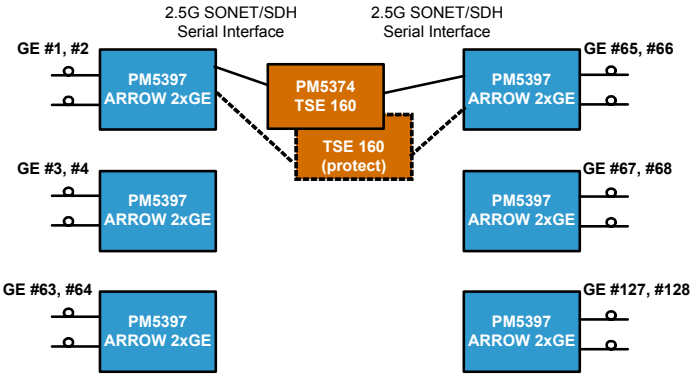
General

- General-purpose 16-bit microprocessor interface for configuration, management and statistics gathering.
- Standard 5 signal IEEE 1149.1 JTAG test port.
- Low power 1.8 V core with 5.0 V tolerant 3.3 V TTL compatible I/O.
- Industrial temperature range (-40 °C to +85 °C).
- 896-pin FCBGA package.

Applications

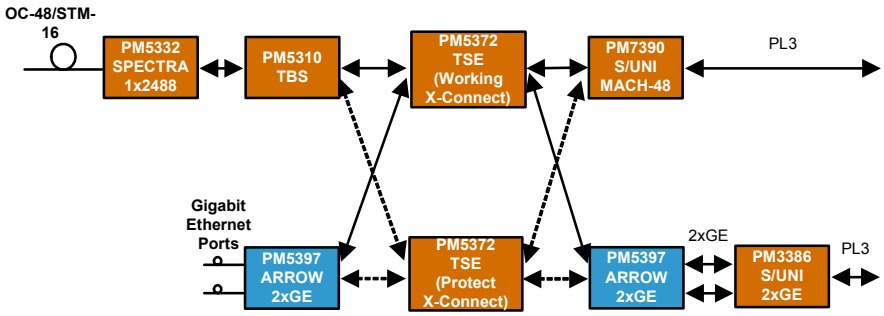
- High density EOS port cards, mapping multiple GE channels into OC-48/STM-16 or OC-192/STM-64 streams.
- Gigabit Ethernet port cards for Multi-Service Provisioning Platforms.
- Non-blocking 128-512 port single-stage fabric Gigabit Ethernet Cross Connect.

128 Port GE Cross Connect



Gigabit Ethernet to SONET/SDH OC-48/STM-16 Port Card

Gigabit Ethernet Port Card for Multi-Service Provisioning Platform



Corporate Head Office:
PMC-Sierra, Inc.
Mission Towers One
3975 Freedom Circle
Santa Clara, CA, 95054, U.S.A.
Tel: 1.408.239.8000
Fax: 1.408. 492.1157

Operations Head Office:
PMC-Sierra, Inc.
100-2700 Production Way
Burnaby, BC V5A 4X1 Canada
Tel: 1.604.415.6000
Fax: 1.604.415.6200

PMC-SIERRA

Enabling connectivity. Empowering people.