



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

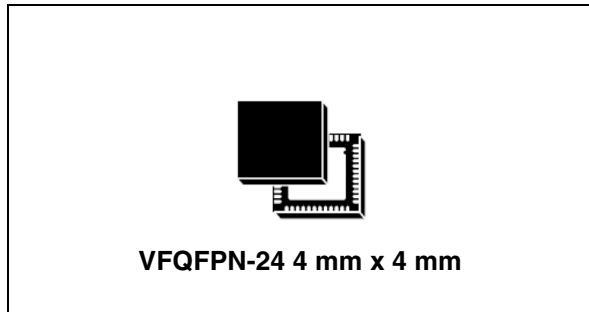
Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

6-row 32 mA LED driver with boost regulator for LCD panel backlight

Features

- Boost section
 - 4.7 V to 28 V input voltage range
 - Internal power MOSFET
 - Internal +5 V LDO for device supply
 - Up to 36 V output voltage
 - Constant frequency peak current-mode control
 - 200 kHz to 1 MHz adjustable switching frequency
 - External synchronization for multi-device application
 - Pulse-skip power saving mode at light load
 - Programmable soft-start
 - Programmable OVP protection
 - Stable with ceramic output capacitors
 - Thermal shutdown
- Backlight driver section
 - Six rows with 32 mA maximum current capability (adjustable)
 - Up to 10 WLEDs per row
 - Unused rows detection
 - 500 ns minimum dimming time (1% minimum dimming duty-cycle at 20 kHz)
 - $\pm 2.1\%$ current accuracy
 - $\pm 2\%$ current matching between rows
 - LED failure (open and short circuit) detection



Description

The PM6600 consists of a high efficiency monolithic boost converter and six controlled current generators (ROWS), specifically designed to supply LEDs arrays used in the backlight of LCD panels. The device can manage a nominal output voltage up to 36 V (i.e. 10 White-LEDs per ROW). The generators can be externally programmed to sink up to 32 mA and they can be dimmed via a PWM signal (1% dimming duty-cycle at 20 kHz can be managed). The device allows to detect and manage the open and shorted LED faults and to let unused ROWs floating. Basic protections (output over-voltage, internal MOSFET over-current and thermal shutdown) are provided.

Applications

- Notebook monitors backlight
- UMPC backlight

Table 1. Device summary

Order codes	Package	Packaging
PM6600	VFQFPN-24 4 mm x 4 mm (exposed pad)	Tube
PM6600TR		Tape and reel

Contents

1	Typical application circuit	7
2	Pin settings	8
2.1	Connections	8
2.2	Pin description	8
3	Electrical data	10
3.1	Maximum rating	10
3.2	Thermal data	10
3.3	Recommended operating conditions	11
4	Electrical characteristics	12
5	Typical operating characteristics	15
6	Block diagram	25
7	Operation description	26
7.1	Boost section	26
7.1.1	Functional description	26
7.2	Overshoot protection	27
7.3	Switching frequency selection and synchronization	28
7.4	System stability	30
7.4.1	Loop compensation	30
7.4.2	Slope compensation	32
7.5	Soft-start	33
7.6	Boost current limit	35
7.7	Enable function	35
7.8	Thermal protection	36
8	Backlight driver section	37
8.1	Current generators	37
8.2	PWM dimming	38

9	Fault management	39
9.1	FAULT pin	39
9.2	MODE pin	39
9.3	Open LED fault	40
9.4	Shorted LED fault	40
9.5	Intermittent connection	40
10	Package mechanical data	42
Appendix A	Layout guidelines	44
A.1	Basic points:	44
A.1.1	GNDs planes - 1 device	44
A.1.2	GNDs planes - 3 devices (RGB)	44
A.2	Compensation network	44
A.3	LX area – vout power area	45
A.4	Overshoot voltage divider	45
A.5	LDO5 – AVCC filter	45
A.6	ROWS current generators	45
A.7	Top layer of the standard PM6600 demonstration board	46
Appendix B	Application note	48
B.1	Inductor selection	48
B.2	Capacitors selection	48
B.3	Flywheel diode selection	48
B.4	Design example	49
B.4.1	Switching frequency setting	49
B.4.2	Row current setting	49
B.4.3	Inductor choice	49
B.4.4	Output capacitor choice	51
B.4.5	Input capacitor choice	52
B.4.6	Overshoot voltage protection divider setting	52
B.4.7	Compensation network	53
B.4.8	Boost current limit	53
B.4.9	Soft-start	54

Appendix C Application suggestions	55
C.1 Full application schematic	55
C.2 EN, DIM path in production line	56
C.3 ROW pins protection	57
C.4 Debug and measurements test points	57
C.5 Inductor choice	58
11 Revision history	59

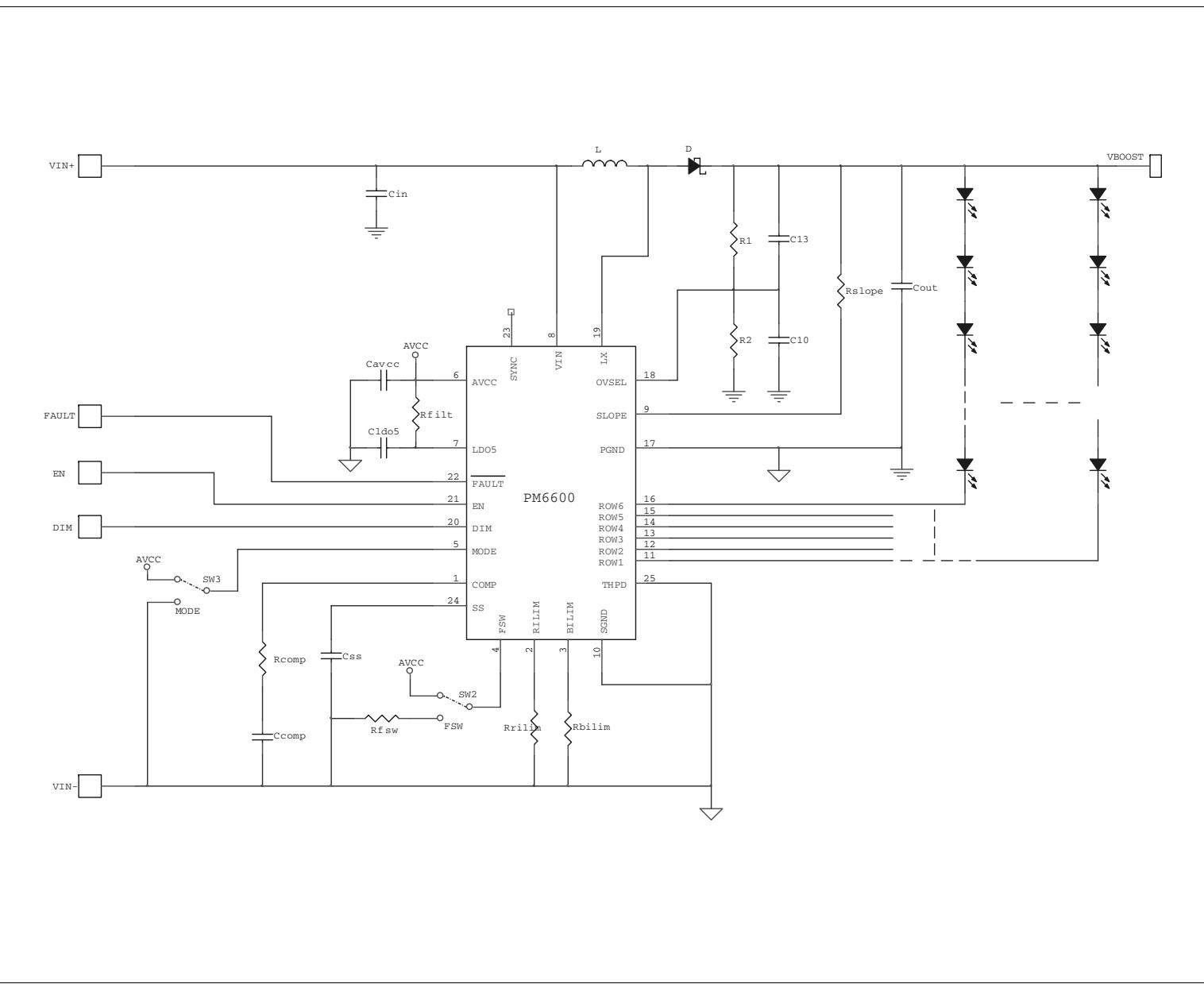
List of figures

Figure 1.	Application circuit	7
Figure 2.	Pin connection (through top view)	8
Figure 3.	Efficiency vs DIM duty cycle @ fDIM = 200 Hz.	15
Figure 4.	Efficiency vs DIM duty cycle @ fDIM = 500 Hz.	15
Figure 5.	Efficiency vs DIM duty cycle @ fDIM = 1 kHz.	15
Figure 6.	Efficiency vs DIM duty cycle @ fDIM = 5 kHz.	15
Figure 7.	Efficiency vs DIM duty cycle @ fDIM = 10 kHz.	16
Figure 8.	Efficiency vs DIM duty cycle @ fDIM = 20 kHz.	16
Figure 9.	Efficiency vs DIM duty cycle @ Vin = 8 V.	16
Figure 10.	Efficiency vs DIM duty cycle @ Vin = 12 V.	16
Figure 11.	Efficiency vs DIM duty cycle @ Vin = 18 V.	16
Figure 12.	Efficiency vs DIM duty cycle @ Vin = 24 V.	16
Figure 13.	Efficiency vs Vin @ DIM duty cycles = 10%	17
Figure 14.	Efficiency vs Vin @ DIM duty cycles = 50%	17
Figure 15.	Efficiency vs Vin @ DIM duty cycles = 75%	17
Figure 16.	Efficiency vs Vin @ DIM duty cycles = 100%	17
Figure 17.	Working waveforms @ fDIM = 100 Hz, D = 1%	18
Figure 18.	Working waveforms @ fDIM = 100 Hz, D = 10%	18
Figure 19.	Working waveforms @ fDIM = 100 Hz, D = 50%	18
Figure 20.	Working waveforms @ fDIM = 100 Hz, D = 80%	18
Figure 21.	Working waveforms @ fDIM = 200 Hz, D = 1%	19
Figure 22.	Working waveforms @ fDIM = 200 Hz, D = 20%	19
Figure 23.	Working waveforms @ fDIM = 200 Hz, D = 50%	19
Figure 24.	Working waveforms @ fDIM = 200 Hz, D = 80%	19
Figure 25.	Working waveforms @ fDIM = 500 Hz, D = 1%	20
Figure 26.	Working waveforms @ fDIM = 500 Hz, D = 50%	20
Figure 27.	Working waveforms @ fDIM = 1 kHz, D = 1%	20
Figure 28.	Working waveforms @ fDIM = 1 kHz, D = 50%	20
Figure 29.	Working waveforms @ fDIM = 10 kHz, D = 1%	21
Figure 30.	Working waveforms @ fDIM = 10 kHz, D = 50%	21
Figure 31.	Working waveforms @ fDIM = 20 kHz, D = 1%	21
Figure 32.	Working waveforms @ fDIM = 20 kHz, D = 50%	21
Figure 33.	Output voltage ripple @ fDIM = 200 Hz, D = 1%	22
Figure 34.	Output voltage ripple @ fDIM = 200 Hz, D = 20%	22
Figure 35.	Output voltage ripple @ fDIM = 200 Hz, D = 50%	22
Figure 36.	Output voltage ripple @ fDIM = 200 Hz, D = 80%	22
Figure 37.	Shorted LED protection @ fDIM = 200 Hz all WLEDs connected	23
Figure 38.	Shorted LED protection @ fDIM = 200 Hz 1 WLED shorted	23
Figure 39.	Shorted LED protection @ fDIM = 200 Hz 2 WLEDs shorted.	23
Figure 40.	Shorted LED protection @ fDIM = 200 Hz 3 WLEDs shorted - ROW disabled	23
Figure 41.	Open ROW detection @ fDIM = 200 Hz.	24
Figure 42.	Simplified block diagram.	25
Figure 43.	AVCC filtering	26
Figure 44.	OVP threshold setting.	28
Figure 45.	Multiple device synchronization	28
Figure 46.	External sync waveforms	29
Figure 47.	Poor phase margin (a) and properly damped (b) load transient responses	31
Figure 48.	Load transient response measurement set-up	32

Figure 49.	Main loop and current loop diagram	32
Figure 50.	Effect of slope compensation on small inductor current perturbation (D > 0.5)	33
Figure 51.	Soft-start sequence waveforms in case of floating ROWs	34
Figure 52.	fDIM enabling schematic	36
Figure 53.	VFQFPN-24 mechanical data	43
Figure 54.	Top layer critical signals components assembly and layout	46
Figure 55.	Top side	47
Figure 56.	Bottom side	47
Figure 57.	Inductor current in DCM operation	50
Figure 58.	Full application schematic	55
Figure 59.	EN pin filter	56
Figure 60.	DIM pin filter	56
Figure 61.	ROW pins protection	57

1 Typical application circuit

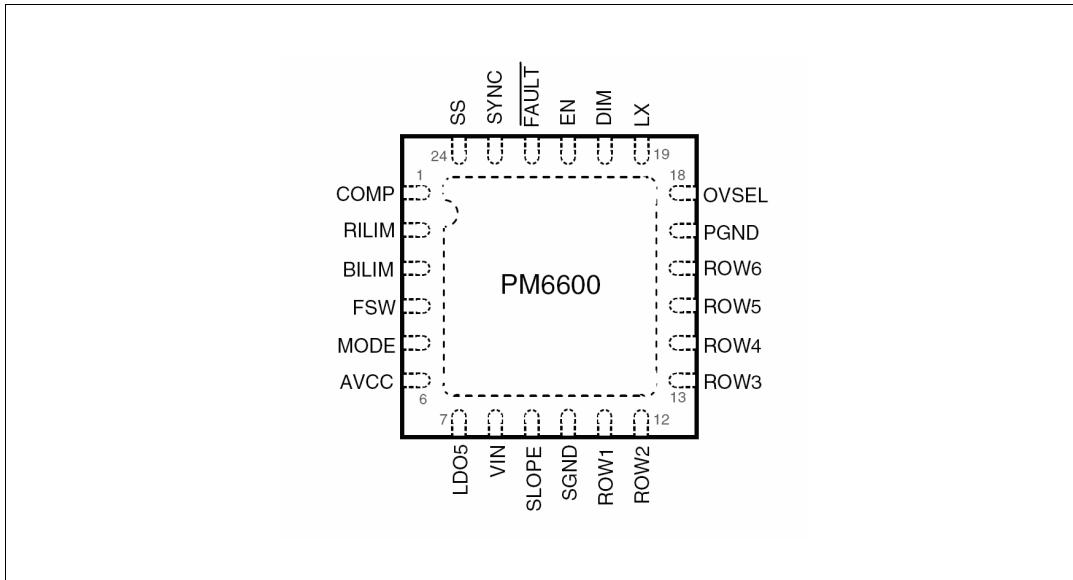
Figure 1. Application circuit



2 Pin settings

2.1 Connections

Figure 2. Pin connection (through top view)



2.2 Pin description

Table 2. Pin functions

N°	Pin	Function
1	COMP	Error amplifier output. A simple RC series between this pin and ground is needed to compensate the loop of the boost regulator.
2	RILIM	Output generators current limit setting. The output current of the ROWs can be programmed connecting a resistor to SGND.
3	BILIM	Boost converter current limit setting. The internal MOSFET current limit can be programmed connecting a resistor to SGND.
4	FSW	Switching frequency selection and external sync input. A resistor to SGND is used to set the desired switching frequency. The pin can also be used as external synchronization input. See Section 7.3 on page 28 for details.
5	MODE	Current generators fault management selector. It allows to detect and manage LEDs failures. See Section 9.2 on page 39 for details.
6	AVCC	+5 V analog supply. Connect to LDO5 through a simple RC filter.
7	LDO5	Internal +5 V LDO output and power section supply. Bypass to SGND with a 1 μ F ceramic capacitor.
8	VIN	Input voltage. Connect to the main supply rail.

Table 2. Pin functions (continued)

N°	Pin	Function
9	SLOPE	Slope compensation setting. A resistor between the output of the boost converter and this pin is needed to avoid sub-harmonic instability. Refer to section 1.4 for details.
10	SGND	Signal ground. Supply return for the analog circuitry and the current generators.
11	ROW1	Row driver output #1.
12	ROW2	Row driver output #2.
13	ROW3	Row driver output #3.
14	ROW4	Row driver output #4.
15	ROW5	Row driver output #5.
16	ROW6	Row driver output #6.
17	PGND	Power ground. Source of the internal power-MOSFET.
18	OVSEL	Over-voltage selection. Used to set the desired OV threshold by an external divider. See Section 7.2 on page 27 for details.
19	LX	Switching node. Drain of the internal power-MOSFET.
20	DIM	Dimming input. Used to externally set the brightness of the LEDs by using a PWM signal.
21	EN	Enable input. When low, the device is turned off. If tied high or left floating, the device is turned on and a soft-start sequence takes place.
22	FAULT	Fault signal output. Open drain output. The pin goes low when a fault condition is detected (see Section 9.1 on page 39 for details).
23	SYNC	Synchronization output. Used as external synchronization output.
24	SS	Soft-start. Connect a capacitor to SGND to set the desired soft-start duration.

3 Electrical data

3.1 Maximum rating

Table 3. Absolute maximum ratings⁽¹⁾

Symbol	Parameter	Value	Unit
V_{AVCC}	AVCC to SGND	-0.3 to 6	V
V_{LDO5}	LDO5 to SGND	-0.3 to 6	
	PGND to SGND	-0.3 to 0.3	
V_{IN}	VIN to PGND	-0.3 to 40	
V_{LX}	LX to SGND	-0.3 to 40	
	LX to PGND	-0.3 to 40	
	RILIM, BILIM, SYNC, OVSEL, SS to SGND	-0.3 to $V_{AVCC} + 0.3$	
	EN, DIM, FSW, MODE, FAULT to SGND	-0.3 to 6	
	ROWx to PGND/ SGND	-0.3 to 40	
	SLOPE to VIN	$V_{IN} - 0.3$ to $V_{IN} + 6$	
	SLOPE to SGND	-0.3 to 40	
	Maximum LX RMS current	2.0	A
P_{TOT}	Power dissipation @ = 25 °C	2.3	W
	Maximum withstanding voltage range test condition: CDF-AEC-Q100-002- "human body model" acceptance criteria: "normal performance"	± 2000	V

1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	42	°C/W
T_{STG}	Storage temperature range	-50 to 150	°C
T_J	Junction operating temperature range	-40 to 125	°C
T_A	Operating ambient temperature range	-40 to 85	°C

3.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter		Values			Unit
			Min	Typ	Max	
Supply section						
V_{IN}	Input voltage range		4.7	-	28	V
Boost section						
V_{BST}	Output voltage range			-	36	V
f_{SW}	Adjustable switching frequency	FSW connected to R_{FSW}	200	-	1000	kHz
	FSW sync input duty-cycle			-	40	%
I_{rowx}	ROWS output maximum current			-	32	mA

4 Electrical characteristics

$V_{IN} = 12 \text{ V}$; $T_A = 0 \text{ }^\circ\text{C}$ to $85 \text{ }^\circ\text{C}$ and MODE connected to AVCC unless specified⁽¹⁾.

Table 6. Electrical characteristics

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
Supply section						
V_{LDO5}, V_{AVCC}	LDO output and IC supply voltage	EN High, $I_{LDO5} = 0 \text{ mA}$	4.6	5	5.5	V
$I_{IN,Q}$	Operating quiescent current	$R_{RILIM} = 51 \text{ k}\Omega$, $R_{BILIM} = 220 \text{ k}\Omega$, $R_{SLOPE} = 680 \text{ k}\Omega$ DIM tied to SGND.		1		mA
$I_{IN,SHDN}$	Operating current in shutdown	EN low		20	30	μA
$V_{UVLO,ON}$	LDO5 under voltage lockout upper threshold			4.6	4.75	V
$V_{UVLO,OFF}$	LDO5 under voltage lockout lower threshold		3.8	4.0		
LDO linear regulator						
	Line regulation	$6 \text{ V} = V_{IN} = 28 \text{ V}$, $I_{LDO5} = 30 \text{ mA}$			25	mV
	LDO dropout voltage	$V_{IN} = 4.3 \text{ V}$, $I_{LDO5} = 10 \text{ mA}$		80	120	
	LDO maximum output current limit	$V_{LDO5} > V_{UVLO,ON}$	25	40	60	mA
		$V_{LDO5} < V_{UVLO,OFF}$			30	

- $T_A = T_J$. All parameters at operating temperature extremes are guaranteed by design and statistical analysis (not production tested)

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
Boost section						
$t_{on,min}$	Minimum switching on time				200	ns
	Default switching frequency	FSW connected to AVCC	570	660	750	kHz
	Minimum FSW Sync frequency			210		
	FSW sync Input low level threshold		240			mV
	FSW sync Input hysteresis			60		
	FSW sync Min ON time				270	ns
	SYNC output duty-cycle	FSW connected to AVCC (Internal oscillator selected)		34	40	%
	SYNC output high level	$I_{SYNC} = 10 \mu A$	$V_{AVCC} -20$			mV
	SYNC output low level	$I_{SYNC} = -10 \mu A$			20	
Power switch						
K_B	LX current coefficient	$R_{BILIM} = 300 k\Omega$	5.7e5	6.7e5	7.7e5	V
	Internal MOSFET R_{DSon}			280	500	$m\Omega$
OV protections						
$V_{TH,OVP}$	Overvoltage protection reference (OVSEL) threshold		1.190	1.235	1.280	V
$V_{TH,FRD}$	Floating ROWs detection (OVSEL) threshold		1.100	1.145	1.190	V
$\Delta V_{OVP,FRD}$	Voltage gap between the OVP and FRD thresholds			90		mV

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
Soft-start and power management						
	EN, turn-on level threshold				1.6	V
	EN, turn-off level threshold		0.8			
	DIM, high level threshold				1.3	
	DIM, low level threshold		0.8			
	EN, pull-up current			2.5		
	SS, charge current		4	5	6	
	SS, end-of-startup threshold		2	2.4	2.8	
	SS, reduced switching frequency Release threshold			0.8		V
Current generators section						
T _{DIM-ON,min}	Minimum dimming on-time	R _{RILIM} = 51 kΩ		500		ns
K _R	ROWS current coefficient accuracy	R _{RILIM} = 51 kΩ		998	±21	V
ΔI _{ROWx}	ROWS current mismatch ⁽¹⁾	R _{RILIM} = 51 kΩ			±2	%
V _{IFB}	Feedback regulation voltage	No LEDs mismatch		400		mV
V _{TH,FAULT}	Shorted LED fault detection threshold			8.2		V
V _{FAULT,LOW}	FAULT pin low-level voltage	I _{FAULT,SINK} = 4 mA			350	mV
Thermal shutdown						
T _{SHDN}	Thermal shutdown Turn-off temperature			150		°C

Note: The current mismatch is the maximum current difference among the ROWs of one device.

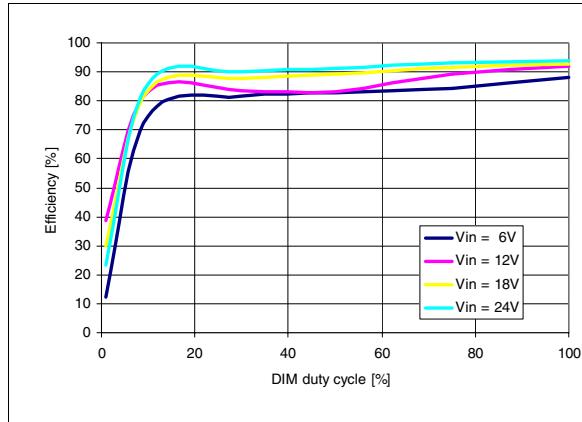
5 Typical operating characteristics

All the measures are done with a standard PM6600EVAL demonstration board and a standard WLED6021NB tamboured, with the components listed in the EVAL_KIT document.

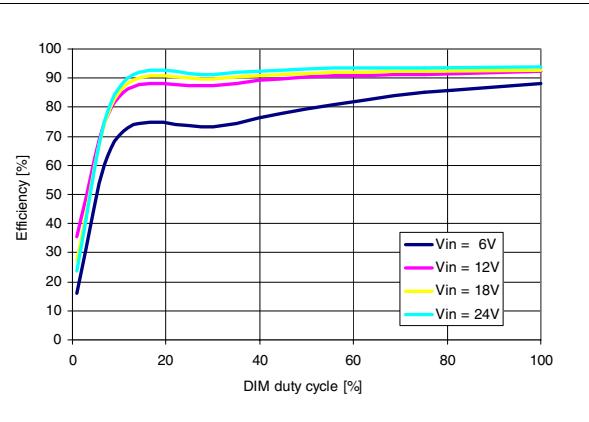
The measures are done with this working conditions, unless specified:

- $V_{in} = 12\text{ V}$
- $V_{out} = 6 \text{ rows} \times 10 \text{ WLEDs} = 34\text{ V (typ)}$
- $I_{out} = 20\text{ mA each row}$
- $f_{sw} = 660\text{ kHz (nominal switching frequency, with FSW. AVCC)}$
- $V_{row1}\text{ to }V_{row6} = \{0.697, 0.75, 0.818, 0.696, 0.822, 0.363\}\text{ V}$

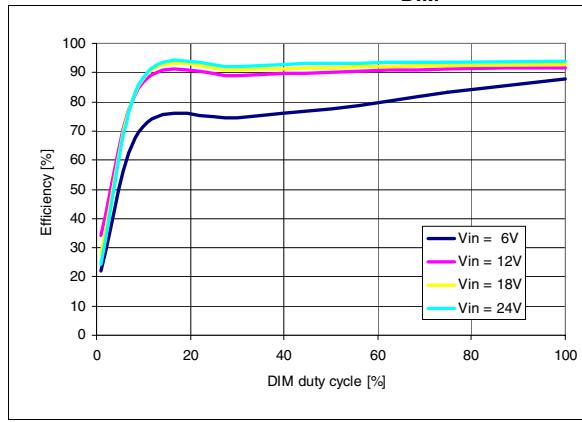
**Figure 3. Efficiency vs
DIM duty cycle @ $f_{DIM} = 200\text{ Hz}$**



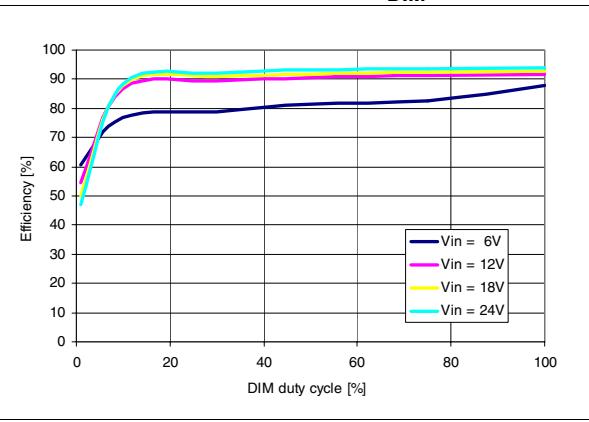
**Figure 4. Efficiency vs
DIM duty cycle @ $f_{DIM} = 500\text{ Hz}$**



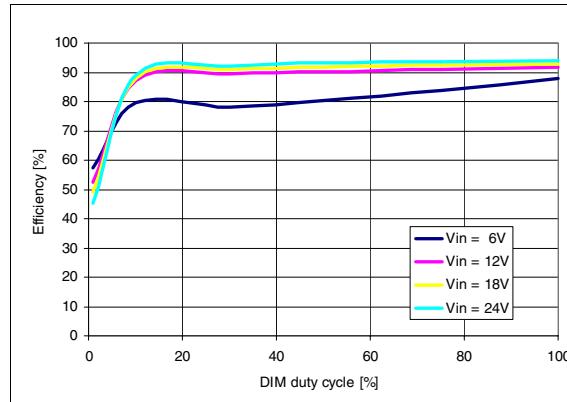
**Figure 5. Efficiency vs
DIM duty cycle @ $f_{DIM} = 1\text{ kHz}$**



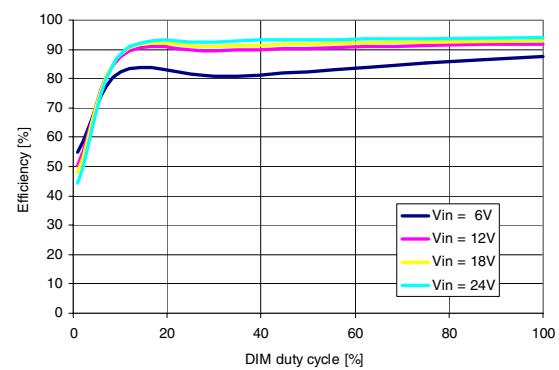
**Figure 6. Efficiency vs
DIM duty cycle @ $f_{DIM} = 5\text{ kHz}$**



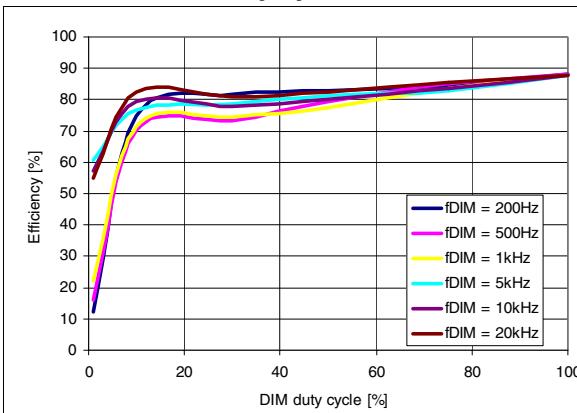
**Figure 7. Efficiency vs
DIM duty cycle @ $f_{\text{DIM}} = 10 \text{ kHz}$**



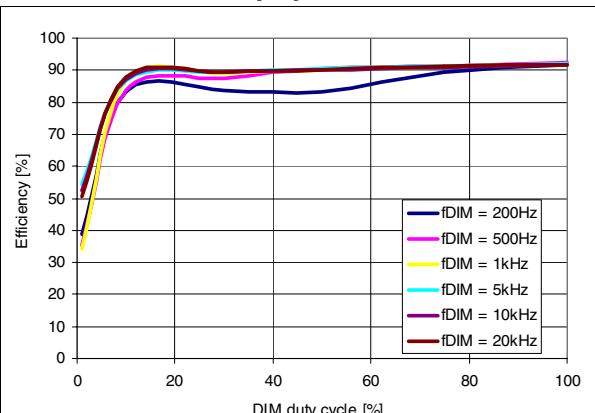
**Figure 8. Efficiency vs
DIM duty cycle @ $f_{\text{DIM}} = 20 \text{ kHz}$**



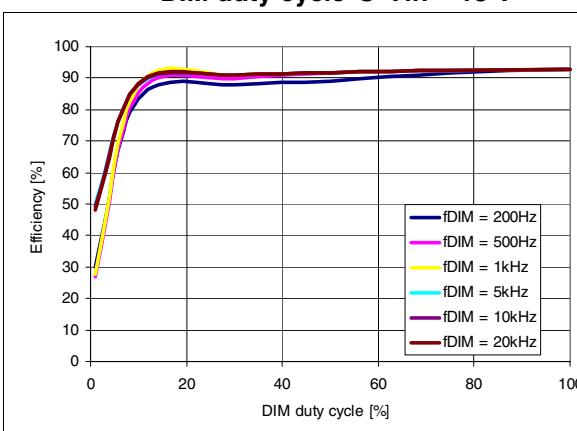
**Figure 9. Efficiency vs
DIM duty cycle @ $V_{\text{in}} = 8 \text{ V}$**



**Figure 10. Efficiency vs
DIM duty cycle @ $V_{\text{in}} = 12 \text{ V}$**



**Figure 11. Efficiency vs
DIM duty cycle @ $V_{\text{in}} = 18 \text{ V}$**



**Figure 12. Efficiency vs
DIM duty cycle @ $V_{\text{in}} = 24 \text{ V}$**

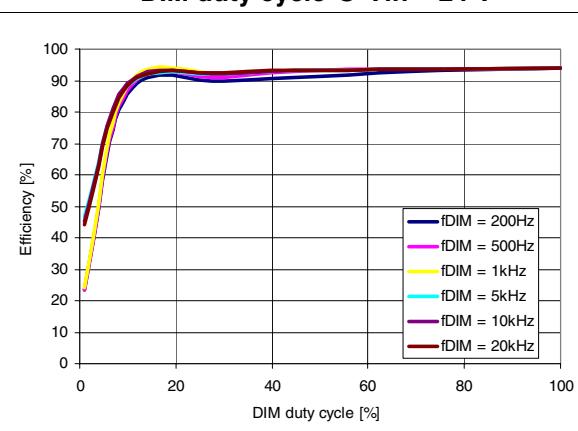


Figure 13. Efficiency vs Vin @ DIM duty cycles = 10%

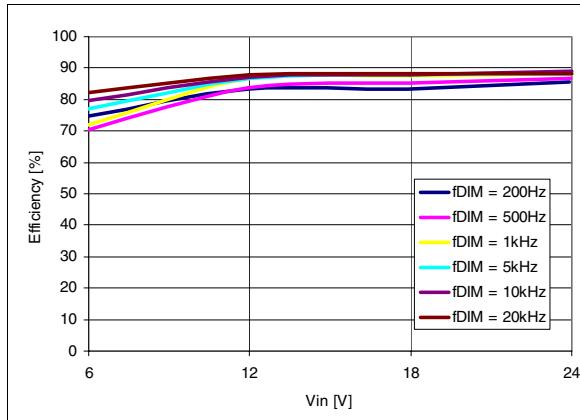


Figure 14. Efficiency vs Vin @ DIM duty cycles = 50%

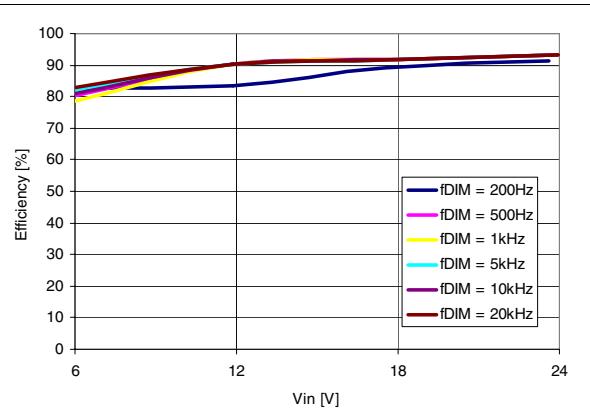


Figure 15. Efficiency vs Vin @ DIM duty cycles = 75%

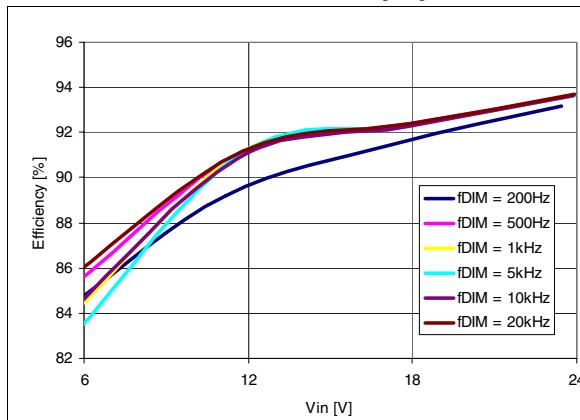
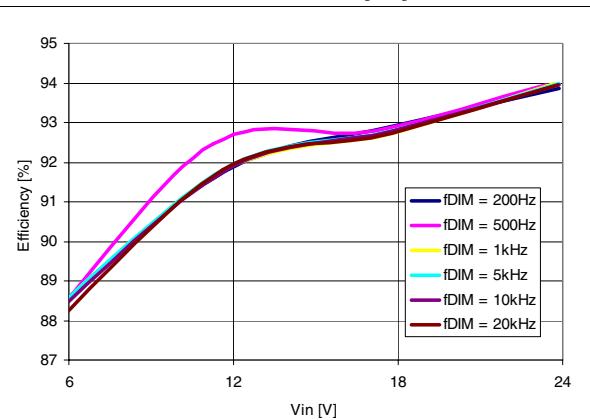
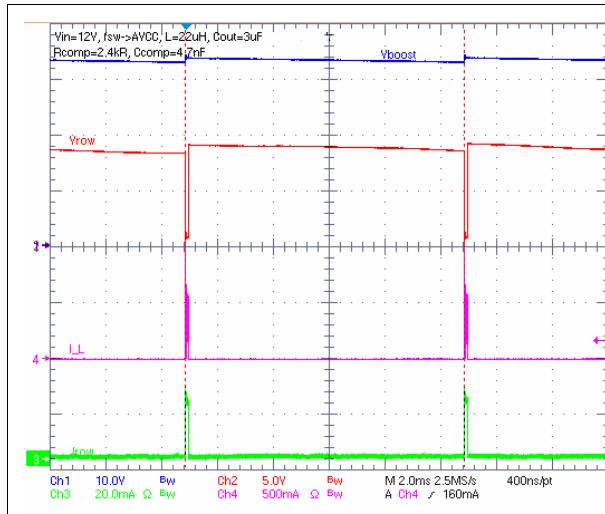


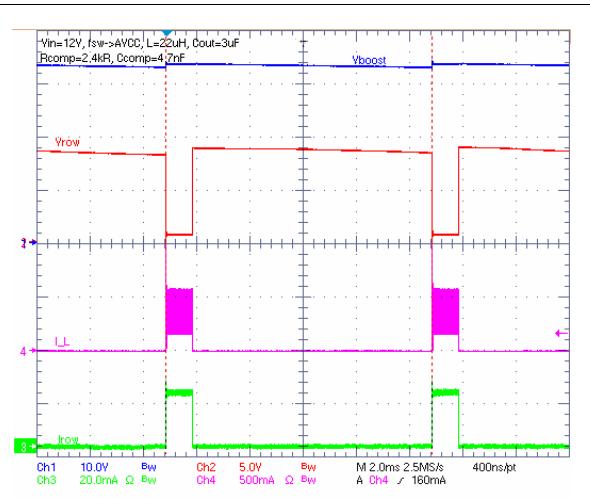
Figure 16. Efficiency vs Vin @ DIM duty cycles = 100%



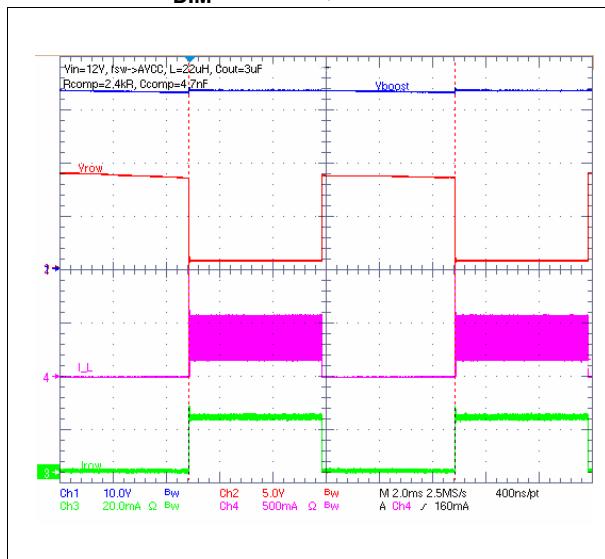
**Figure 17. Working waveforms @
 $f_{DIM} = 100$ Hz, D = 1%**



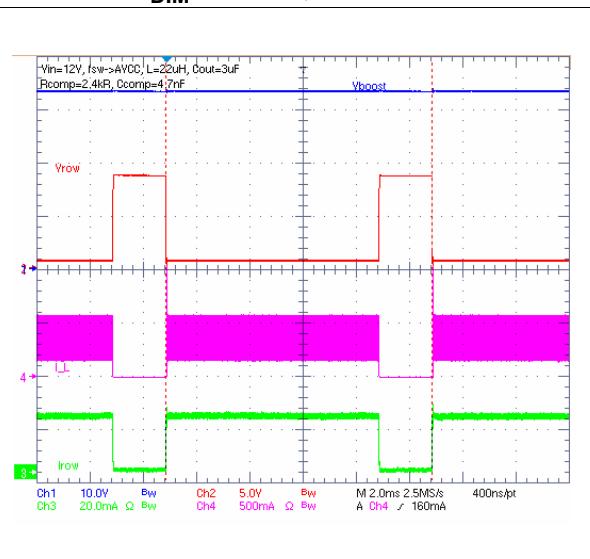
**Figure 18. Working waveforms @
 $f_{DIM} = 100$ Hz, D = 10%**



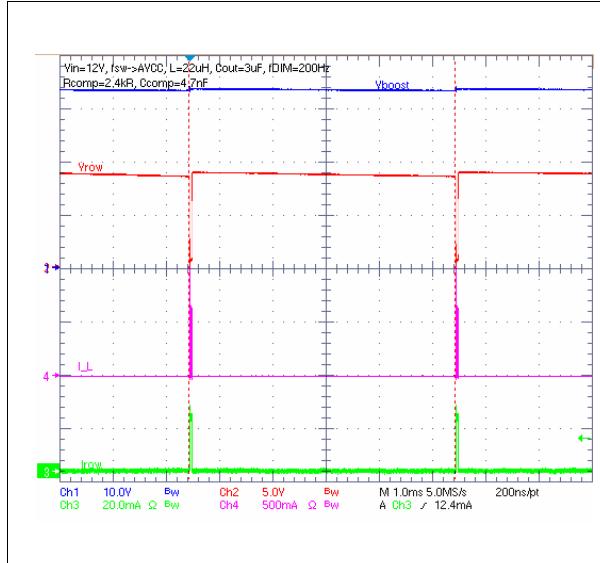
**Figure 19. Working waveforms @
 $f_{DIM} = 100$ Hz, D = 50%**



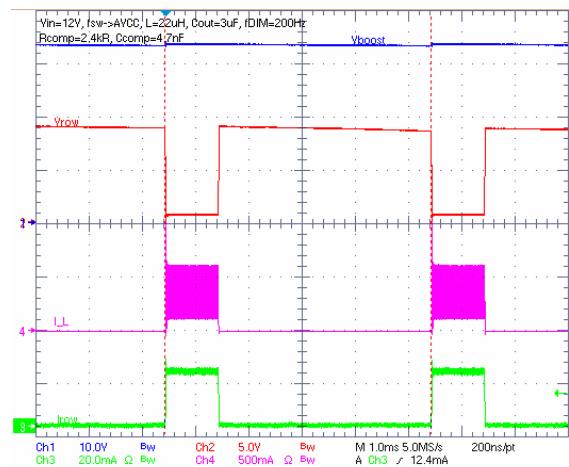
**Figure 20. Working waveforms @
 $f_{DIM} = 100$ Hz, D = 80%**



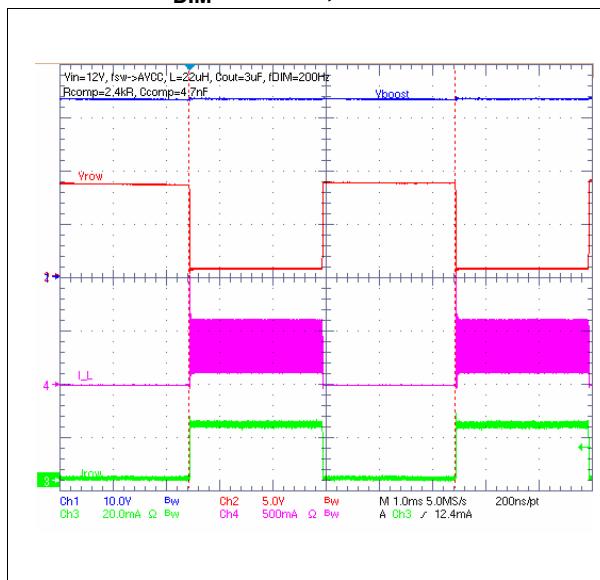
**Figure 21. Working waveforms @
 $f_{DIM} = 200$ Hz, D = 1%**



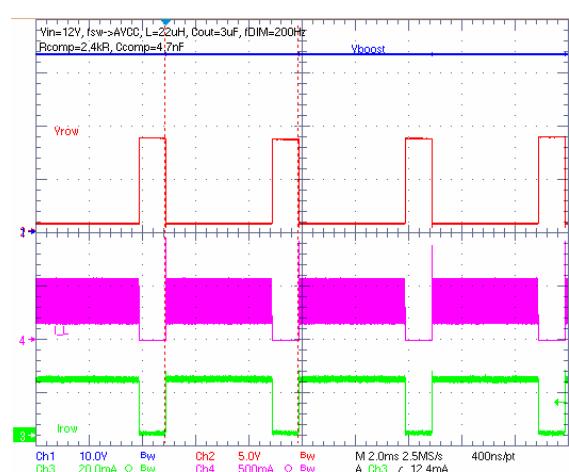
**Figure 22. Working waveforms @
 $f_{DIM} = 200$ Hz, D = 20%**



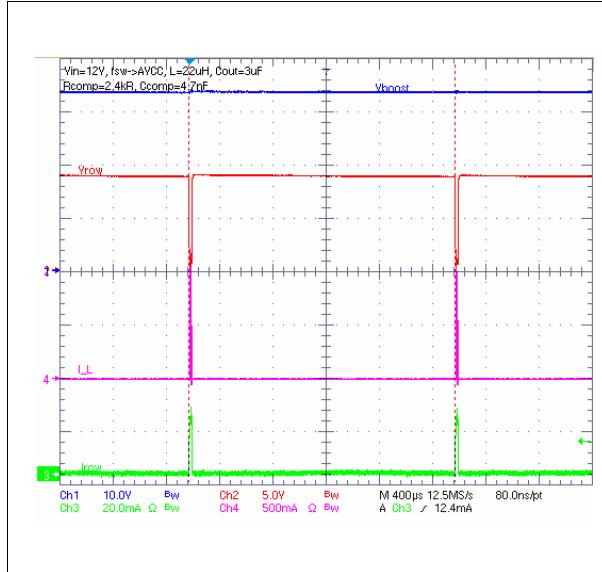
**Figure 23. Working waveforms @
 $f_{DIM} = 200$ Hz, D = 50%**



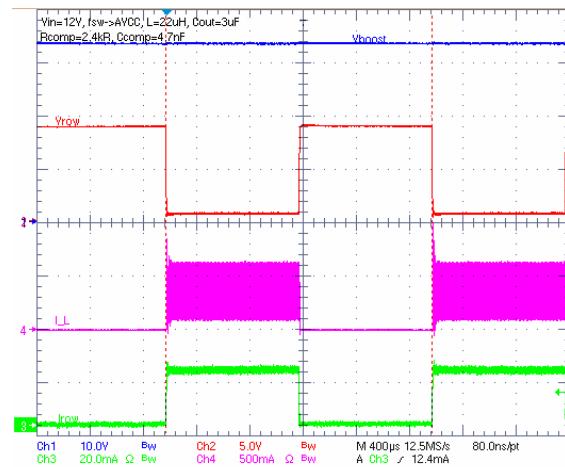
**Figure 24. Working waveforms @
 $f_{DIM} = 200$ Hz, D = 80%**



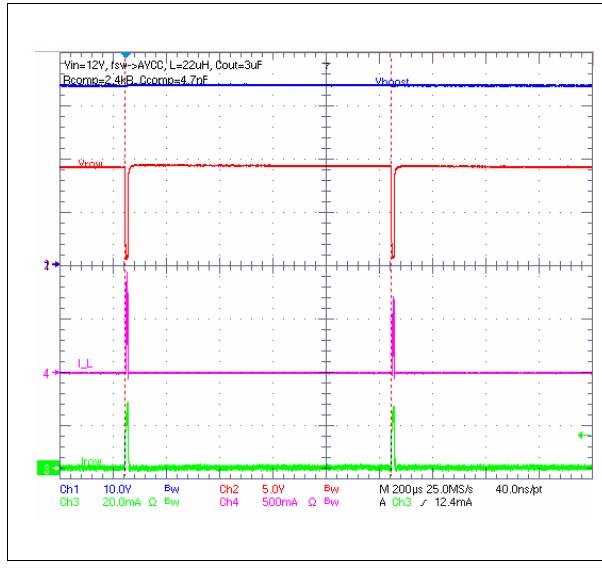
**Figure 25. Working waveforms @
 $f_{DIM} = 500$ Hz, D = 1%**



**Figure 26. Working waveforms @
 $f_{DIM} = 500$ Hz, D = 50%**



**Figure 27. Working waveforms @
 $f_{DIM} = 1$ kHz, D = 1%**



**Figure 28. Working waveforms @
 $f_{DIM} = 1$ kHz, D = 50%**

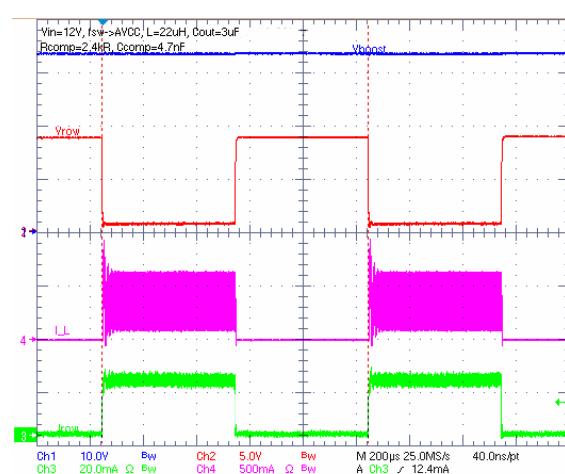


Figure 29. Working waveforms @ $f_{DIM} = 10 \text{ kHz}$, D = 1%

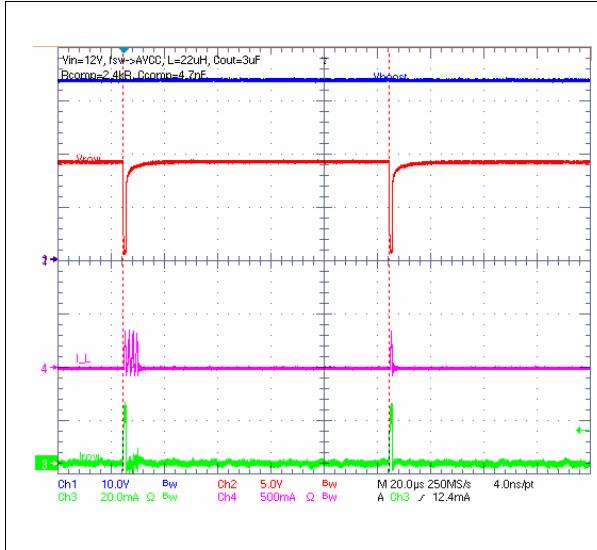


Figure 30. Working waveforms @ $f_{DIM} = 10 \text{ kHz}$, D = 50%

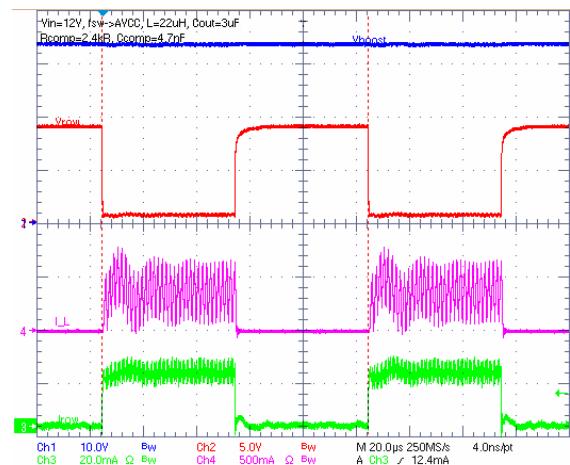


Figure 31. Working waveforms @ $f_{DIM} = 20 \text{ kHz}$, D = 1%

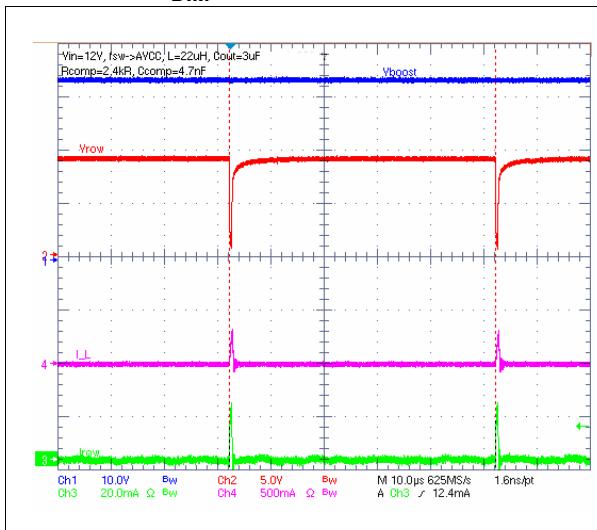
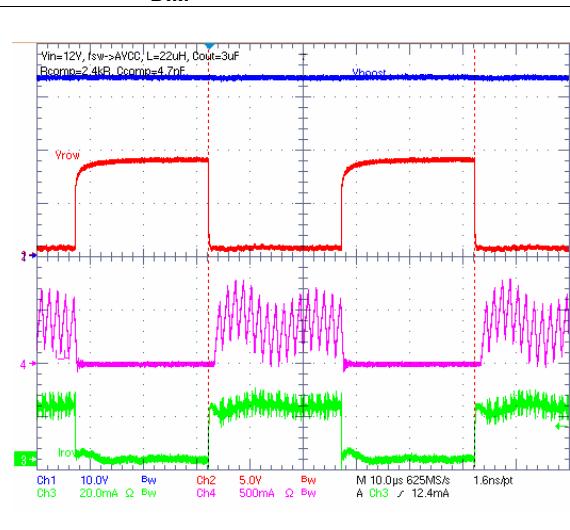
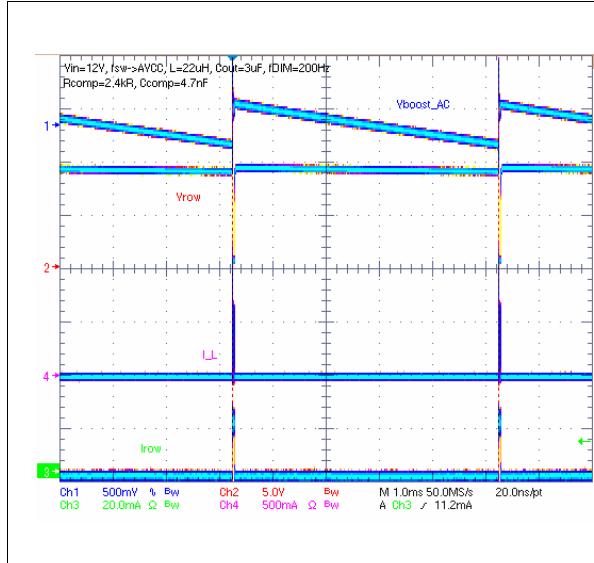


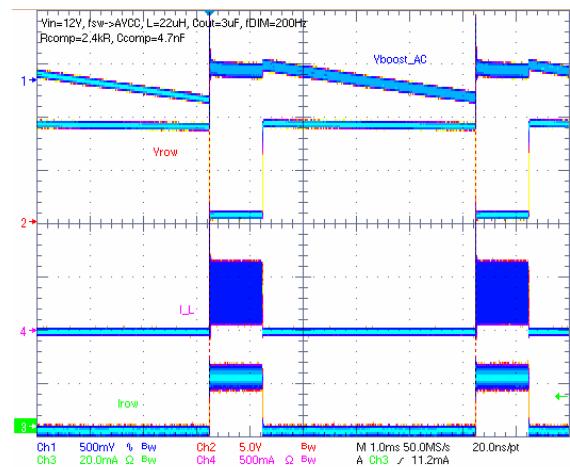
Figure 32. Working waveforms @ $f_{DIM} = 20 \text{ Hz}$, D = 50%



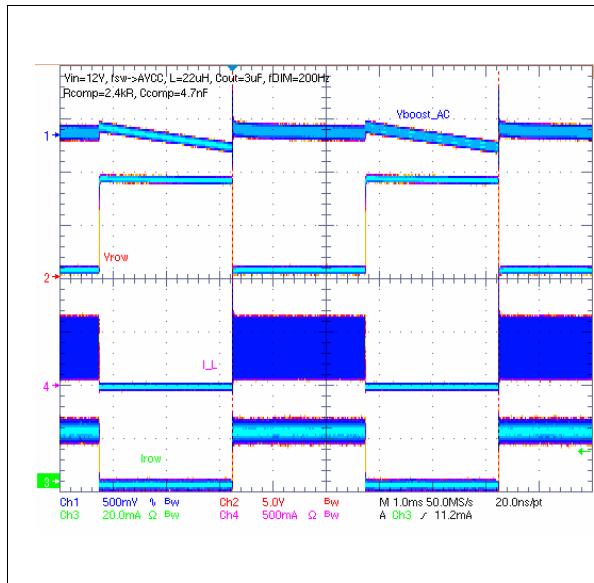
**Figure 33. Output voltage ripple @
 $f_{DIM} = 200$ Hz, D = 1%**



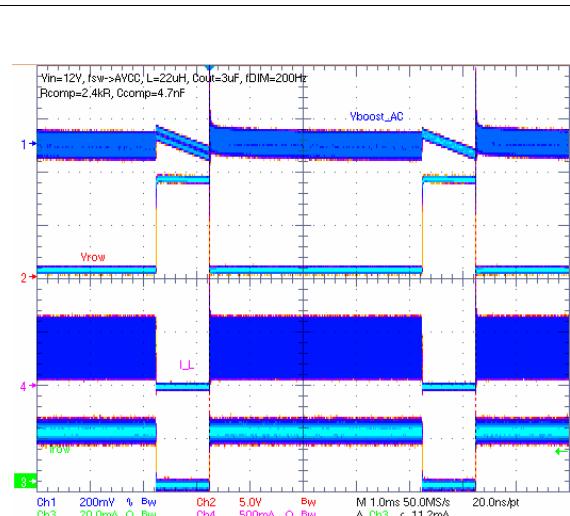
**Figure 34. Output voltage ripple @
 $f_{DIM} = 200$ Hz, D = 20%**



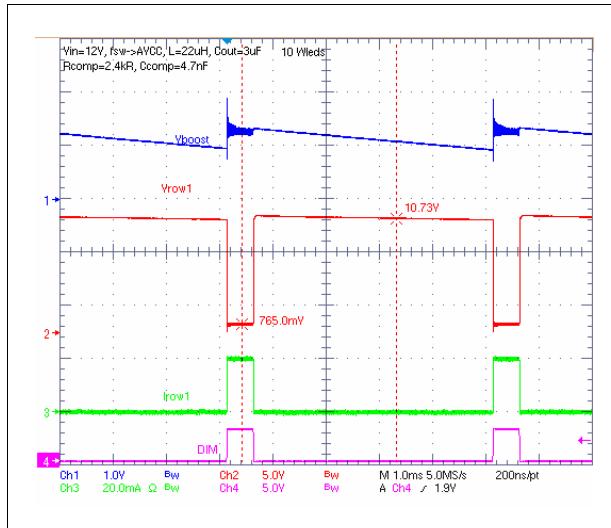
**Figure 35. Output voltage ripple @
 $f_{DIM} = 200$ Hz, D = 50%**



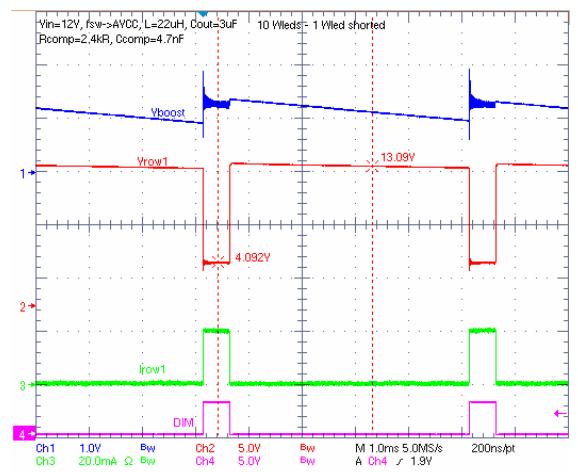
**Figure 36. Output voltage ripple @
 $f_{DIM} = 200$ Hz, D = 80%**



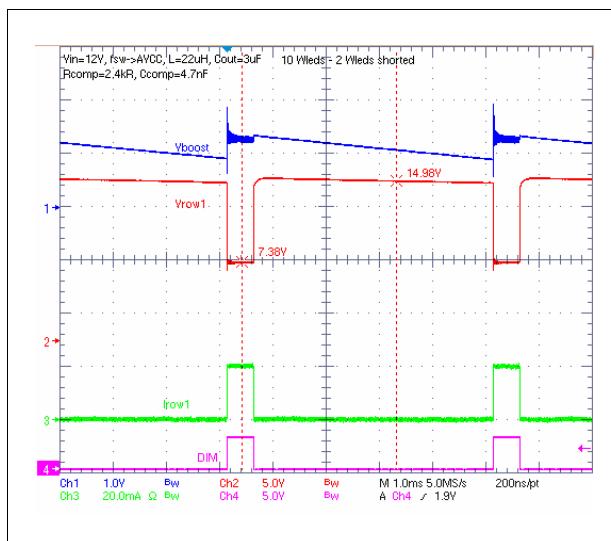
**Figure 37. Shorted LED protection
@ $f_{DIM} = 200$ Hz
all WLEDs connected**



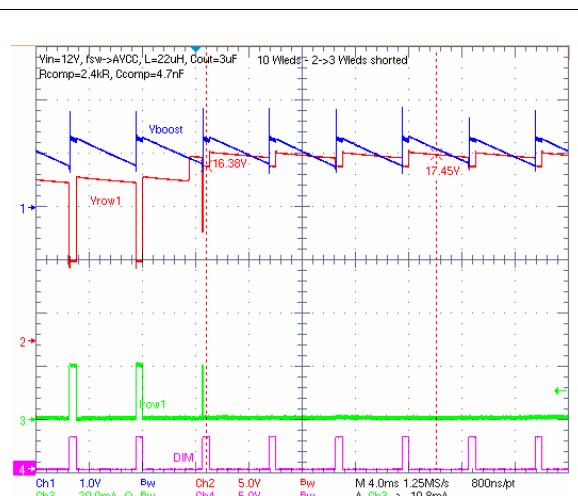
**Figure 38. Shorted LED protection
@ $f_{DIM} = 200$ Hz
1 WLED shorted**



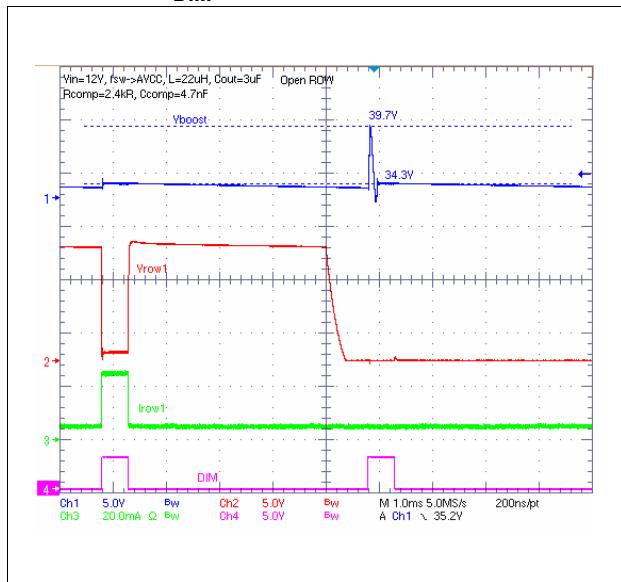
**Figure 39. Shorted LED protection
@ $f_{DIM} = 200$ Hz
2 WLEDs shorted**



**Figure 40. Shorted LED protection
@ $f_{DIM} = 200$ Hz
3 WLEDs shorted - ROW disabled**



**Figure 41. Open ROW detection @
 $f_{DIM} = 200$ Hz**



6 Block diagram

Figure 42. Simplified block diagram

