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PM6641

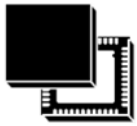
Monolithic VR for chipset and DDR2/3 supply for ultra-mobile PC (UMPC) applications

Features

- 0.8 V ±1% internal voltage reference
- 2.7 V to 5.5 V input voltage range
- Fast response, constant frequency, current mode control
- Three independent, adjustable, out-of-phase SMPS for DDR2/3 (VDDQ) and chipset supply
- Low noise DDR2/3 reference (VTTREF)
- ±2 Apk LDO for DDR2/3 termination (VTT) with foldback
- S0-S5 states compliant DDR2/3 section
- Active soft-end for all outputs
- Selectable tracking discharge for VDDQ
- Separate Power Good signals
- Pulse skipping at light load
- Programmable current limit and soft-start for all outputs
- Latched OVP, UVP protection
- Thermal protection

Applications

- DDR2/3 memory and chipset supply
- UMPC and portable equipment
- Handheld and PDAs



VFQFPN-48 7x7 mm

Description

The PM6641 is a monolithic voltage regulator module specifically designed to supply DDR2/3 memory and chipset in ultra-mobile PC and real estate constrained portable systems.

It integrates three independent, adjustable, constant frequency buck converters, a ±2 Apk low drop-out (LDO) linear regulator and a ±15 mA low noise buffered reference.

Each regulator provides basic UV and OV protections, programmable soft-start and current limit and active soft-end.

Pulse-skipping technique is performed to increase efficiency at very light load.

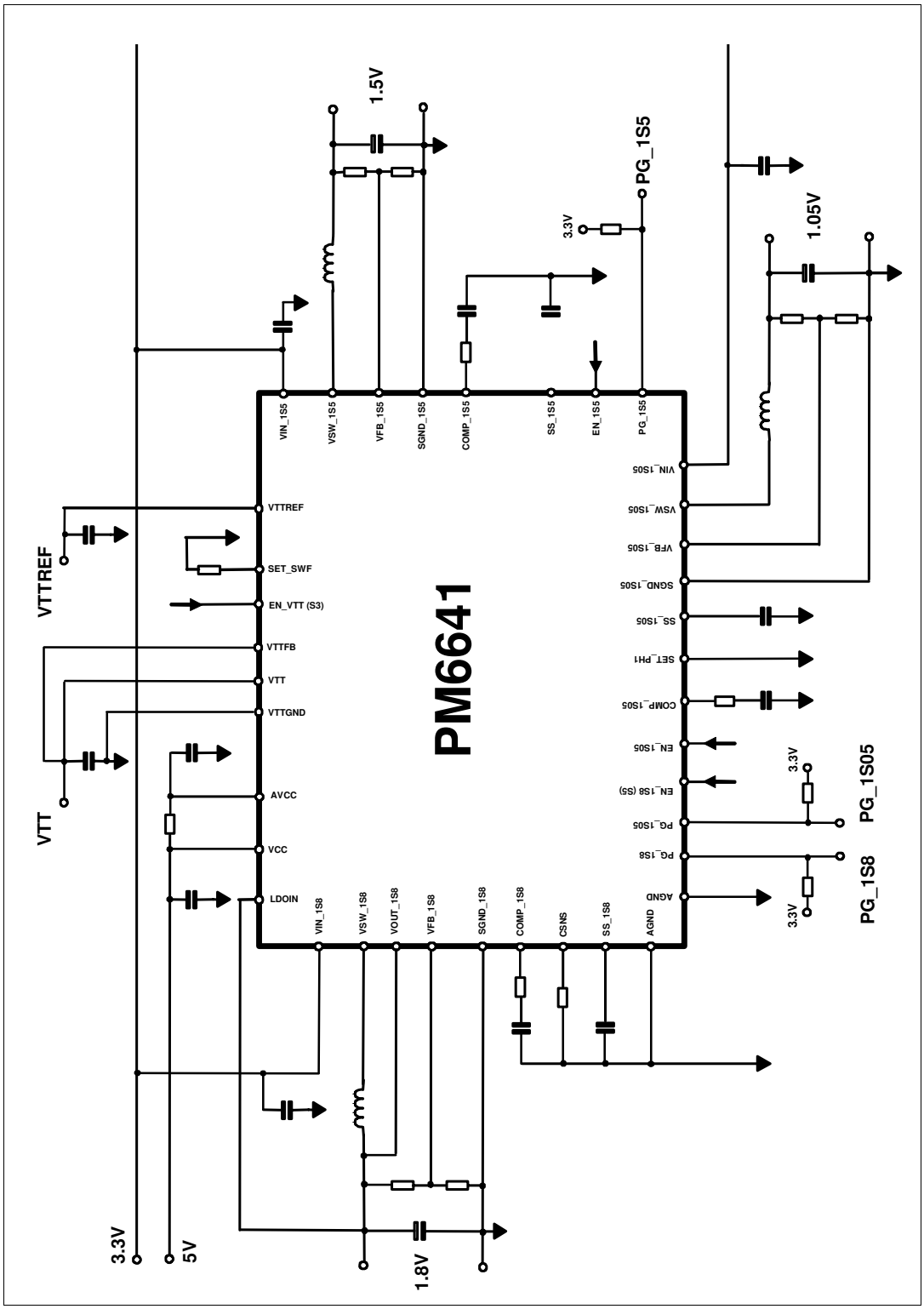
Table 1. Device summary

Order codes	Package	Packaging
PM6641	VFQFPN-48 7x7 (exposed pad)	Tray
PM6641TR		Tape and reel

Contents

1 Typical application circuit

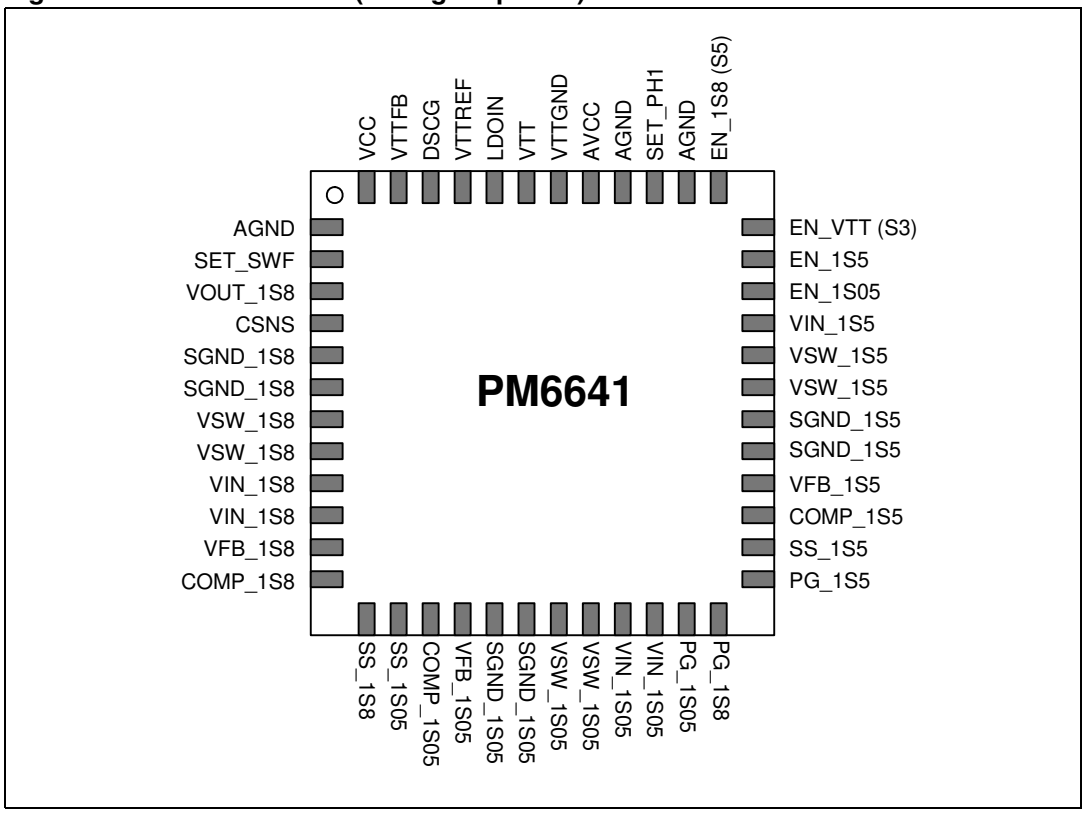
Figure 1. Application circuit



2 Pin settings

2.1 Connections

Figure 2. Pin connection (through top view)



2.2 Pin description

Table 2. Pin functions

n°	Pin	Function
1	AGND	Analog and signal ground.
2	SET_SWF	Switching frequency setting input. See *Chapter 7.8: Switching frequency selection on page 29*
3	VOUT_1S8	VDDQ/2 divider input and discharge path for 1.8 V rail.
4	CSNS	Current limit setting input for all rails. See *Chapter 7.10: Peak current limit on page 31*
5	SGND_1S8	Switcher power ground for 1.8 V rail.
6	SGND_1S8	Switcher power ground for 1.8 V rail.
7	VSW_1S8	Switch node for 1.8 V rail.
8	VSW_1S8	Switch node for 1.8 V rail.
9	VIN_1S8	Power supply input for 1.8 V rail.
10	VIN_1S8	Power supply input for 1.8 V rail.
11	VFB_1S8	Feedback input for 1.8 V rail. See *Chapter 7.5: Output voltage divider on page 27*
12	COMP_1S8	Loop compensation output for 1.8 V rail. See *Chapter 7.3: SW regulators control loop on page 24* and *Chapter 8.4: SW regulator compensation components selection on page 38* sections for details.
13	SS_1S8	Positive terminal of the external soft-start capacitor for 1.8 V rail. See *Chapter 7.6: Outputs soft-start on page 28* section for details.
14	SS_1S05	Positive terminal of the external soft-start capacitor for 1.05 V rail. See *Chapter 7.6: Outputs soft-start on page 28* section for details.
15	COMP_1S05	Loop compensation output for 1.05 V rail. See *Chapter 7.3: SW regulators control loop on page 24* and *Chapter 8.4: SW regulator compensation components selection on page 38* for details.
16	VFB_1S05	Feedback input for 1.05 V rail. See *Chapter 7.5: Output voltage divider on page 27* section for details
17	SGND_1S05	Switcher power ground for 1.05 V rail.
18	SGND_1S05	Switcher power ground for 1.05 V rail.
19	VSW_1S05	Switch node for 1.05 V rail.
20	VSW_1S05	Switch node for 1.05 V rail.
21	VIN_1S05	Power supply input for 1.05 V rail.
22	VIN_1S05	Power supply input for 1.05 V rail.
23	PG_1S05	Power Good signal for 1.05 V rail. Open drain. See *Chapter 7.2: Chipset supply on page 22* section for details.
24	PG_1S8	Power Good signal for 1.8 V rail. Open drain. See *Chapter 7.1.1: VDDQ switching regulator on page 20* section for details.
25	PG_1S5	Power Good signal for 1.5 V rail. Open drain. See *Chapter 7.2: Chipset supply on page 22* section for details.

Table 2. Pin functions (continued)

n°	Pin	Function
26	SS_1S5	Positive terminal of the external soft-start capacitor for 1.5 V rail. See *Chapter 7.6: Outputs soft-start on page 28* section for details.
27	COMP_1S5	Loop compensation output for 1.5 V rail. *Chapter 7.3: SW regulators control loop on page 24* and *Chapter 8.4: SW regulator compensation components selection on page 38* sections for details.
28	VFB_1S5	Feedback input for 1.5 V rail. See *Chapter 7.5: Output voltage divider on page 27* section for details
29	SGND_1S5	Switcher power ground for 1.5 V rail.
30	SGND_1S5	Switcher power ground for 1.5 V rail.
31	VSW_1S5	Switch node for 1.5 V rail.
32	VSW_1S5	Switch node for 1.5 V rail.
33	VIN_1S5	Power supply input for 1.5 V rail.
34	EN_1S05	Enable input for 1.05 V rail.
35	EN_1S5	Enable input for 1.5 V rail.
36	EN_VTT	Enable input for VTT rail. High in S0 system states. See *Chapter 7.1.4: S3 and S5 power management pins on page 22* section for details.
37	EN_1S8	Enable input for 1.8 V (VDDQ) rail. High in S0-S3 system states. See *Chapter 7.1.4: S3 and S5 power management pins on page 22* section for details.
38	AGND	Analog and signal ground.
39	SET_PH1	Switching regulator phase control. See *Chapter 7.9: Phase management on page 30* section for details.
40	AGND	Analog and signal ground.
41	AVCC	Analog circuitry supply. Connect to +5 V by a simple RC filter.
42	VTTGND	LDO linear regulator power ground.
43	VTT	LDO linear regulator output. DDR2-3 termination voltage. See *Chapter 7.1: Memory supply on page 20* and *Chapter 7.1.2: VTT LDO and VTTREF buffered reference on page 21* sections for details.
44	LDOIN	LDO linear regulator input. Typically connected to the 1.8 V rail.
45	VTTREF	Reference voltage buffer output. See *Chapter 7.1: Memory supply on page 20* and *Chapter 7.1.2: VTT LDO and VTTREF buffered reference on page 21* sections for details.
46	DSCG	Tracking/non-tracking discharge selection for DDR2-3 section. See *Chapter 7.7: Outputs soft-end on page 29* section for details.
47	VTTFB	Feedback input for VTT linear regulator output.
48	VCC	+5 V switching circuitry supply. Bypass to AGND by a 100 nF capacitor.

3 Electrical data

3.1 Maximum rating

Table 3. Absolute maximum ratings (1)

Symbol	Parameter		Value	Unit
V_{VIN}	VIN_x to SGND_x	$V_{IN} = V_{AVCC}$ $V_{VCC} = V_{AVCC}$	-0.3 to 6	V
V_{VCC}	VCC to AGND or SGND_x			
V_{AVCC}	AVCC to AGND or SGND_x			
	AGND to SGND_x		-0.3 to 0.3	
	VTTGND to SGND_x			
V_{VSW}	VSW_x to SGND_x		-0.3 to 6	
	VSW_x to AGND			
	CSNS, PG_x, EN_x, DSCG, COMP_x, VFB_x, SS_x, SET_SWF, SET_PH1, VOUT_1S8 to AGND		-0.3 to V_{AVCC} + 0.3	
	VTT, VTTREF, VTTFB to AGND			
	LDOIN, VTT, VTTREF, VTTFB to VTTGND			
P_{TOT}	Power dissipation @ T_A = 25 °C		4	W

1. Free air operating conditions unless otherwise specified. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	25	°C/W
T_{STG}	Storage temperature range	-50 to 150	°C
T_A	Operating ambient temperature range	-40 to 85	°C
T_J	Junction operating temperature range	-40 to 125	°C

3.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Values			Unit
		Min	Typ	Max	
V_{AVCC}	AVCC voltage range	4.5		5.5	V
V_{VCC}	VCC IC supply voltage	4.5		V_{AVCC}	
V_{IN}	VIN_x input voltage range	2.7		V_{VCC}	

4 Electrical characteristics

T_A = 0 °C to 85 °C, AVCC = 5 V, VCC = 5 V, VIN_x = 3.3 V and LDOIN connected to 1.8 V output if not otherwise specified [(a)].

Table 6. Electrical characteristics

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
Supply section all rails						
I_{CC}	AVCC+VCC operating current	V_{VCC} = +5 V, all switching regulators active without load			3	mA
I_{SHDN}	Total shutdown current into VIN_x + AVCC + VCC pins	V_{IN} = V_{AVCC} = V_{VCC} = +5 V, all EN_x low			10	µA
$UVLO_{th}$	AVCC under voltage lockout upper threshold		4.0	4.1	4.35	V
	AVCC under voltage lockout lower threshold		3.6	3.9	4.0	
	UVLO hysteresis		100			mV
Error amplifier, FB AND SS – all rails						
V_{REF}	Error amplifier reference voltage	V_{AVCC} = V_{VCC} = 5 V	792	800	808	mV
I_{FB}	FB input bias current	VFB_X = 0.8 V			25	nA
I_{SS}	Soft-start current	V_{SS_X} = 0.4 V		10		µA
Oscillator frequency						
f_{SW}	Switching frequency	R_{SETSWF} = 140 kΩ		500		kHz
		SET_SWF to VCC	675	750	825	
		R_{SETSWF} = 70 kΩ		1000		
Comp all rails						
g_m	COMP_x transconductance			300		µS
UVP/OVP protections and PGOOD signal (SMPS only) all rails						
OVP_{th}	Overvoltage threshold		116	120	124	%
UVP_{th}	Undervoltage threshold		56	60	64	
PG_{th}	Power good upper threshold		106	110	115	
	Power Good lower threshold		86	90	94	
$I_{PG,LEAK}$	PG_x outputs leakeage current	PG_x tied to +5 V			1	µA
$V_{PG,LOW}$	PG_x outputs low level	V_{FB_X} = 0.6 V or 1V, I_{PG_X} = 2 mA			250	mV

a. All parameters at operating temperature extremes are guaranteed by design and statistical analysis (not production tested).

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Values			Unit
				Min	Typ	Max	
Thermal shutdown							
T_{SHDN}	Thermal shutdown threshold				150		°C
	Thermal shutdown hysteresis				15		
Switching node – chipset 1.5 V rail							
t_{Onmin}	Minimum on-time				200		ns
$R_{DSon,HS}$	High side PMOS Ron				150	220	mΩ
$R_{DSon,LS}$	Low side NMOS Ron				100	160	
I_{INLEAK}	VIN_1S5 leakage current	V_{AVCC} = V_{VCC} = +5 V, all EN_1S5 low	V_{IN} = +5 V			1	µA
			V_{IN} = +3.3 V				
	Peak current limit	R_{CSNS} = 50 kΩ			3.9		A
Soft-end section – chipset 1.5 V rail							
	Discharge resistance				25		Ω
	LS turn-on VFB_1SX threshold with internal divider	VFB_S1X to OUT_X			0.29		V
	LS turn-on VFB_1SX threshold with external divider	VFB_S1X to external divider			0.16		
Power management section – chipset 1.5 V rail							
	EN_1S5 turn-off level	V_{AVCC} = 5 V		0.8			V
	EN_1S5 turn-on level					2	
Switching node – chipset 1.05 V rail							
t_{Onmin}	Minimum on-time				180		ns
$R_{DSon,HS}$	High side PMOS Ron				100	160	mΩ
$R_{DSon,LS}$	Low side NMOS Ron				70	110	
I_{INLEAK}	VIN_1S05 leakage current	V_{AVCC} = V_{VCC} = +5 V, all EN_1S05 low	V_{IN} = +5 V			1	µA
			V_{IN} = +3.3 V			1	
	Peak current limit	R_{CSNS} = 50 kΩ			5.1		A
Soft end section – chipset 1.05 V rail							
	Discharge resistance				25		Ω

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Values			Unit
				Min	Typ	Max	
	LS turn-on VFB_1SX threshold with internal divider	VFB_S1X to OUT_X			0.2		V
	LS turn-on VFB_1SX threshold with external divider	VFB_S1X to external divider			0.16		
Power management section – chipset 1.05 V rail							
	EN_1S05 turn-off level	V_{AVCC} = +5 V		0.8			V
	EN_1S05 turn-on level					2	
Switching node – DDR2/3 rails							
t_{Onmin}	Minimum on-time				200		ns
$R_{DSon,HS}$	High side PMOS Ron				90	130	mΩ
$R_{DSon,LS}$	Low side NMOS Ron				80	120	
I_{INLEAK}	VIN_1S8 leakage current	V_{AVCC} = V_{VCC} = 5 V, all EN_1S8 low	V_{IN} = +5 V			1	µA
			V_{IN} = +3.3 V			1	
	Peak current limit	R_{CSNS} = 50 kΩ			6.1		A
Soft-end section – DDR2/3 rails							
	VDDQ discharge resistance in non-tracking discharge mode				25		Ω
	VTTREF discharge resistance in non-tracking discharge mode				200		Ω
	VTTFB discharge resistance in non-tracking discharge mode				40		Ω
	V_{FB_1SX} threshold for final tracking/Non-tracking discharge transition with internal divider	VFB_S1X to OUT_X			0.340		V
	V_{FB_1SX} threshold for final tracking/Non-tracking discharge transition with external divider	VFB_S1X to external divider			0.160		V
Power management section – DDR2/3 rails							
	DSCG turn-off level	V_{AVCC} = +5 V				1.5	V
	DSCG turn-on level			3.5			
	EN_1S8 (S5), EN_VTT (S3) Turn-Off Level	V_{AVCC} = +5 V		0.8			
	EN_1S8 (S5), EN_VTT (S3) Turn-On Level					2	

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
V_{TT} LDO section – DDR2/3 rails						
PG_VTT_TH	Power Good upper threshold		106	110	114	%
	Power Good lower threshold		86	90	94	%
$I_{LDOIN,ON}$	LDO input bias current in full-ON state	EN_1S8 = EN_VTT = +5 V, no load on VTT		1	10	µA
$I_{LDOIN,STR}$	LDO input bias current in suspend-to-RAM state	EN_1S8 = +5 V, EN_VTT = 0 V, no load on VTT			10	
$I_{LDOIN,STD}$	LDO input bias current in suspend-to-disk state	EN_1S8 = EN_VTT = 0 V, no load on VTT			3	
$I_{VTTFB, BIAS}$	VTTFB bias current	EN_1S8 = EN_VTT = +5 V, $V_{VTTFB} = V_{VOUT\_1S8}/2$			1	µA
$I_{VTTFB, LEAK}$	VTTFB leakage current	EN_1S8 = +5 V, EN_VTT = 0 V, $V_{VTTFB} = V_{VOUT\_1S8}/2$			1	
$I_{VTT,LEAK}$	VTT leakage current	EN_1S8 = +5 V, EN_VTT = 0 V, $V_{VTT} = V_{VOUT\_1S8}/2$	-10		10	
V_{VTT}	LDO linear regulator output voltage (DDR2)	EN_1S8 = EN_VTT = +5 V, I_{VTT} 0 A, V_{LDOIN} = 1.8 V		0.9		V
	LDO linear regulator output voltage (DDR3)	EN_1S8 = EN_VTT = +5 V, I_{VTT} = 0 A, V_{LDOIN} = 1.5 V		0.75		
	LDO output accuracy respect to VTTREF, V_{LDOIN} =1.8 V	EN_1S8 = EN_VTT = +5 V, -1 mA < I_{VTT} < 1 mA	-20		20	mV
		EN_1S8 = EN_VTT = +5 V, -1 A < I_{VTT} < 1 A	-25		25	
		EN_1S8 = EN_VTT = +5 V, -2 A < I_{VTT} < 2 A	-35		35	
$I_{VTT,CL}$	LDO source current limit	V_{VTT} < 1.10*(V_{VOUT_1S8} /2)	2	2.3	3	A
		V_{VTT} > 1.10*(V_{VOUT_1S8} /2)	1	1.25	1.5	
	LDO sink current limit	V_{VTT} > 0.90*(V_{VOUT_1S8} /2)	-3	-2.3	-2	
		V_{VTT} < 0.90*(V_{VOUT_1S8} /2)	-1.5	-1.25	-1	
VTTREF section – DDR2/3 rails						
V_{VTTREF}	VTTREF output voltage	I_{VTTREF} = 0A, V_{VOUT_1S8} = 1.8 V		0.9		V
	VTTREF output voltage accuracy relative to $V_{VOUT\_1S8}/2$	-15 mA < I_{VTTREF} < +15 mA, V_{VOUT_1S8} = 1.8 V	-2		2	%
I_{VTTREF}	VTTREF short circuit source current	V_{VOUT_1S8} = 1.8 V, V_{VTTREF} = 0 V		40		mA
	VTTREF short circuit sink current	V_{VOUT_1S8} = 1.8 V, V_{VTTREF} = 1.8 V		-40		

5 Typical operating characteristics

Figure 3. VDDQ and VTT soft-start without load

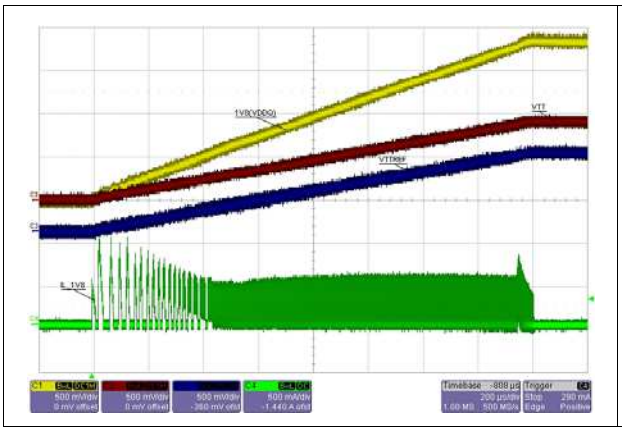


Figure 4. VDDQ and VTT soft-start with AVG load

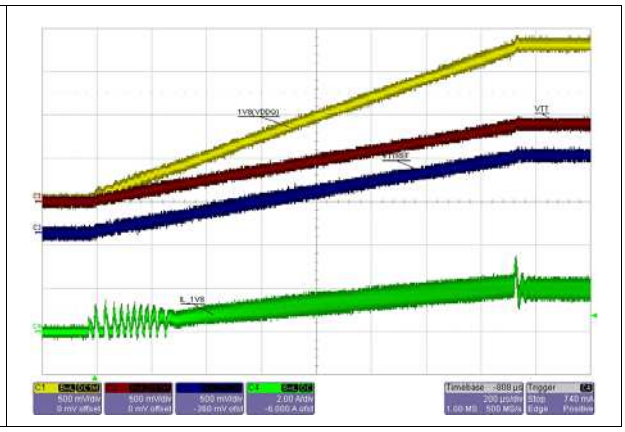


Figure 5. 1V5 soft-start without load

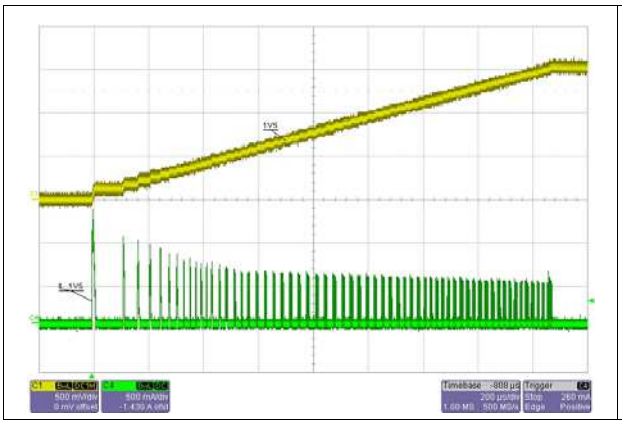


Figure 6. 1V5 soft-start with load

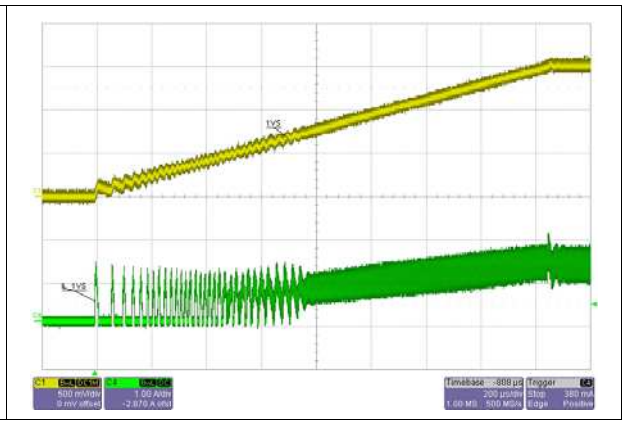


Figure 7. 1V05 soft-start without load

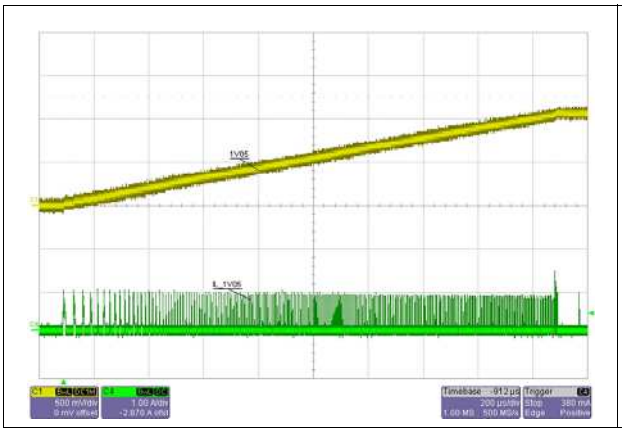


Figure 8. 1V05 soft-start without load

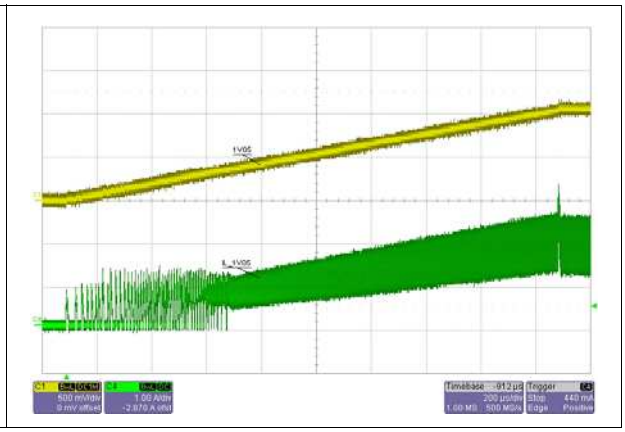


Figure 9. VDDQ output ripple and phase @ AVG current

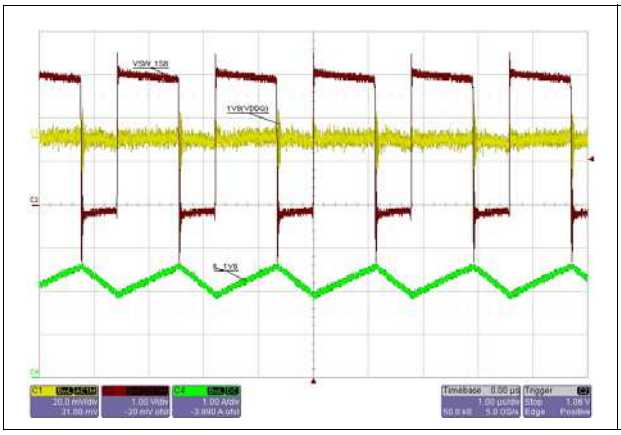


Figure 10. VTT, VTTREF output ripple @ AVG current

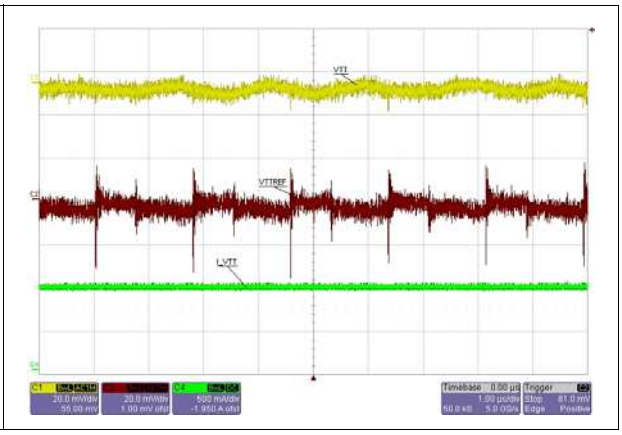


Figure 11. 1V5 output ripple and phase @ AVG current

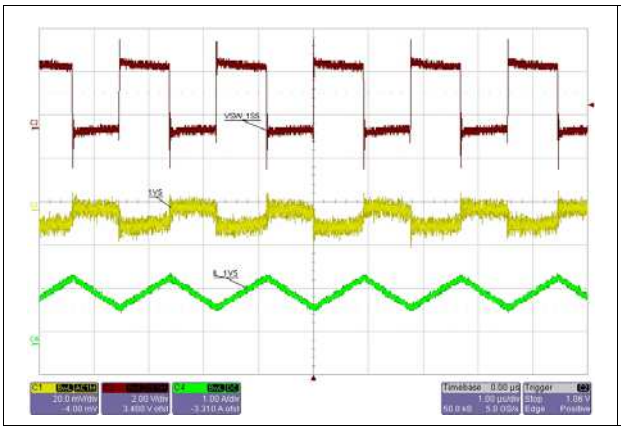


Figure 12. 1V05 output ripple and phase @ AVG current

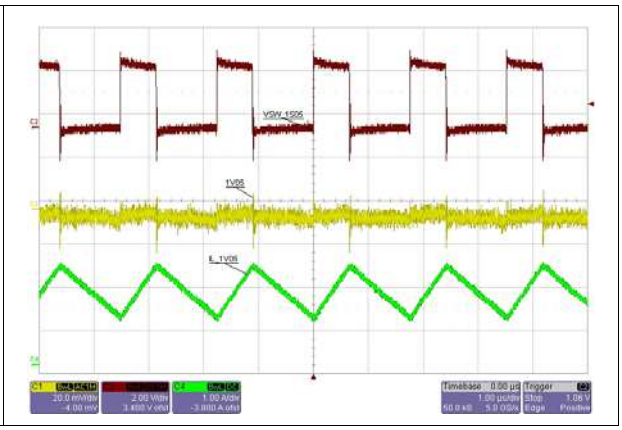


Figure 13. SW reg. efficiency @ V_{IN} = 3.3 V, F_{SW} = 600 kHz

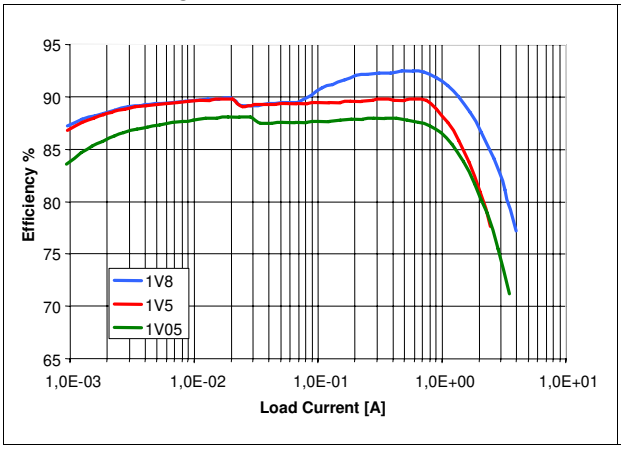


Figure 14. VDDQ (1.8 V) load regulation

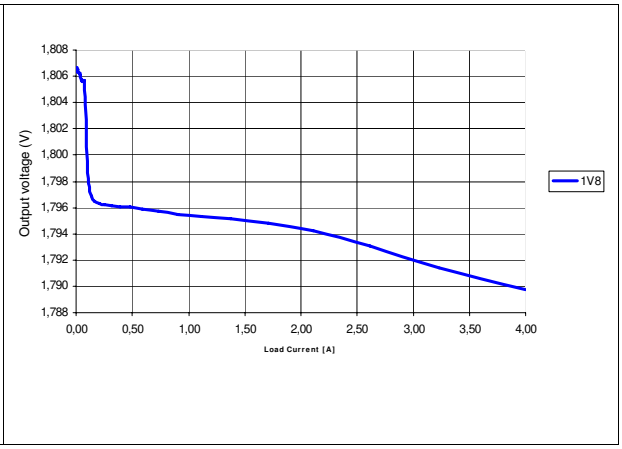


Figure 15. 1.5 V load regulation

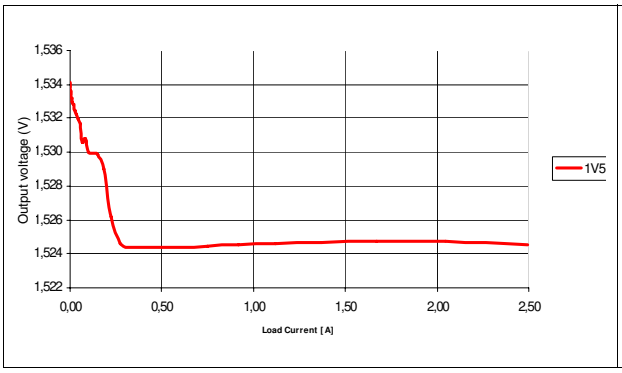


Figure 16. 1.05 V load regulation

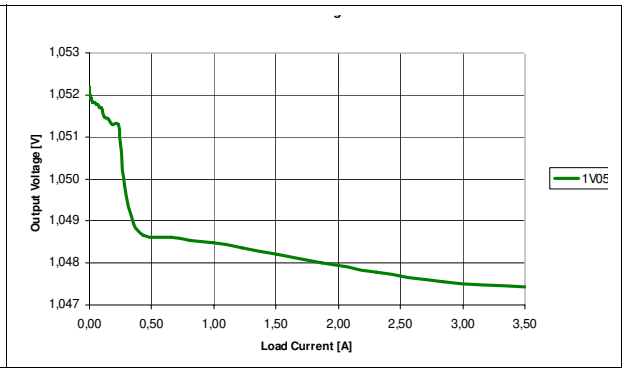


Figure 17. VDDQ (1.8 V) load transient: 0-AVG

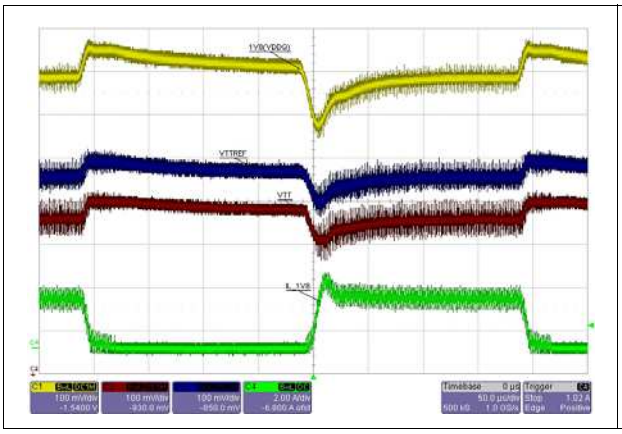


Figure 18. VTT load transient: -1 A +1 A

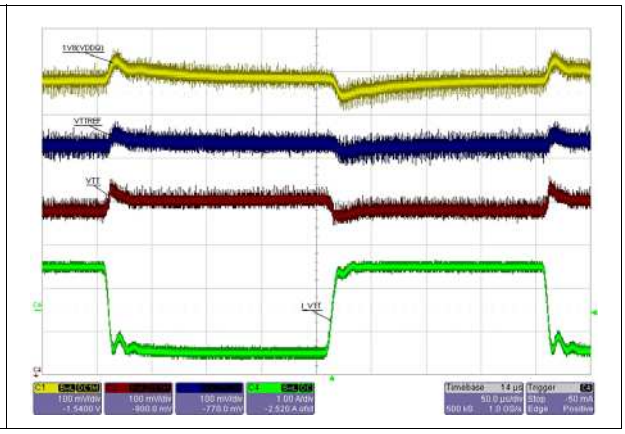


Figure 19. 1V5 load transient: 0-AVG

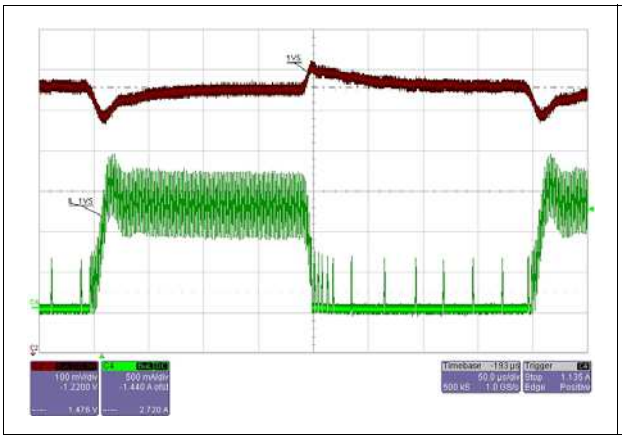


Figure 20. 1V05 load transient: 0-AVG

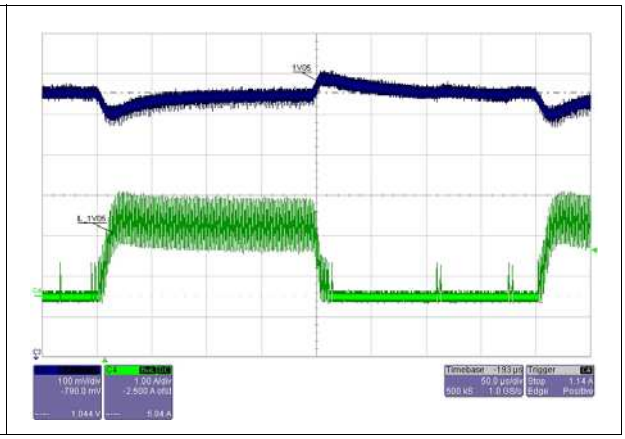


Figure 21. VDDQ e VTT soft-end with DSCG = AVCC

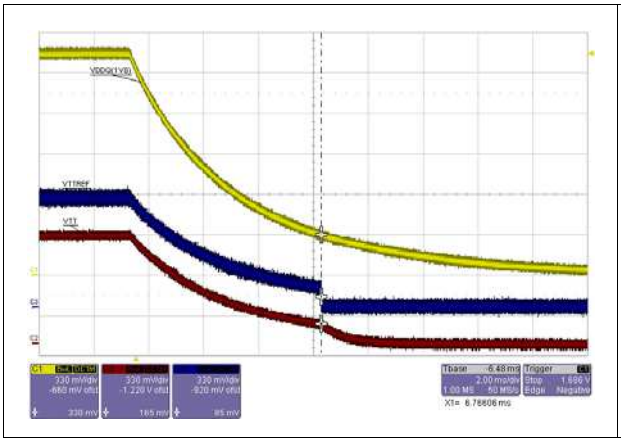


Figure 22. VDDQ e VTT soft-end with DSCG = AGND

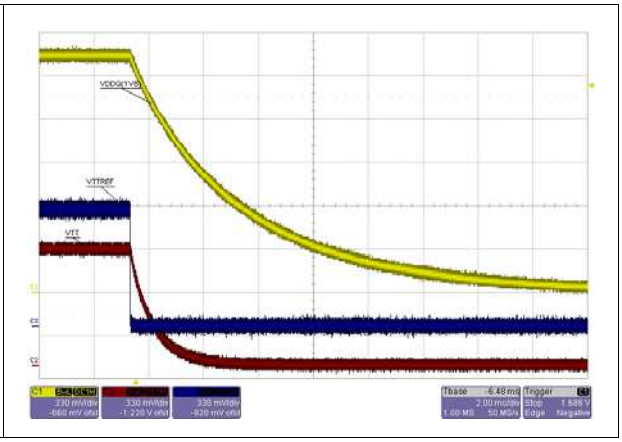


Figure 23. Current limit

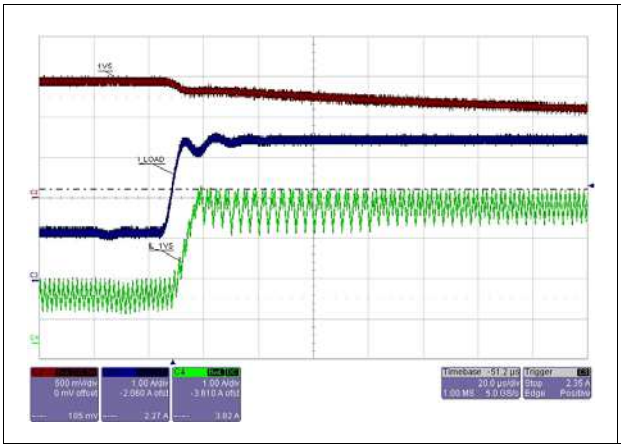


Figure 24. Soft-OV (1V05)

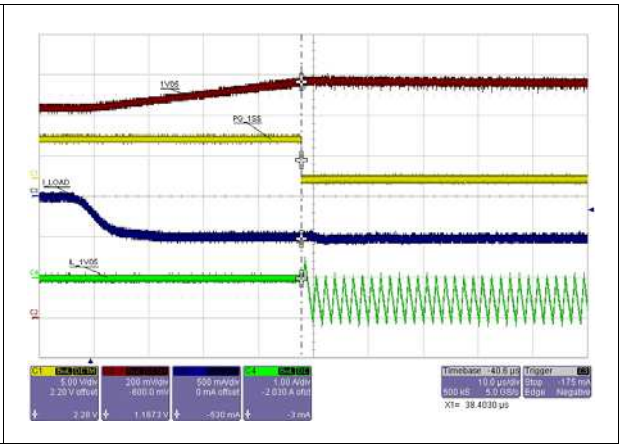


Figure 25. Output OV (1V5) @ R_{CSNS} = 1 MΩ

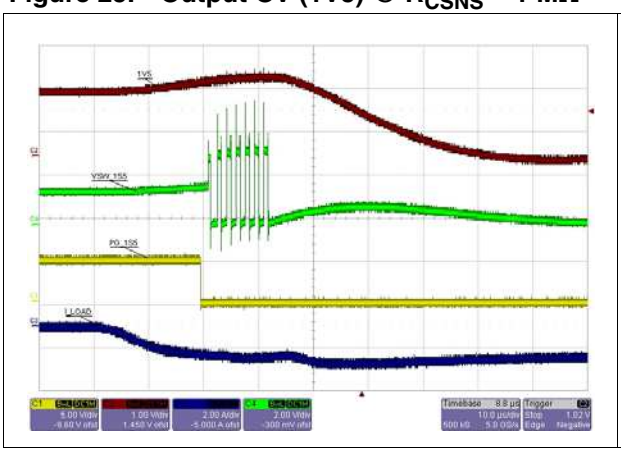
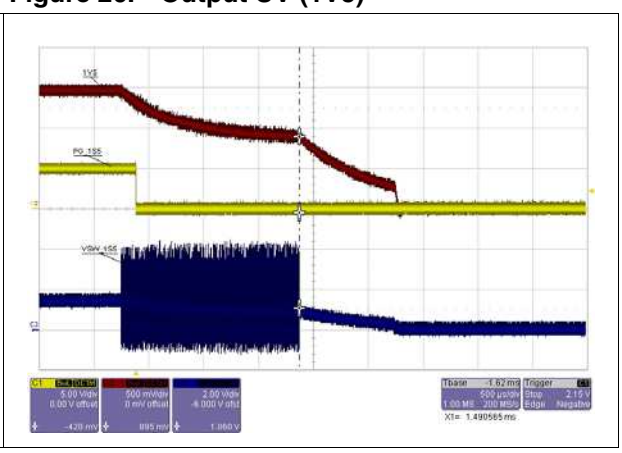


Figure 26. Output UV (1V5)



Note: All the above measures and screen captures are based on PM6641EVAL demonstration board. Refer to PM6641 demonstration kit for details.

6 Block diagram

Figure 27. Functional and block diagram

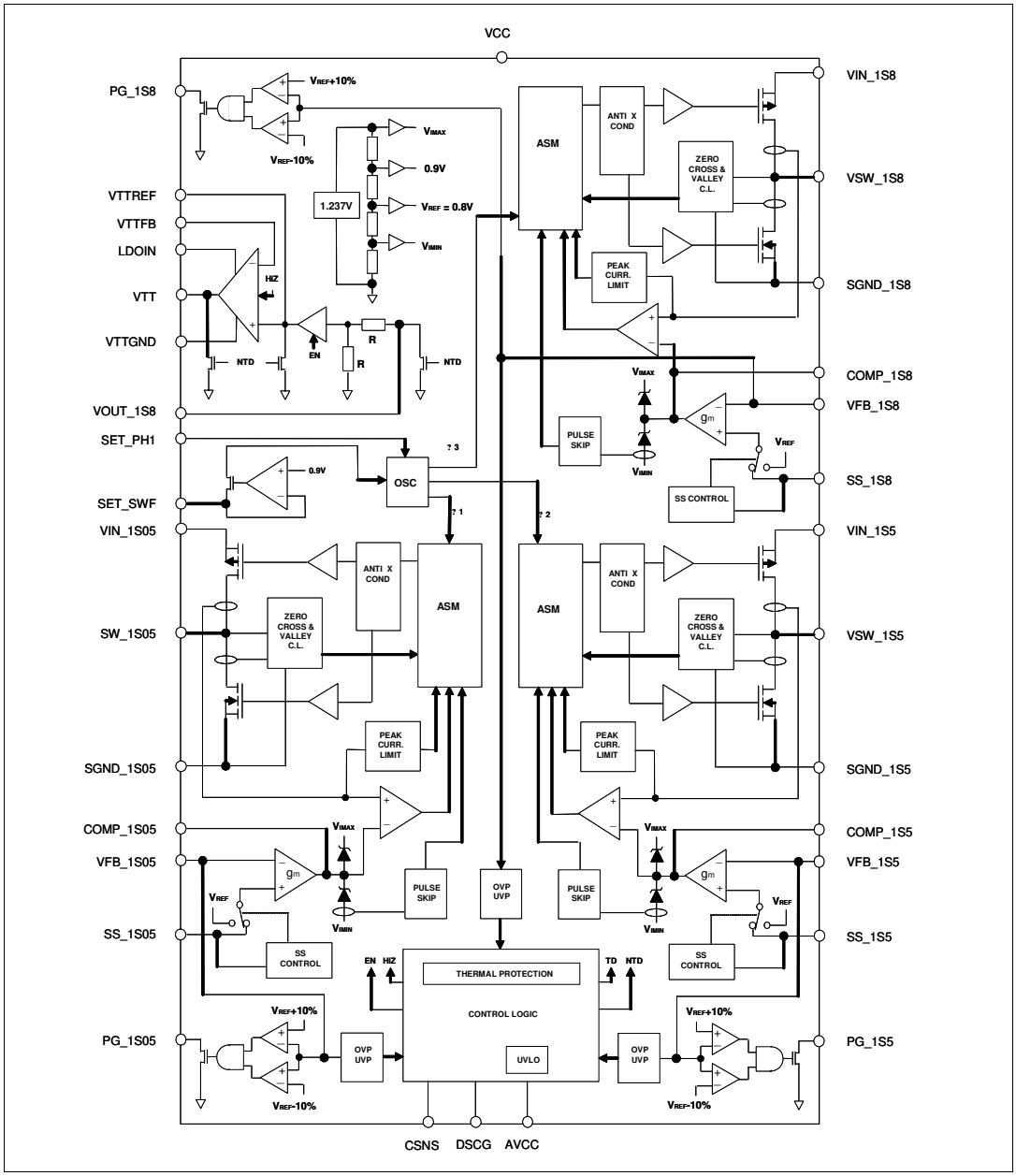


Table 7. Legend

TD	Tracking discharge enable
NTD	Non-tracking discharge enable
EN	VTTREF buffer enable
HiZ	LDO high impedance mode enable

7 Device description

The PM6641 is an integrated voltage regulator module designed to supply DDR2/3 memory and chipset I/O in real estate constrained portable equipment and ultra-mobile PCs. The device consists of three buck regulators (two for chipset supply and one for main DDR supply), a low drop-out (LDO) linear regulator capable of ±2 Apk (DDR termination voltage) and a low noise buffered reference (DDR input buffer reference). It has been developed for single-series Li-Ion battery stack powered equipment, allowing an input power supply from 2.7 V up to 5.5 V.

The PM6641 provides a compact solution by integrating DDR and chipset voltage regulators on a single IC with internal power MOSFETs and requiring a minimum number of external components. All its buck regulators are based on a current-mode control scheme with integrated features to guarantee stability and fast load transient response. Each regulator output voltage can be adjusted or a pre-fixed output voltage can be chosen, if external components are unwanted. Each switching regulator has independent programmable soft-start, to reduce inrush current, and output soft-end, to avoid inductor and MOSFETs high peak current.

Other buck regulators features include output over-voltage and under-voltage protections, programmable current limit and output Power Good signals high efficiency is achieved over a wide range of load conditions by using a pulse-skipping technique at light load.

The PM6641 can detect the AVCC pin under-voltage through the under-voltage lock-out (UVLO) block and it is able to limit its internal temperature through its auto-recovery thermal shutdown.

The switching frequency of the buck controllers can be set in the range 500 kHz-1 MHz with an external resistor or can be set equal to 750 kHz without external components use. All buck regulators work at the same switching frequency with selectable phase shift.

The regulators can support both electrolytic and ceramic output capacitors because no minimum output voltage ripple is required for stability purposes.

The PM6641 is provided in a QFN7x7 mm 48-pin lead-free package.

7.1 Memory supply

The DDR2/3 section of PM6641 is based on the VDDQ rail, the VTT termination rail and the VTTREF reference voltage buffer.

The VDDQ rail is provided by a step-down switching regulator whose output voltage, by default, is set to 1.8 V, in order to be compliant with DDR2 JEDEC specs. The output voltage can also be adjusted using an external resistor divider. This rail performs latched output under-voltage and over-voltage and auto-recovery current limit, without requiring external sensing resistor.

The VTT termination rail is supplied by a low drop-out (LDO) linear regulator, able to sink and source up to 2 A peak current. This regulator follows the half of the VDDQ rail and is a replica of the VTTREF reference voltage buffer. When LDOIN is directly supplied by VDDQ, i.e. the PM6641 1S8 rail, VTT and VDDQ can perform the so called tracking discharge, in compliance with the JEDEC specs, as described in the following section. If higher efficiency is required, VTT can be supplied by a lower voltage rail. An output capacitor of at least 20 µF is the only external component required.

The VTTREF reference voltage buffer is always in tracking with the half of VDDQ and is able to sink and source up to 15 mA with an accuracy of ±2% relative to VDDQ half. A 10 nF up to 100 nF bypass capacitor for stability purposes is required.

7.1.1 VDDQ switching regulator

The VDDQ rail is provided by a constant frequency current-mode buck regulator, whose frequency is set by inserting an external resistor between SET_SWF pin and AGND (see *Chapter 7.8: Switching frequency selection on page 29* section for details). The output voltage can easily be set to 1.8 V by connecting the feedback pin VFB_1S8 directly to the output rail, avoiding the use of external components. However, if a different output voltage is desired, the VFB_1S8 pin must be connected to the central tap of a resistor divider.
The output voltage can be adjusted from 0.8 V up to the input voltage value, decreased by a drop due to the high-side MOSFET on resistance.

(see *Chapter 7.5: Output voltage divider on page 27* section for details).

The control loop needs to be compensated by inserting a resistor-capacitor series connected between the COMP_1S8 pin and ground; if electrolytic capacitor with relevant equivalent series resistance (ESR) are used, an additional capacitor between the COMP_1S8 pin and ground can be useful (see *Chapter 7.3: SW regulators control loop on page 24* section for details). The classical slope compensation is internally implemented and no external components are required.

The internal high-side PMOS and low-side NMOS allow the regulator to source an average current of 2.8 A and a peak current of 5 A. The peak current limit protection is performed by sensing the internal high side MOSFET current and can be decreased by inserting an external resistor between CSNS pin and AGND (see *Chapter 7.10: Peak current limit on page 31* section for details).

This 1S8 rail is able to protect the load from Over-Voltage and Under-Voltage protection, which avoid the output to be higher than 120% or lower than 60% of the nominal value (see *Chapter 7.11.1: Output overvoltage on page 33* and *Chapter 7.11.2: Output under voltage on page 33* section for details).

When the EN_1S8 pin goes high the VDDQ rail is turned on and the output voltage soft-start is performed by slowly charging the rail output capacitor; this behavior is achieved because

the loop voltage reference is increased linearly from zero up to 0.8V in a long time (up to a couple of milliseconds) (see *Chapter 7.6: Outputs soft-start on page 28* for details).

When the EN_1S8 pin goes low, the VDDQ rail output capacitor is discharged through internal discharge MOSFET and, at the end of the capacitor discharge, the low side power MOSFET is eventually closed (see *Chapter 7.7: Outputs soft-end on page 29* for details).

The Power Good signal (PG_1S8 pin) is an open drain output, shorting the output to GND in the following conditions:

- When the 1.8 V rail output voltage is outside +/- 10% range from nominal value
- When a protection (UV, OV, thermal) has been triggered
- When the regulator is in soft-start.

When VDDQ and VTT rails are enabled, PG_1S8 is left floating and, as a consequence, pulled-up by the external pull-up resistor, if both the rails are inside +/- 10% range of nominal value. The PG_1S8 pin can sink current up to 4 mA when it's asserted low.

7.1.2 VTT LDO and VTTREF buffered reference

The PM6641 provides the required DDR2/3 reference voltage on VTTREF pin. The internal buffer tracks half the voltage on VOUT_1S8 pin and has a sink and source capability up to 15 mA with an accuracy of ±2% referred to the VDDQ half.

Higher currents rapidly deteriorate the output accuracy. A 10 nF to 100 nF (33 nF typical) bypass capacitor to SGND is required for stability.

The VTT low-drop-out linear regulator has been designed to sink and source up to 2 A peak current and 1 A continuously. The VTT voltage tracks VTTREF within ±35 mV. A remote voltage sensing pin (VTTFB) is provided to recovery voltage drops due to parasitic resistance. In DDR2/3 applications, the linear regulator input LDOIN is typically connected to VDDQ output; connecting LDOIN pin to a lower voltage (if available in the system) reduces the power dissipation of the LDO, but a minimum drop-out voltage must be guaranteed, depending on the maximum current expected.

A minimum output capacitance of 20 µF (2x10 µF or single 22 µF ceramic capacitors) is enough to assure stability and fast load transient response.

According to DDR2/3 JEDEC specifications, when the system enters the suspend-to-RAM state (S5 high and S3 low) the LDO output is left in high-impedance while VTTREF and VDDQ are still alive. When the suspend-to-disk state (S3 and S5 tied to ground) is entered, all outputs are actively discharged by a tracking or a non-tracking discharge as selected through the DSCG pin (see *Chapter 7.7: Outputs soft-end on page 29* for details).

7.1.3 VTT and VTTREF soft-start

Soft-start on VTT and VTTREF outputs is achieved by current clamping. The LDO linear regulator is provided of a current fold-back protection: when the output voltage exits the internal ±10% VTT-Good window, the output current is clamped at ±1 A. Re-entering VTT-Good window releases the current limit clamping. The fold-back mechanism naturally implements a two steps soft-start charging the output capacitors with a 1 A constant current.

Something similar occurs at VTTREF pin, where the output capacitor is smoothly charged at a fixed 40 mA (typ) current limit.

7.1.4 S3 and S5 power management pins

According to DDR2/3 memories supply requirements, the PM6641 can manage all S0 to S5 system states just connecting EN_VTT – EN_1S8 pins to their respective sleep-mode signals in the notebook's motherboard: connect EN_1S8 to S5 and EN_VTT to S3.

Keeping EN_VTT and EN_1S8 high, the S0 (full-on) state is decoded and the outputs are alive.

In S3 state (EN_1S8 = 1, EN_VTT = 0), the PM6641 maintains VDDQ and VTTREF outputs active and VTT output in high-impedance as needed.

In S4/S5 states (EN_1S8 = EN_VTT = 0) all outputs are turned off and, according to DSCG pin voltage, the proper Soft-End is performed (see *Chapter 7.7: Outputs soft-end on page 29* section for details).

The following table resumes the DDR power supply states.

Table 8. S3 and S5 sleep-states decoding

S3 (EN_VTT)	S5 (EN_1S8)	System state	VDDQ	VTTREF	VTT
1	1	S0 (Full-on)	On	On	On
0	1	S3 (Suspend-to-RAM)	On	On	Hi-Z
0	0	S4/S5 (Suspend-to-disk)	Off (Discharge)	Off (Discharge)	Off (Discharge)

7.2 Chipset supply

The chipset power supply section is based on two constant frequency current-mode buck regulators with a pre-fixed output voltage of 1.5 V and 1.05 V.

These two independent rails have programmable switching frequency, set by inserting an external resistor between SET_SWF pin and AGND. The PM6641 allows also to manage the switching regulators phases for 1.5 V, 1.05 V and 1.8 V (VDDQ) rails in order to limit the RMS input current (see *Chapter 7.8: Switching frequency selection on page 29* and *Chapter 7.9: Phase management on page 30* section for details).

The output voltages can easily be set to the pre-fixed value by connecting the feedback pins VFB_1S5 and VFB_1S05 directly to the respective output rail, avoiding the use of external components. However, if a different output voltage is desired, the feedback pins can be independently connected to the central tap of a resistor divider.

The output voltage can be adjusted from 0.8 V up to the input voltage value, decreased by a drop due to the high-side MOSFET on resistance.
(see *Chapter 7.5: Output voltage divider on page 27* section for details).
Both regulators are current-mode step-down switching regulators whose control loop needs to be compensated by inserting a resistor-capacitor series connected between the compensation pin (COMP_1S5 and COMP_1S05) and ground; if electrolytic capacitor with relevant equivalent series resistance (ESR) are used, an additional capacitor between this compensation pin and ground can be useful (see *Chapter 7.3: SW regulators control loop on page 24* section for details). The classical slope compensation, which allows the peak

current mode loop to avoid sub-harmonic instability with duty cycle greater than 50%, is internally implemented and no further external components are required.

The chipset supply is able to source the following average and peak currents, assuming 1 A peak-to-peak inductor current ripple:

Table 9. Chipset supply currents

Chipset supply rail [V]	Average current [A]	Peak current [A]
1.5	1.5	3.0
1.05	2.1	4.0

The peak current and the inductor ripple must be carefully evaluated in order to choose the right current limit protection; this feature is performed by sensing the internal high side MOSFET current and can be decreased by inserting an external resistor between CSNS pin and AGND (see *Chapter 7.10: Peak current limit on page 31* for details).

Both rails are able to protect the load from over-voltage and under-voltage protection, which avoid the output to be higher than 120% or lower than 60% of the nominal value (see *Chapter 7.11.1: Output overvoltage on page 33* and *Chapter 7.11.2: Output under voltage on page 33* section for details).

When the EN_1S5 or EN_1S05 pin goes high the respective rail is turned on and the output voltage soft-start is performed by slowly charging the rail output capacitor; this behavior is achieved because the loop voltage reference is increased linearly from zero up to 0.8V (see *Chapter 7.6: Outputs soft-start on page 28* section for details). When the EN_1S5 or EN_1S05 pin goes low, the respective rail output capacitor is discharged through internal discharge MOSFET and, at the end of the capacitor discharge, the low side power MOSFET is finally closed (see *Chapter 7.7: Outputs soft-end on page 29* section for details).

Each rail has a dedicated pin to assert if its output voltage is not in the power good window, i.e. if the output voltage drops 10% below or rises 10% above the nominal regulated value. These power good signals (PG_1S5 and PG_1S05 pins) are open drain outputs, tied to GND in the following conditions:

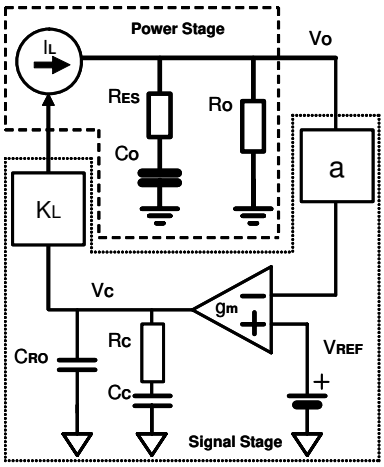
- When the rail output voltage is outside +/- 10% range from nominal value
- When a protection (UV, OV, thermal) has been triggered
- When the regulator is in soft-start.

The PG_1S5 and PG_1S05 pins can sink current up to 4 mA when it's asserted low.

7.3 SW regulators control loop

The PM6641 switching regulators are buck converters employing a constant frequency, peak current mode PWM control loop, as shown in the following figure:

Figure 28. SW regulator control loop



In the current mode constant frequency loop the power stage is represented by a controlled current generator feeding the power stage output capacitor and load. The equivalent transfer function is:

Equation 1

$$H(s) = \frac{V_O(s)}{I_L(s)} = \frac{(sC_OR_{ES} + 1)}{sC_O(R_{ES} + R_O) + 1}R_O$$

with Co and Res being the output capacitance and its equivalent series resistance and Ro representing the output load.

In order to obtain the typical integrative loop transfer function the signal stage must compensate for the power stage pole (due to the output capacitor and the load) and zero (above the loop bandwidth if ceramic output capacitors are selected). The signal stage transfer function is:

Equation 2

$$G(s) = g_m K_L \alpha \frac{sC_C R_C + 1}{sC_C\left(sC_{Ro}R_C + \frac{C_{Ro}}{C_C} + 1\right)}$$

Where g_M is the power stage transconductance, K_L is a design parameter and α is the gain due to the output resistor divider (0.8 V / Vout). The external compensation network (R_c, C_c and C_{RO}) introduces:

- One zero, to compensate the power stage pole:

$$C_C R_C = C_O(R_O + R_{ES})$$

- One pole in order to delete the static output voltage error;
- One pole, if necessary, in order to compensate the high frequency zero due to the output capacitor ESR:

$$C_{RO} R_C = C_O R_{ES}$$

The control loop gain is obtained by multiplying G(s) by H(s):

Equation 3

$$G_{LOOP}(s) = g_m K_L \alpha \frac{(sC_C R_C + 1)}{sC_C\left(sC_{Ro}R_C + \frac{C_{Ro}}{C_C} + 1\right)} \cdot \frac{(sC_O R_{ES} + 1)}{sC_O(R_{ES} + R_O) + 1} R_O$$

This model provides good results if the control loop cut-off frequency f_{CO} is lower than about fsw/10.