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PM6652

Single-phase controller for Intel® MVP 6.5 render voltage regulator, CPU and VR11 CPU

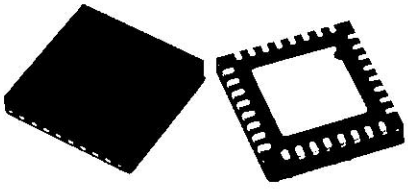
Datasheet – production data

Features

- 4.5 V to 36 V input voltage range
- 0.3 V to 1.5 V output voltage range
- IMVP6.5 GPU/CPU and VR11 CPU mode selection
- Very fast load transient response using constant-on-time loop control
- Remote voltage sensing
- Programmable droop function
- 7-bit dynamic voltage positioning (VID)
- Programmable PWM frequency
- Lossless current sense with inductor DCR
- Accurate inductor current sense with R_{SENSE}
- Negative current limit
- Boot diode embedded
- Latched OVP, UVP and overtemperature
- Pulse-skipping when suspend state is selected
- Output voltage ripple compensation
- Soft-start and soft-end
- Power good available
- Current monitor (IMON)
- Thermal throttling

Applications

- Intel mobile graphic core IMVP6.5
- Intel mobile CPU IMVP6.5
- Intel ATOM® VR11 based devices
- Notebook, netbook and nettop computers
- Handheld devices and PDAs



VFQFPN-32 5x5 mm

Description

The PM6652 is a single-phase, step-down SMPS controller with high precision 7-bit DAC. It has been designed to supply the CPU and the graphics core (render engine) of the Intel® mobile platform, according to Intel MVP6.5 specifications.

The PM6652 can also be configured to supply the 7-bit family, VR11 compliant, ATOM® processors.

The controller, based on constant on-time (COT) architecture, allows real-time dynamic switching of the core operating voltages and frequencies, working in both performance and suspend render states.

An embedded integrator control loop compensates the DC voltage error due to the output ripple.

The high efficiency at light load, achieved with pulse-skipping working mode, and the extremely low shutdown and quiescent adsorbed current, make the PM6652 the ideal choice in battery powered devices.

Table 1. Device summary

Order codes	Package	Packaging
PM6652	VFQFPN-32 5 x 5 mm (exposed pad)	Tray
PM6652TR		Tape and reel

Contents

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1 Typical application circuit

Figure 1. Typical application circuit - IMVP6.5 render core supply

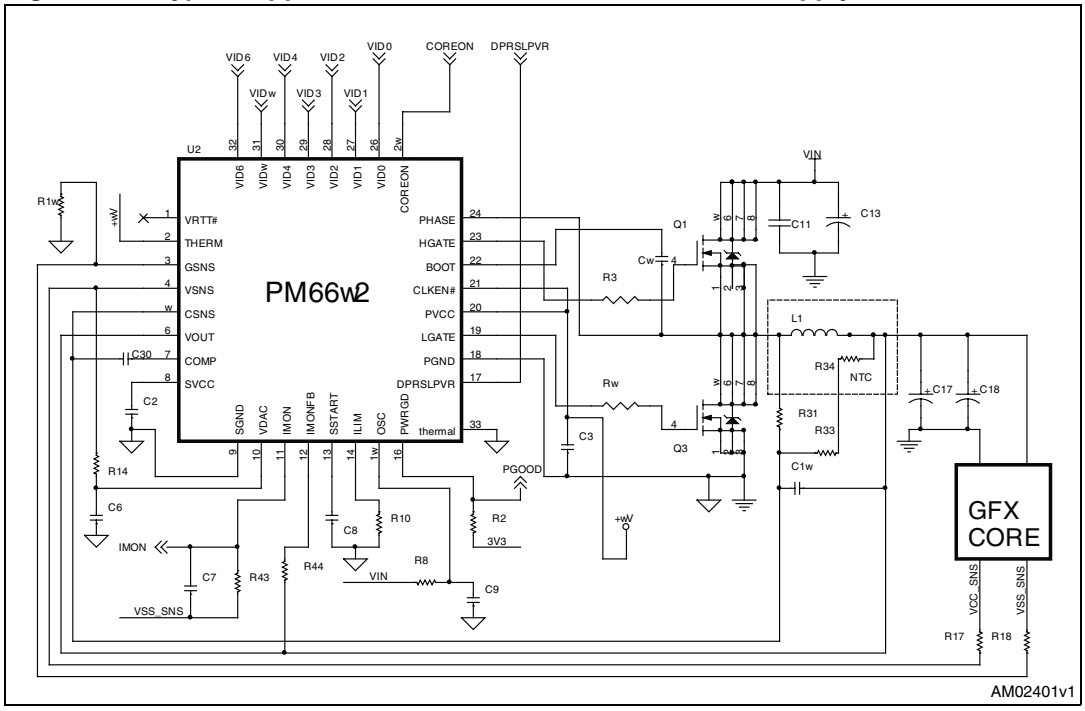


Figure 2. Typical application circuit - IMVP6.5 LV/ULV CPU supply

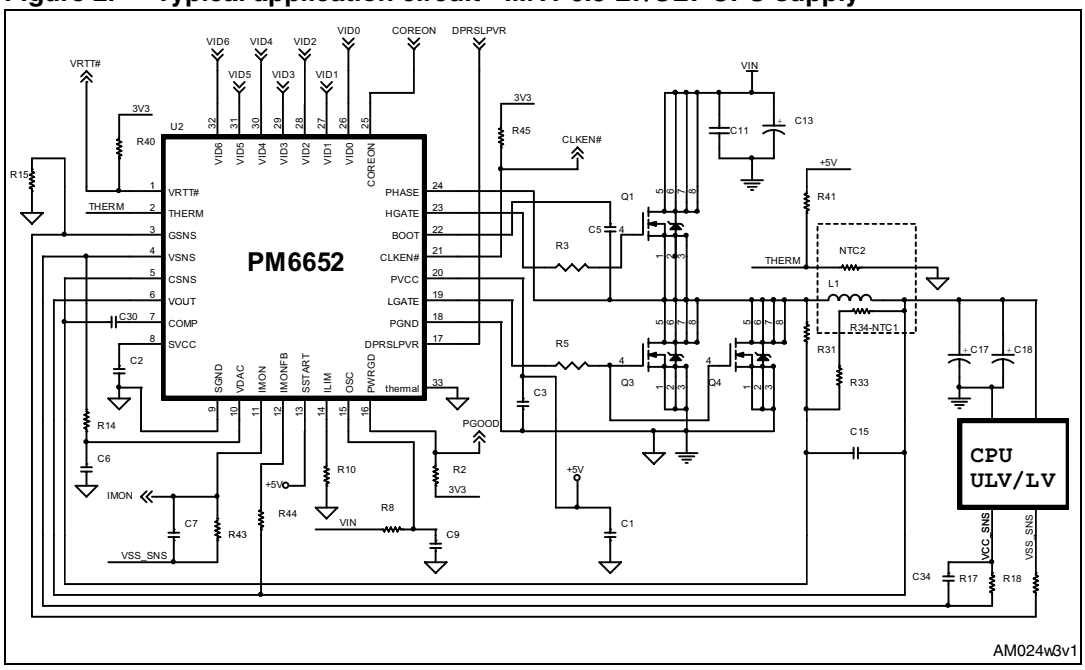
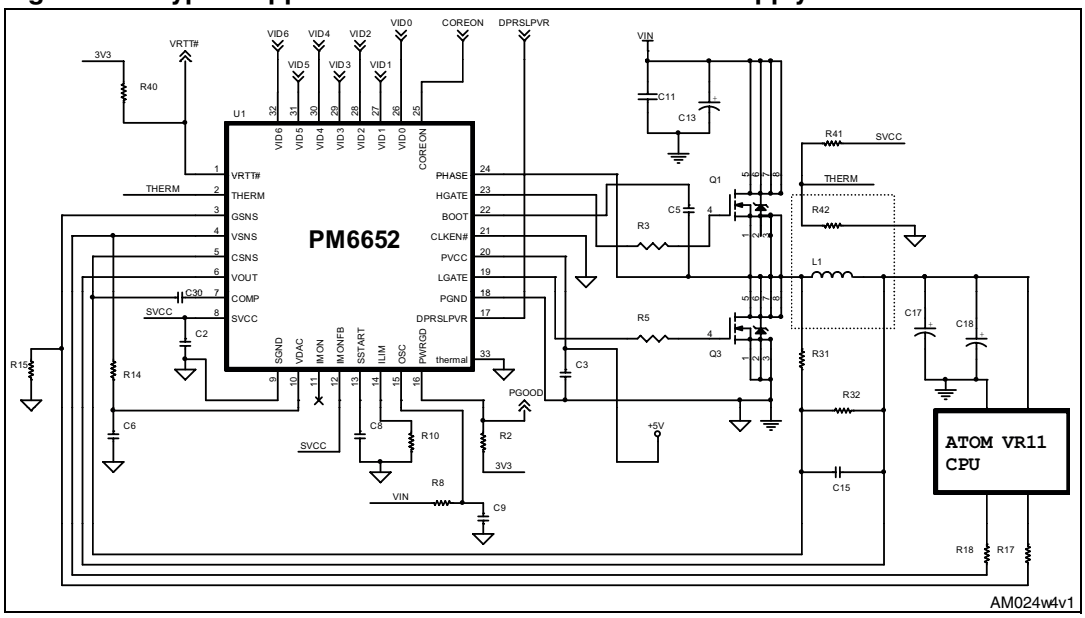


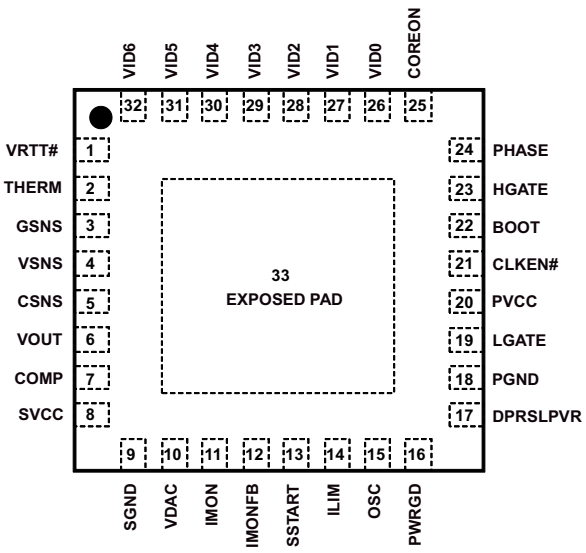
Figure 3. Typical application circuit – VR11 Atom CPU supply



2 Pin settings

2.1 Connections

Figure 4. PM6652 pinout (top view)



AM02402v1

2.2 Pin description

Figure 5. Pin functions

Pin n°	Name	Description
1	VRTT#	Thermal throttling indicator, open drain output.
2	THERM	Thermal throttling input. Connect to the central tap of NTC-based divider for MOS or inductor thermal monitoring.
3	GSNS	Output voltage ground remote sensing.
4	VSNS	Output voltage remote sensing.
5	CSNS	Current sensing input for droop function and IMON reporting. It represents the positive input of the differential current comparator. Connect to the inductor, for DCR sensing, or to a dedicated resistor for precision current sensing.
6	VOUT	Output voltage feedback. It also represents the negative input of the differential current comparator.
7	COMP	DC output voltage error compensation pin.
8	SVCC	+5 V analog and digital supply.
9	SGND	Analog and digital ground.

Figure 5. Pin functions (continued)

Pin n°	Name	Description
10	VDAC	Internal DAC reference output. Bypass to GND with a 10 nF capacitor.
11	IMON	Current monitor output. Bypass to remote ground through R-C network.
12	IMONFB	Current monitor gain setting pin. Connect to V_{OUT} through a resistor in the range 0.47 kΩ to 7 kΩ.
13	SSTART	Soft-start programming pin and mode of operation selection input.
14	ILIM	Current limit input. Connect ILIM to GND with a resistor to set the current limit threshold.
15	OSC	Frequency selection pin. Connect this pin to the input power supply rail through a resistor.
16	PWRGD	Power good signal (open drain output). High when VCC_GFX output voltage is within +200 mV/-300 mV of the programmed V_{DAC} value.
17	DPRSLPVR	Render suspend state enter and render suspend exit mode control input. Pulse-skipping or forced PWM working mode selection for IMVP6.5 CPU and VR11 mode.
18	PGND	Power ground.
19	LGATE	Low-side gate driver output.
20	PVCC	+5 V supply for internal driver supply.
21	CLKEN#	CLOCK ENABLE open drain output (active low) and mode of operation selection pin.
22	BOOT	Bootstrap capacitor connection. Input for the supply voltage of the high-side gate driver.
23	HGATE	High-side gate driver output.
24	PHASE	Switch node connection and return path for the high-side gate driver.
25	COREON	Switching regulator ON/OFF control input.
26	VID0	VIDs bits of the controller voltage programming DAC input. They allow programming of the no load output voltage, depending on the selected mode of operation. VID0 is the LSB and VID6 the MSB. Connect VIDx to a voltage <0.33 V to program a ‘0’; connect VIDx to a voltage >0.77 V to program a ‘1’.
27	VID1	
28	VID2	
29	VID3	
30	VID4	
31	VID5	
32	VID6	
33	EP	Exposed pad. Connect to SGND.

3 Electrical data

3.1 Maximum rating [a]

Table 2. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{PVCC}	PVCC to PGND		-0.3 to 6	V
V_{SVCC}	SVCC to SGND		-0.3 to 6	V
	SGND to PGND		-0.3 to 0.3	V
V_{BOOT}	BOOT to PHASE		-0.3 to 6	V
V_{HGATE}	HGATE to PHASE		-0.3 to V_{BOOT} +0.3	V
V_{PHASE}	PHASE to PGND		-0.3 to 37	V
V_{LGATE}	LGATE to PGND		-0.3 to V_{PVCC} +0.3	V
	VRTT#, THERM, GSNS, VSNS, CSNS, VOUT, COMP, VDAC, IMON, IMONFB, ILIM, OSC, PWRGD, DPRSLPVR, SSTART, CLKEN#, COREON, VIDx, to SGND		-0.3 to V_{SVCC} +0.3	V
	Maximum withstanding voltage range test condition: CDF-AEC-Q100-002- “human body model” acceptance criteria: “Normal Performance”	All the pins	±1250	V

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance between junction and ambient	35	°C/W
T_J	Junction operating temperature range	-40 to 125	°C
T_A	Operating ambient temperature range	-40 to 85	
T_{STG}	Storage temperature range	-50 to 150	

a. Free air operating conditions unless otherwise specified. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{IN}	Input voltage range	4.5	-	36	V
V_{PVCC}	PVCC voltage range	4.5	-	5.5	V

4 Electrical characteristics

T_J = 25 °C, V_{IN} = +12 V, PVCC = +5 V if not otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
Supply section							
$I_{SVCC,QUIESCENT}$	IC supply current	COREON=5 V, DPRSLPVR=5 V, FB forced above the regulation point				850	µA
$I_{SVCC,SHDN}$	Operating current in shutdown	COREON=SGND, T_A=25 °C				1	µA
V_{SVCC} UVLO	SVCC undervoltage lockout upper threshold	Rising edge, controller disabled below this level			4.3	4.5	V
	SVCC undervoltage lockout lower threshold	Falling edge, controller enabled above this level		3.8	3.9		
	UVLO hysteresis				400		mV
On-time							
T_{on}	On-time duration	V_{CORE}=1.5 V	OSC=250 mV	820	920	1020	ns
			OSC=500 mV	410	470	530	
			OSC=1 V	210	248	280	
Off-time							
T_{OFFMIN}	Minimum off-time				250	400	ns
Integrator							
V_{COMP}	Overvoltage clamp	$V_{OVCLAMP}=V_{COMP}-V_{CSNS}$			80		mV
	Undervoltage clamp	$V_{UVCLAMP}=V_{COMP}-V_{CSNS}$			-140		mV
	Integrator offset			-2.5		2.5	mV
Voltages and DAC							
V_{DAC}	Internal DAC reference voltage accuracy	DAC codes from 0.8125 V to 1.5000 V		-0.7%		0.7%	mV
		DAC codes from 0.3000 V to 0.8000 V		-10		10	
V_{DAC} slew-rate	V_{DAC} output voltage slew rate after VIDs variation.	GFX mode selected, and DPRSLPVR asserted, positive V_{DAC} dV/dt only, or VR11 mode selected.		10	12.5		mV/µs
		GFX mode selected, and DPRSLPVR de-assert, or CPU mode selected.		5	6.25		mV/µs
$I_{leakVCC\_GFXC}$	V_{CORE} voltage sense leakage current					1	µA
VBOOT	Boot-up voltage	CPU or VR11 mode selected			1.100		V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Current sensing						
I_{CSNS}	Input leakage current				1	µA
	Current limit comparator offset	$V_{OFFS}=V_{PGND}-V_{PHASE}$	-4		4	mV
I_{LIM}	ILIM bias current		4.5	5	5.5	µA
	Zero-crossing comparator offset		-3.5		3.5	mV
High-side and low-side gate drivers						
	HGATE driver ON-resistance	HGATE high state (pull-up)		2.0	3	Ω
		HGATE low state (pull-down)		1.6	2.7	Ω
	LGATE driver ON-resistance	LGATE high state (pull-up)		1	1.7	Ω
		LGATE low state (pull-down)		0.6	1	Ω
UVP/OVP protections, PWRGD and CLKEN# signals						
OVP_{FIXED}	Fixed overvoltage threshold			1.55		V
$OVP_{LATCHED}$	Overvoltage threshold	Referred to V_{DAC} value		200		mV
$UVP_{LATCHED}$	Undervoltage threshold	Referred to V_{DAC} value		-300		mV
PWRGD	Upper threshold	Referred to V_{DAC} value		200		mV
	Lower threshold			-300		
I_{PWRGD}	PWRGD leakage current	PWRGD forced to 3.3 V			1	µA
V_{PWRGD}	Output low voltage	Isink=4 mA		250	350	mV
CLKEN#	Output low voltage	Isink=4 mA		250	350	mV
	CLKEN# leakage current	CLKEN# forced to 3.3 V; SSTART=5 V			1	µA
Current monitor section						
IMON	Current monitor output	$V_{CSNS} - V_{OUT}$ = 60 mV; RIMONFB=1.8 kΩ; R_{IMON}=10 kΩ	970	1000	1030	mV
		$V_{CSNS} - V_{OUT}$ = 30 mV; RIMONFB=1.8 kΩ; R_{IMON}=10 kΩ	474	500	526	
		$V_{CSNS} - V_{OUT}$ = 15 mV; RIMONFB=1.8 kΩ; R_{IMON}=10 kΩ	226	250	274	
	Current monitor clamp, referred to GSNS	8 kΩ<R_{IMON}<16 kΩ; GSNS-AGND<20 mV			1.15	V
	Current monitor input offset	I_{IMON} = 0 µA	0		1.0	mV

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Soft-start section						
	Default soft-start slew rate	SSTART pin connected to AVCC	5	6.25		mV/µs
Soft-end section						
	VCC_GFX discharge resistance			7		Ω
Thermal throttling management						
THERM	Thermal detection trip threshold	Measured with respect to SGND		1.0		V
	Threshold hysteresis			200		mV
VRTT#	Output ON-resistance	THERM tied to SGND		7		Ω
$I_{VRTT\#}$	VRTT# leakage current	VRTT# forced to 3.3 V; THERM=5 V			1	µA
Power management						
COREON	SW regulator enable turn-on level		0.800			V
	SW regulator enable turn-off level				0.346	
$V_{DPRSLPVR}$	Render suspend pin thresholds	Render suspend (low)			0.346	V
		Render performance (high)	0.731			
VID_{IH}	VID high threshold		0.731			V
VID_{IL}	VID low threshold				0.346	V
I_{VID}	VID pull-up current				1	µA
Thermal shutdown						
T_{SHDN}	Shutdown temperature (1)			150		°C

1. Guaranteed by design. Not production tested.

5 Voltage identification (VID)

Table 6. VID for INTEL MVP 6.5 GFX core and CPU operation mode

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE
0	0	0	0	0	0	0	1.5000	1	0	0	0	0	0	0	0.7000
0	0	0	0	0	0	1	1.4875	1	0	0	0	0	0	1	0.6875
0	0	0	0	0	1	0	1.4750	1	0	0	0	0	1	0	0.6750
0	0	0	0	0	1	1	1.4625	1	0	0	0	0	1	1	0.6625
0	0	0	0	1	0	0	1.4500	1	0	0	0	1	0	0	0.6500
0	0	0	0	1	0	1	1.4375	1	0	0	0	1	0	1	0.6375
0	0	0	0	1	1	0	1.4250	1	0	0	0	1	1	0	0.6250
0	0	0	0	1	1	1	1.4125	1	0	0	0	1	1	1	0.6125
0	0	0	1	0	0	0	1.4000	1	0	0	1	0	0	0	0.6000
0	0	0	1	0	0	1	1.3875	1	0	0	1	0	0	1	0.5875
0	0	0	1	0	1	0	1.3750	1	0	0	1	0	1	0	0.5750
0	0	0	1	0	1	1	1.3625	1	0	0	1	0	1	1	0.5625
0	0	0	1	1	0	0	1.3500	1	0	0	1	1	0	0	0.5500
0	0	0	1	1	0	1	1.3375	1	0	0	1	1	0	1	0.5375
0	0	0	1	1	1	0	1.3250	1	0	0	1	1	1	0	0.5250
0	0	0	1	1	1	1	1.3125	1	0	0	1	1	1	1	0.5125
0	0	1	0	0	0	0	1.3000	1	0	1	0	0	0	0	0.5000
0	0	1	0	0	0	1	1.2875	1	0	1	0	0	0	1	0.4875
0	0	1	0	0	1	0	1.2750	1	0	1	0	0	1	0	0.4750
0	0	1	0	0	1	1	1.2625	1	0	1	0	0	1	1	0.4625
0	0	1	0	1	0	0	1.2500	1	0	1	0	1	0	0	0.4500
0	0	1	0	1	0	1	1.2375	1	0	1	0	1	0	1	0.4375
0	0	1	0	1	1	0	1.2250	1	0	1	0	1	1	0	0.4250
0	0	1	0	1	1	1	1.2125	1	0	1	0	1	1	1	0.4125
0	0	1	1	0	0	0	1.2000	1	0	1	1	0	0	0	0.4000
0	0	1	1	0	0	1	1.1875	1	0	1	1	0	0	1	0.3875
0	0	1	1	0	1	0	1.1750	1	0	1	1	0	1	0	0.3750
0	0	1	1	0	1	1	1.1625	1	0	1	1	0	1	1	0.3625
0	0	1	1	1	0	0	1.1500	1	0	1	1	1	0	0	0.3500
0	0	1	1	1	0	1	1.1375	1	0	1	1	1	0	1	0.3375
0	0	1	1	1	1	0	1.1250	1	0	1	1	1	1	0	0.3250
0	0	1	1	1	1	1	1.1125	1	0	1	1	1	1	1	0.3125

Table 6. VID for INTEL MVP 6.5 GFX core and CPU operation mode (continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE
0	1	0	0	0	0	0	1.1000	1	1	0	0	0	0	0	0.3000
0	1	0	0	0	0	1	1.0875	1	1	0	0	0	0	1	0.2875
0	1	0	0	0	1	0	1.0750	1	1	0	0	0	1	0	0.2750
0	1	0	0	0	1	1	1.0625	1	1	0	0	0	1	1	0.2625
0	1	0	0	1	0	0	1.0500	1	1	0	0	1	0	0	0.2500
0	1	0	0	1	0	1	1.0375	1	1	0	0	1	0	1	0.2375
0	1	0	0	1	1	0	1.0250	1	1	0	0	1	1	0	0.2250
0	1	0	0	1	1	1	1.0125	1	1	0	0	1	1	1	0.2125
0	1	0	1	0	0	0	1.0000	1	1	0	1	0	0	0	0.2000
0	1	0	1	0	0	1	0.9875	1	1	0	1	0	0	1	0.1875
0	1	0	1	0	1	0	0.9750	1	1	0	1	0	1	0	0.1750
0	1	0	1	0	1	1	0.9625	1	1	0	1	0	1	1	0.1625
0	1	0	1	1	0	0	0.9500	1	1	0	1	1	0	0	0.1500
0	1	0	1	1	0	1	0.9375	1	1	0	1	1	0	1	0.1375
0	1	0	1	1	1	0	0.9250	1	1	0	1	1	1	0	0.1250
0	1	0	1	1	1	1	0.9125	1	1	0	1	1	1	1	0.1125
0	1	1	0	0	0	0	0.9000	1	1	1	0	0	0	0	0.1000
0	1	1	0	0	0	1	0.8875	1	1	1	0	0	0	1	0.0875
0	1	1	0	0	1	0	0.8750	1	1	1	0	0	1	0	0.0750
0	1	1	0	0	1	1	0.8625	1	1	1	0	0	1	1	0.0625
0	1	1	0	1	0	0	0.8500	1	1	1	0	1	0	0	0.0500
0	1	1	0	1	0	1	0.8375	1	1	1	0	1	0	1	0.0375
0	1	1	0	1	1	0	0.8250	1	1	1	0	1	1	0	0.0250
0	1	1	0	1	1	1	0.8125	1	1	1	0	1	1	1	0.0125
0	1	1	1	0	0	0	0.8000	1	1	1	1	0	0	0	0.0000
0	1	1	1	0	0	1	0.7875	1	1	1	1	0	0	1	0.0000
0	1	1	1	0	1	0	0.7750	1	1	1	1	0	1	0	0.0000
0	1	1	1	0	1	1	0.7625	1	1	1	1	0	1	1	0.0000
0	1	1	1	1	0	0	0.7500	1	1	1	1	1	0	0	0.0000
0	1	1	1	1	0	1	0.7375	1	1	1	1	1	0	1	0.0000
0	1	1	1	1	1	0	0.7250	1	1	1	1	1	1	0	0.0000
0	1	1	1	1	1	1	0.7125	1	1	1	1	1	1	1	OFF

Table 7. Voltage identification (VID) for INTEL VR11 operation mode

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE
0	0	0	0	0	0	0	1.5000	1	0	0	0	0	0	0	0.8125
0	0	0	0	0	0	1	1.5000	1	0	0	0	0	0	1	0.8000
0	0	0	0	0	1	0	1.5000	1	0	0	0	0	1	0	0.7875
0	0	0	0	0	1	1	1.5000	1	0	0	0	0	1	1	0.7750
0	0	0	0	1	0	0	1.5000	1	0	0	0	1	0	0	0.7625
0	0	0	0	1	0	1	1.5000	1	0	0	0	1	0	1	0.7500
0	0	0	0	1	1	0	1.5000	1	0	0	0	1	1	0	0.7375
0	0	0	0	1	1	1	1.5000	1	0	0	0	1	1	1	0.7250
0	0	0	1	0	0	0	1.5000	1	0	0	1	0	0	0	0.7125
0	0	0	1	0	0	1	1.5000	1	0	0	1	0	0	1	0.7000
0	0	0	1	0	1	0	1.4875	1	0	0	1	0	1	0	0.6875
0	0	0	1	0	1	1	1.4750	1	0	0	1	0	1	1	0.6750
0	0	0	1	1	0	0	1.4625	1	0	0	1	1	0	0	0.6625
0	0	0	1	1	0	1	1.4500	1	0	0	1	1	0	1	0.6500
0	0	0	1	1	1	0	1.4375	1	0	0	1	1	1	0	0.6375
0	0	0	1	1	1	1	1.4250	1	0	0	1	1	1	1	0.6250
0	0	1	0	0	0	0	1.4125	1	0	1	0	0	0	0	0.6125
0	0	1	0	0	0	1	1.4000	1	0	1	0	0	0	1	0.6000
0	0	1	0	0	1	0	1.3875	1	0	1	0	0	1	0	0.5875
0	0	1	0	0	1	1	1.3750	1	0	1	0	0	1	1	0.5750
0	0	1	0	1	0	0	1.3625	1	0	1	0	1	0	0	0.5625
0	0	1	0	1	0	1	1.3500	1	0	1	0	1	0	1	0.5500
0	0	1	0	1	1	0	1.3375	1	0	1	0	1	1	0	0.5375
0	0	1	0	1	1	1	1.3250	1	0	1	0	1	1	1	0.5250
0	0	1	1	0	0	0	1.3125	1	0	1	1	0	0	0	0.5125
0	0	1	1	0	0	1	1.3000	1	0	1	1	0	0	1	0.5000
0	0	1	1	0	1	0	1.2875	1	0	1	1	0	1	0	0.4875
0	0	1	1	0	1	1	1.2750	1	0	1	1	0	1	1	0.4750
0	0	1	1	1	0	0	1.2625	1	0	1	1	1	0	0	0.4625
0	0	1	1	1	0	1	1.2500	1	0	1	1	1	0	1	0.4500
0	0	1	1	1	1	0	1.2375	1	0	1	1	1	1	0	0.4375
0	0	1	1	1	1	1	1.2250	1	0	1	1	1	1	1	0.4250
0	1	0	0	0	0	0	1.2125	1	1	0	0	0	0	0	0.4125
0	1	0	0	0	0	1	1.2000	1	1	0	0	0	0	1	0.4000

Table 7. Voltage identification (VID) for INTEL VR11 operation mode (continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE
0	1	0	0	0	1	0	1.1875	1	1	0	0	0	1	0	0.3875
0	1	0	0	0	1	1	1.1750	1	1	0	0	0	1	1	0.3750
0	1	0	0	1	0	0	1.1625	1	1	0	0	1	0	0	0.3625
0	1	0	0	1	0	1	1.1500	1	1	0	0	1	0	1	0.3500
0	1	0	0	1	1	0	1.1375	1	1	0	0	1	1	0	0.3375
0	1	0	0	1	1	1	1.1250	1	1	0	0	1	1	1	0.3250
0	1	0	1	0	0	0	1.1125	1	1	0	1	0	0	0	0.3125
0	1	0	1	0	0	1	1.1000	1	1	0	1	0	0	1	0.3000
0	1	0	1	0	1	0	1.0875	1	1	0	1	0	1	0	0.2875
0	1	0	1	0	1	1	1.0750	1	1	0	1	0	1	1	0.2750
0	1	0	1	1	0	0	1.0625	1	1	0	1	1	0	0	0.2625
0	1	0	1	1	0	1	1.0500	1	1	0	1	1	0	1	0.2500
0	1	0	1	1	1	0	1.0375	1	1	0	1	1	1	0	0.2375
0	1	0	1	1	1	1	1.0250	1	1	0	1	1	1	1	0.2250
0	1	1	0	0	0	0	1.0125	1	1	1	0	0	0	0	0.2125
0	1	1	0	0	0	1	1.0000	1	1	1	0	0	0	1	0.2000
0	1	1	0	0	1	0	0.9875	1	1	1	0	0	1	0	0.1875
0	1	1	0	0	1	1	0.9750	1	1	1	0	0	1	1	0.1750
0	1	1	0	1	0	0	0.9625	1	1	1	0	1	0	0	0.1625
0	1	1	0	1	0	1	0.9500	1	1	1	0	1	0	1	0.1500
0	1	1	0	1	1	0	0.9375	1	1	1	0	1	1	0	0.1375
0	1	1	0	1	1	1	0.9250	1	1	1	0	1	1	1	0.1250
0	1	1	1	0	0	0	0.9125	1	1	1	1	0	0	0	0.1125
0	1	1	1	0	0	1	0.9000	1	1	1	1	0	0	1	0.1000
0	1	1	1	0	1	0	0.8875	1	1	1	1	0	1	0	0.0875
0	1	1	1	0	1	1	0.8750	1	1	1	1	0	1	1	0.0750
0	1	1	1	1	0	0	0.8625	1	1	1	1	1	0	0	0.0625
0	1	1	1	1	0	1	0.8500	1	1	1	1	1	0	1	0.0500
0	1	1	1	1	1	0	0.8375	1	1	1	1	1	1	0	0.0375
0	1	1	1	1	1	1	0.8250	1	1	1	1	1	1	1	OFF

6 Typical operating characteristics

Measurement setup: V_{IN} = 10 V, F_{SW} = 320 kHz, V_{CORE} = 1.2375 V, DPRSLPVR = 0 V if not otherwise specified.

Figure 6. V_{CORE} turn-on and PGOOD rising - no load

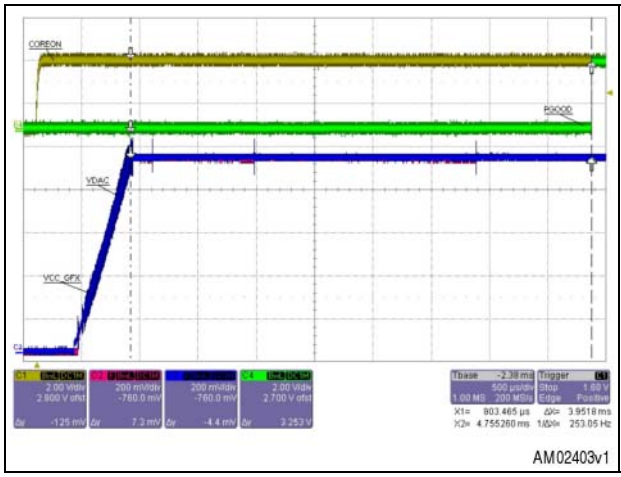


Figure 7. V_{CORE} turn-on - CPU IMVP6.5 mode

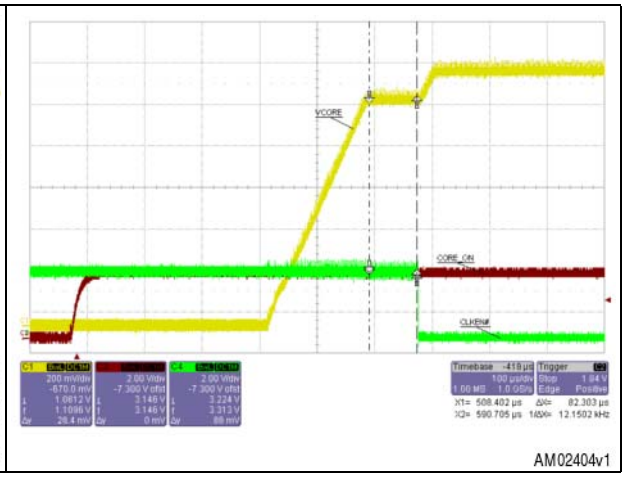


Figure 8. V_{CORE} working mode - DPRSLPVR asserted, no load

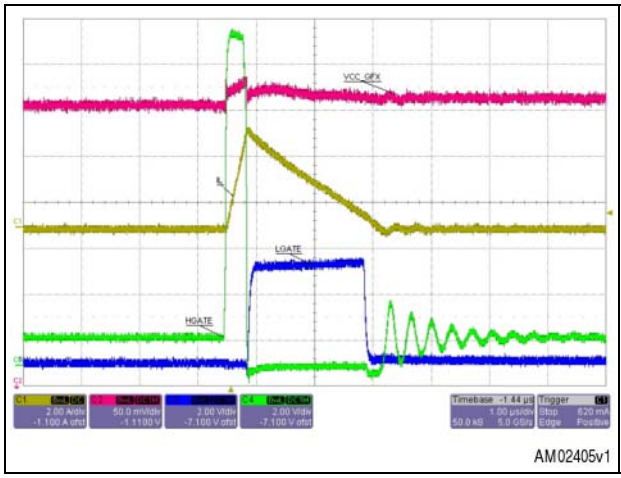


Figure 9. V_{CORE} working mode (0.9 V) - DPRSLPVR asserted, no load

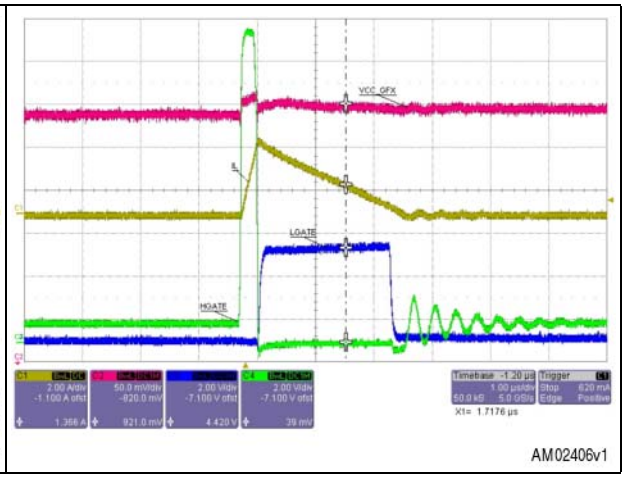


Figure 10. V_{CORE} working mode (0.4 V) - DPRSLPVR asserted, no load

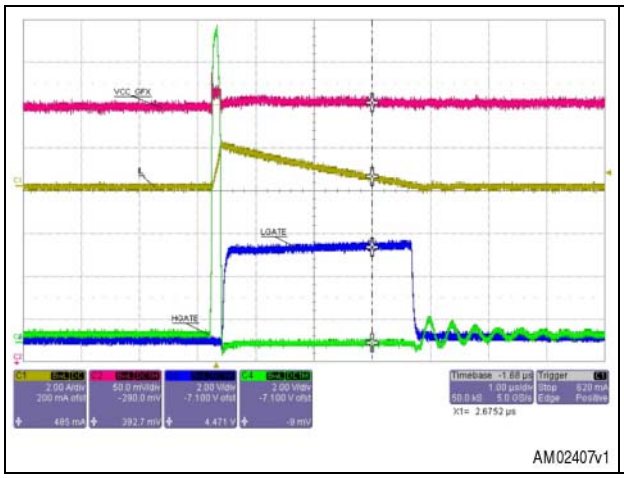


Figure 11. V_{CORE} working mode - DPRSLPVR not asserted, no load

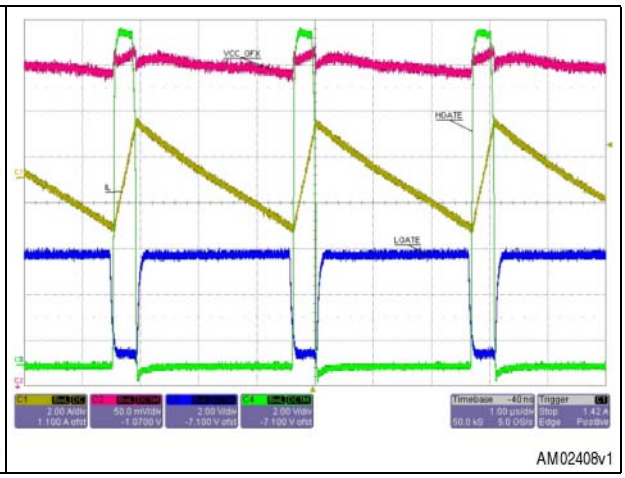


Figure 12. V_{CORE} working mode - DPRSLPVR not asserted, 10 A load

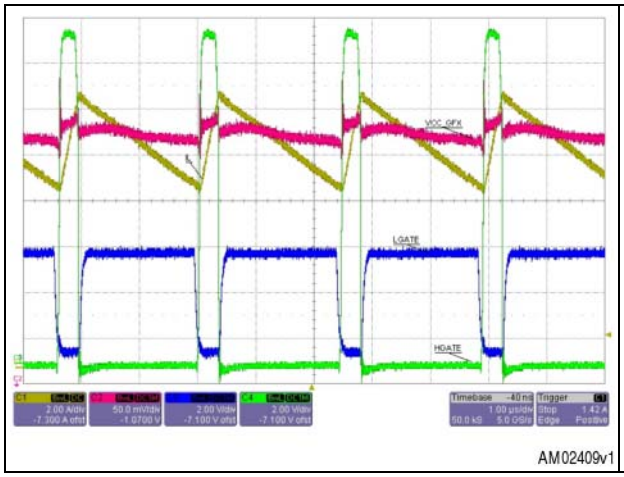


Figure 13. V_{CORE} working mode (0.9 V) - DPRSLPVR not asserted, no load

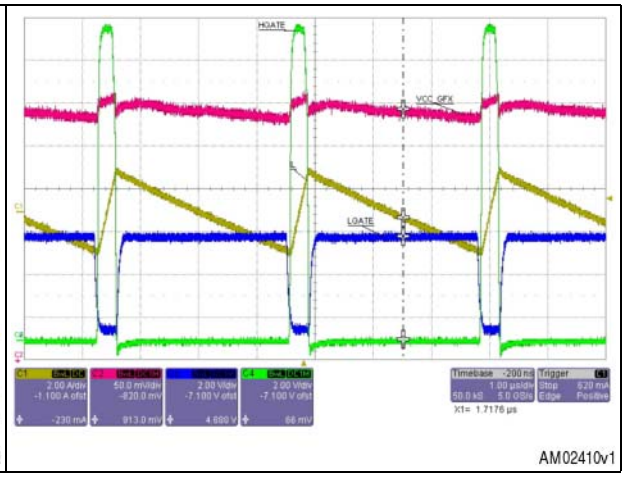


Figure 14. V_{CORE} working mode (0.4 V) - DPRSLPVR not asserted, no load

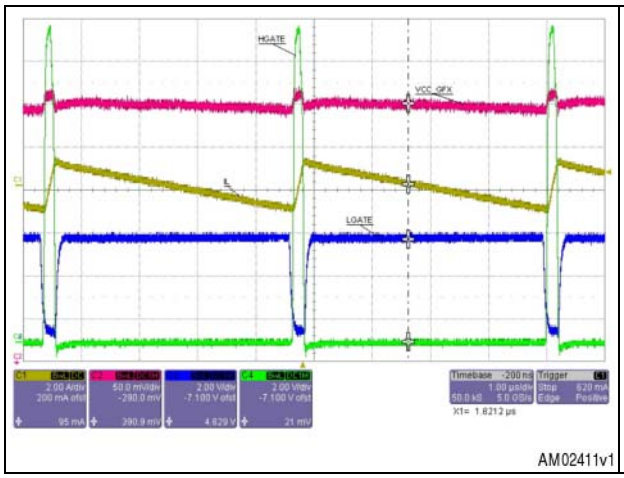


Figure 15. VID5 transition - entering and exiting suspend state (fast exit)

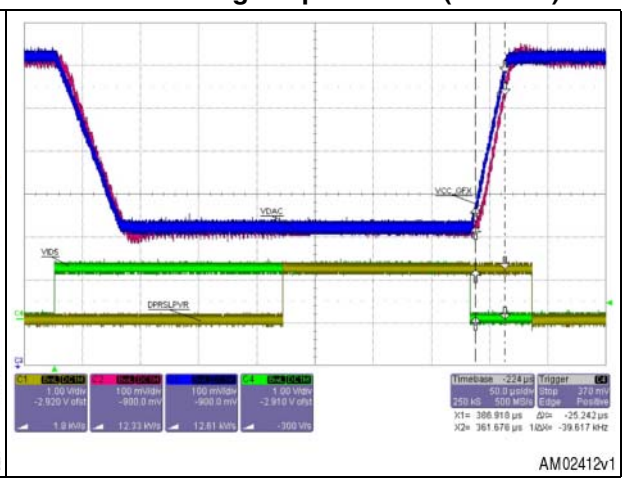


Figure 16. VID5 transition - entering and exiting suspend state (slow exit)

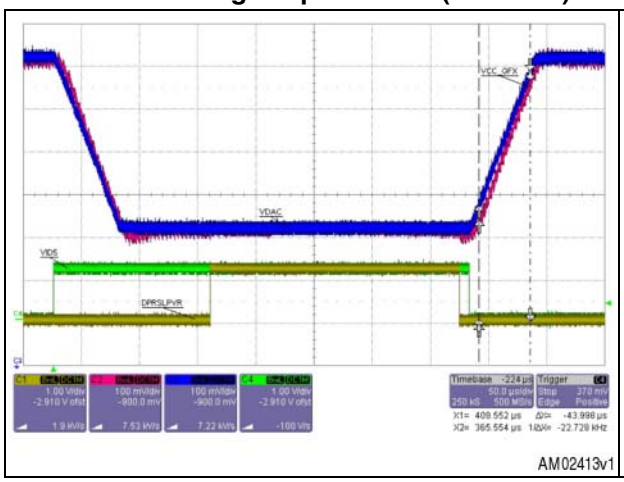


Figure 17. Droop function - 5 A to 15 A transient response

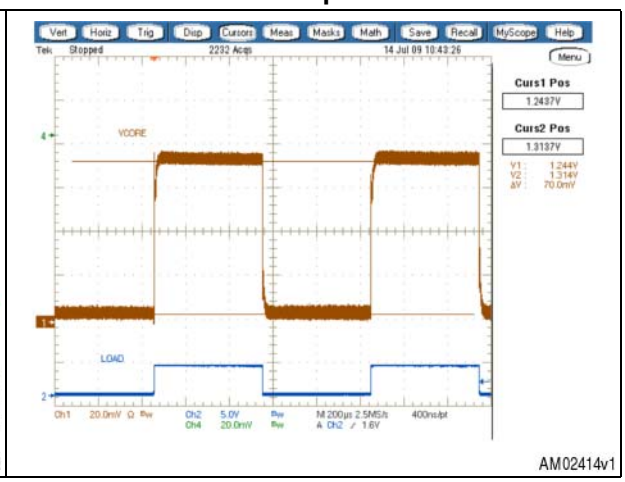


Figure 18. V_{CORE} VID step variation - VR11 mode

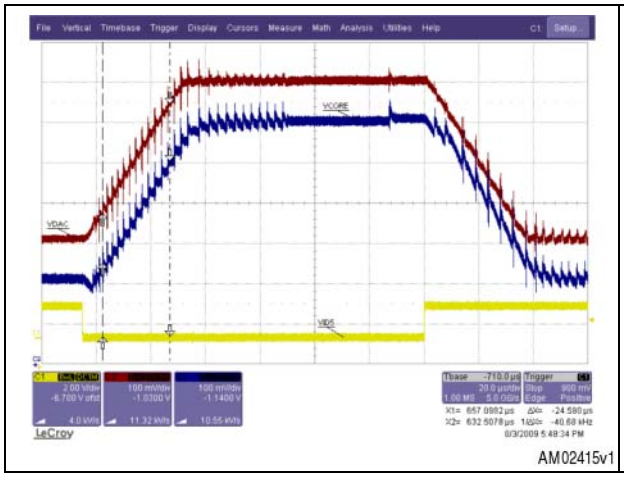


Figure 19. V_{CORE} soft-end - COREON pin de-assertion and PGOOD transition

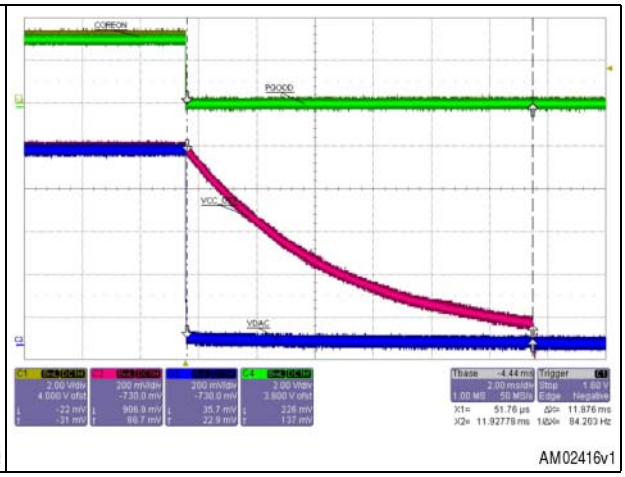


Figure 20. V_{CORE} overvoltage (+200 mV)

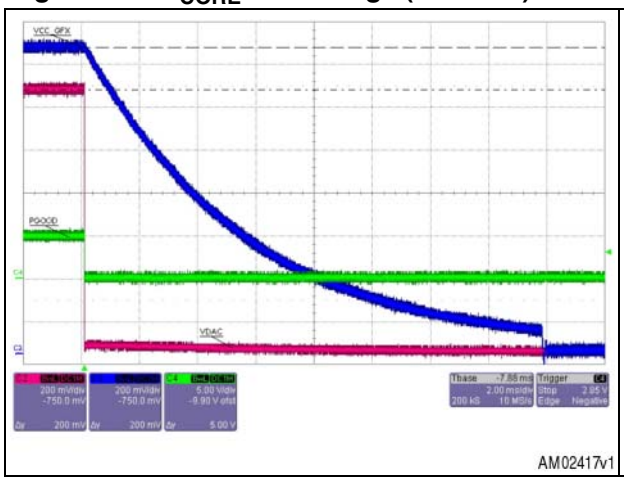


Figure 21. V_{CORE} undervoltage (-300 mV)

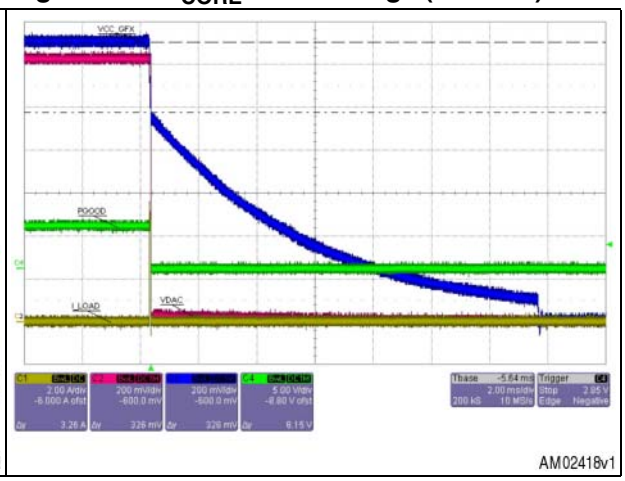


Figure 22. V_{CORE} efficiency (DPRSLPVR high and low)

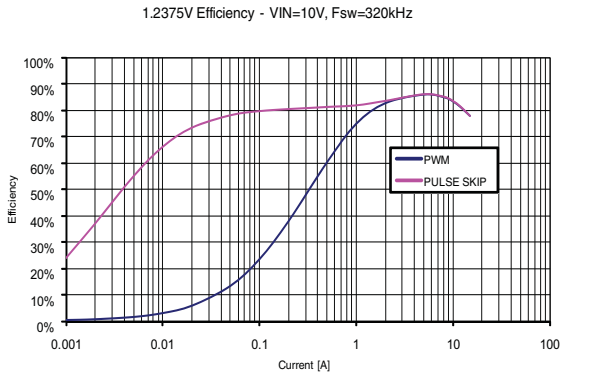
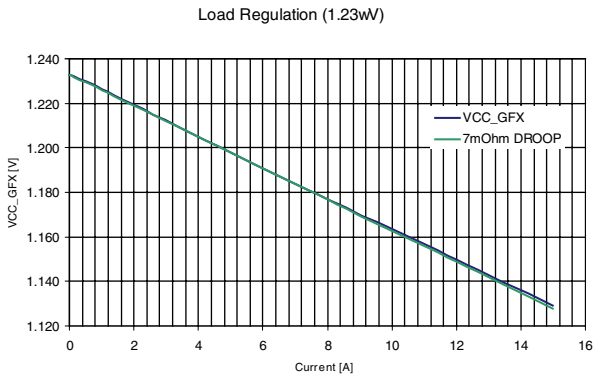
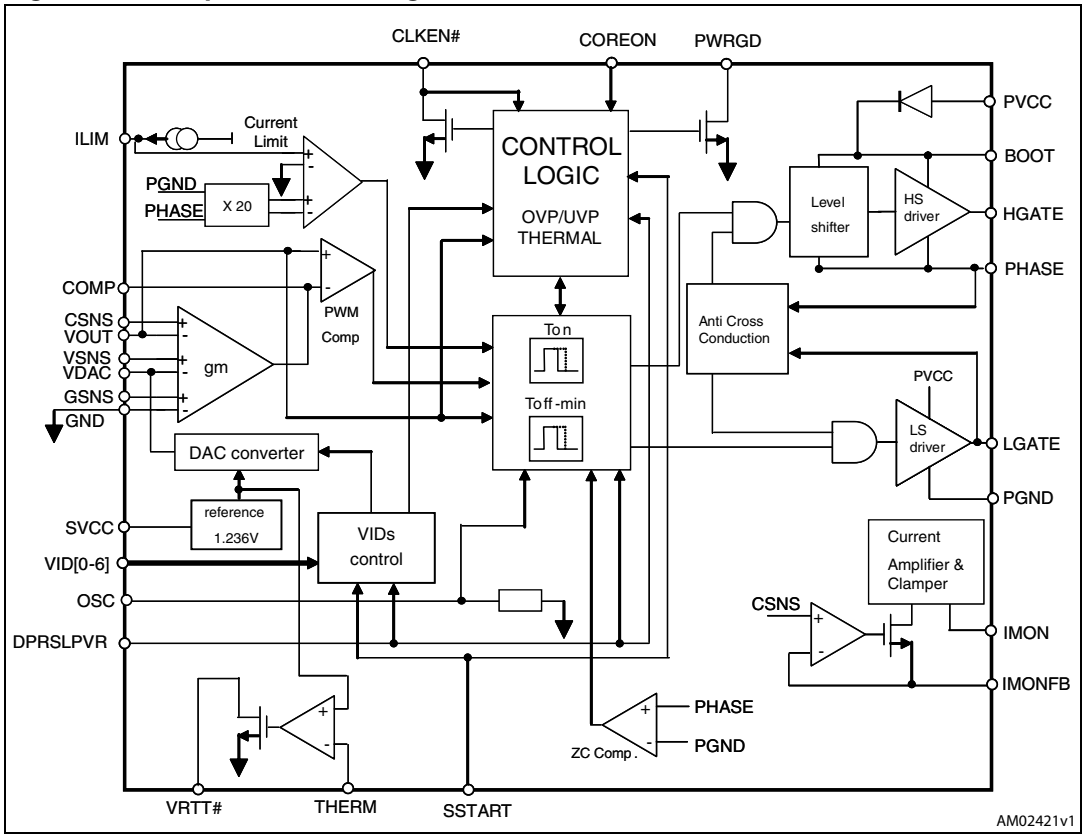


Figure 23. V_{CORE} load regulation - droop function



7 Block diagram

Figure 24. Simplified block diagram



8 Device description

The PM6652 is a single-phase, step-down controller which can be easily configured to regulate power to IMPV6.5 and VR11 devices, as listed below:

- The graphics (Render) core of the Intel® mobile Arrandale processor used on the Calpella platform
- The low voltage and ultra low voltage mobile CPU, used on the Calpella platform
- The VR11 compliant CPU, like Intel® ATOM 200/300 and Pineview-D CPU.

The supply mode and platform compliance are selected by acting on two multi-function pins (refer to *Section 8.2: Mode selection* for details), before the device turn-on.

The PM6652 is based on constant on-time control architecture. This type of control offers a very fast load transient response with a minimum external component count. A typical application circuit is shown in *Figure 1*. The controller includes a 7-bit digital-to-analog converter (DAC) that provides a reference voltage according to the VID pin settings (see *Table 6* and *Table 7*). The PM6652 also allows the adjusting of an active load line (or droop) control, proportional to the inductor DCR or dedicated precision resistor, according to IMVP6.5 specifications.

The switching frequency can be programmed in the range 200 kHz up to 600 kHz with an external resistor connected to the input voltage (see *Section 8.1: Constant on-time PWM control* for details).

In order to maximize the efficiency at very light load, a pulse-skipping control algorithm is performed. The PM6652 is also fully compliant with the fast and slow render suspend state exit mode, as required by IMVP 6.5 spec. for render core supply (see *Section 8.6: Voltage dynamic (VID) transitions* for details).

The device provides protection for overvoltage, undervoltage, overcurrent and overtemperature as well as power good (PWRGD), current monitor (IMON) and thermal throttling (VRTT#) signals for monitoring purposes. The clock enable output signal (CLKEN#), for appropriate platform power-up, is available in CPU supply mode only.

8.1 Constant on-time PWM control

The PM6652 controller uses a pseudo-fixed frequency, constant on-time (COT) controller as the core of the switching section. The COT controller uses a relatively simple algorithm, exploiting the ripple voltage due to inductor resistance DCR (or due to a sense resistor R_{SNS}) to trigger the fixed on-time one-shot generator.

Nearly constant switching frequency is achieved by the system loop in steady-state operating conditions, therefore avoiding the need for a clock generator. A slight switching frequency variation towards the load is the consequence of the switching regulator power losses, which implies the off-time duration decrease.

The on-time one-shot duration is directly proportional to the output voltage, sensed at the VOUT pin, and inversely proportional to the input voltage, sensed at the VOSC pin, as follows: