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PM6670S

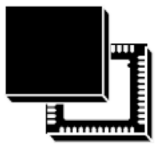
Complete DDR2/3 memory power supply controller

Features

- Switching section (VDDQ)
  - 4.5 V to 28 V input voltage range
  - 0.9 V, ±1 % voltage reference
  - 1.8 V (DDR2) or 1.5 V (DDR3) fixed output voltages
  - 0.9 V to 2.6 V adjustable output voltage
  - 1.237 V ±1 % reference voltage available
  - Very fast load transient response using constant on-time control loop
  - No R_{SENSE} current sensing using low side MOSFET's $R_{DS(ON)}$
  - Negative current limit
  - Latched OVP and UVP
  - Soft-start internally fixed at 3 ms
  - Selectable pulse skipping at light load
  - Selectable no-audible (33 kHz) pulse skip mode
  - Ceramic output capacitors supported
  - Output voltage ripple compensation
- VTT LDO and VTTREF
  - 2 Apk LDO with foldback for VTT
  - Remote VTT sensing
  - High-Z VTT output in S3
  - Ceramic output capacitors supported
  - ±15 mA low noise buffered reference

Applications

- DDR2/3 memory supply
- Notebook computers
- Handheld and PDAs
- CPU and chipset I/O supplies
- SSTL18, SSTL15 and HSTL bus termination



VFQFPN-24 4x4

Description

The device PM6670S is a complete DDR2/3 power supply regulator designed to meet JEDEC specifications.

It integrates a constant on-time (COT) buck controller, a 2 Apk sink/source low drop out regulator and a 15 mA low noise buffered reference.

The COT architecture assures fast transient response supporting both electrolytic and ceramic output capacitors. An embedded integrator control loop compensates the DC voltage error due to the output ripple.

The 2 Apk sink/source linear regulator provides the memory termination voltage with fast load transient response.

The device is fully compliant with system sleep states S3 and S4/S5, providing LDO output high impedance in suspend-to-RAM and tracking discharge of all outputs in suspend-to-disk.

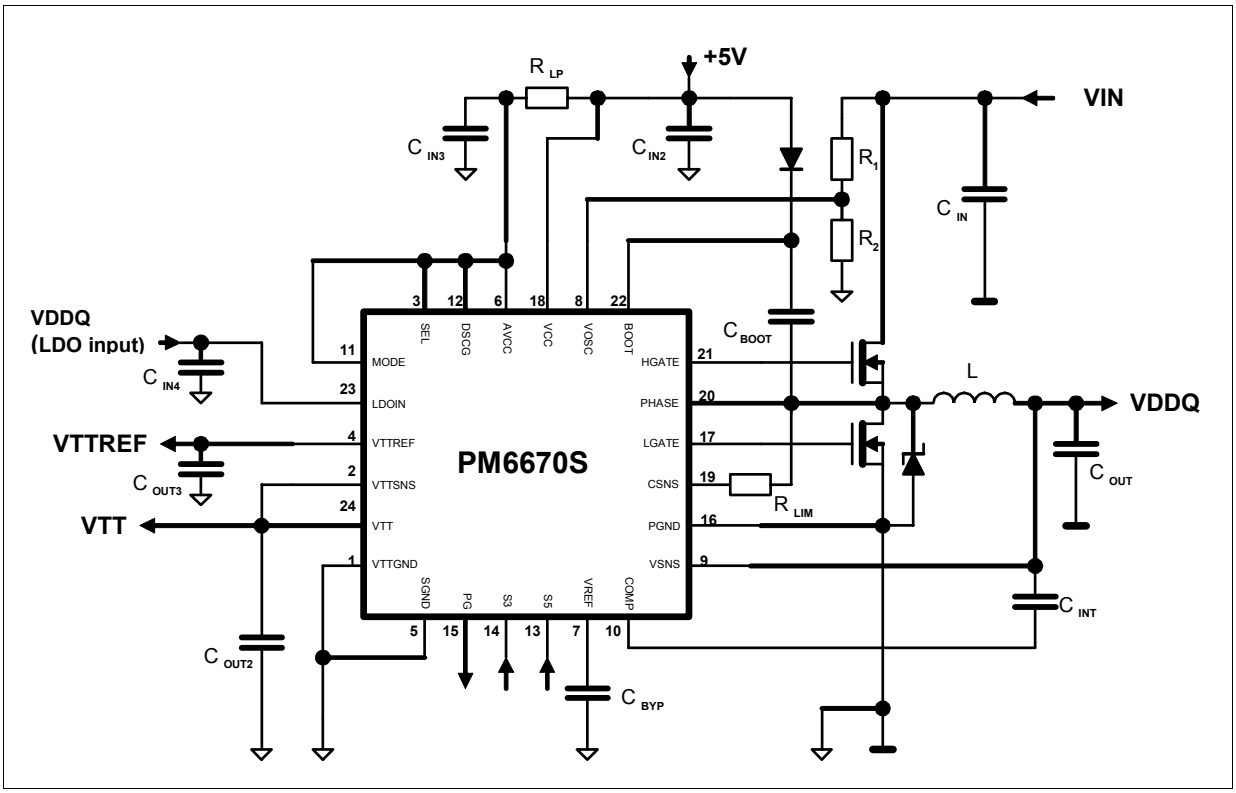
Table 1. Device summary

Order code	Package	Packaging
PM6670S	VFQFPN-24 4x4 (Exposed pad)	Tube
PM6670STR		Tape and reel

Contents

1 Typical application circuit

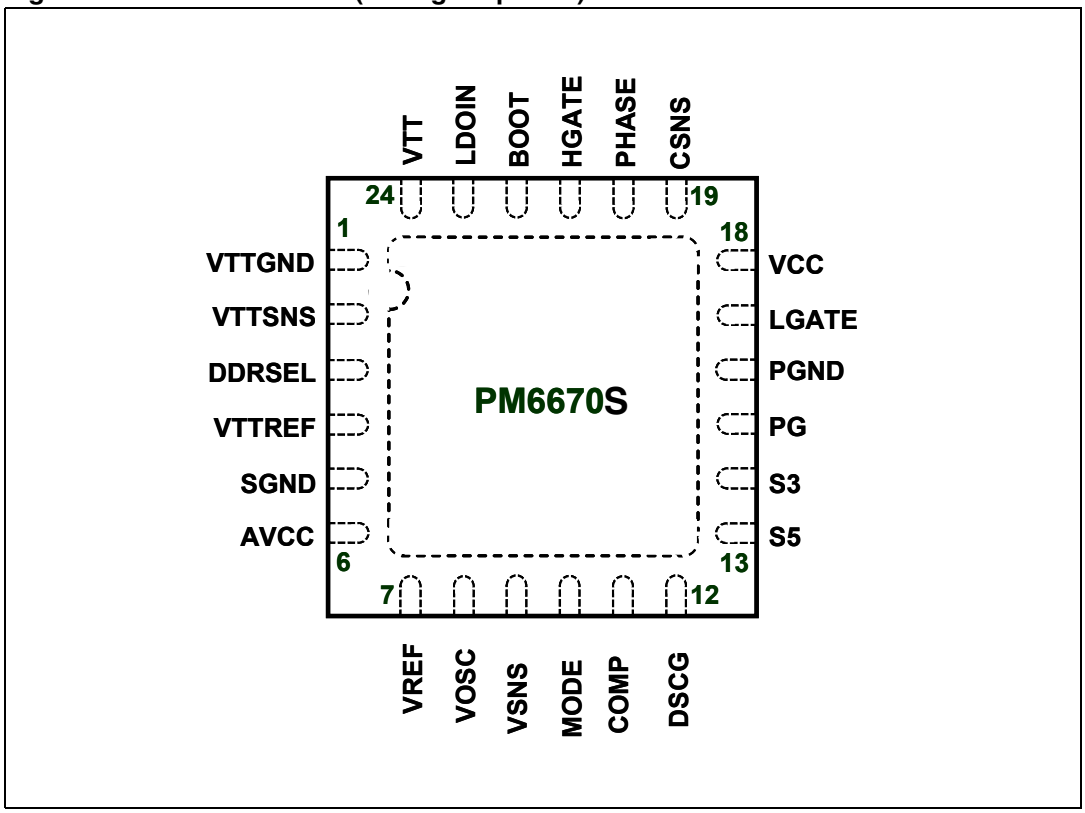
Figure 1. Application circuit



2 Pin settings

2.1 Connections

Figure 2. Pin connection (through top view)



2.2 Pin description

Table 2. Pin functions

N°	Pin	Function
1	VTTGND	LDO power ground. Connect to negative terminal of VTT output capacitor.
2	VTTSNS	LDO remote sensing. Connect as close as possible to the load via a low noise PCB trace.
3	DDRSEL	DDR voltage selector (if MODE is tied to VCC) or pulse-skip/no-audible pulse-skip selector in adjustable mode (MODE voltage lower than 3 V). See *Section 7.1.4: Mode-of-operation selection on page 30*.
4	VTTREF	Low noise buffered DDR reference voltage. A 22 nF (minimum) ceramic bypass capacitor is required in order to achieve stability.
5	SGND	Ground reference for analog circuitry, control logic and VTTREF buffer. Connect together with the thermal pad and VTTGND to a low impedance ground plane. See the *Application Note* for details.
6	AVCC	+5 V supply for internal logic. Connect to +5 V rail through a simple RC filtering network.
7	VREF	High accuracy output voltage reference (1.237 V) for multilevel pins setting. It can deliver up to 50 µA. Connect a 100 nF capacitor between VREF and SGND in order to enhance noise rejection.
8	VOSC	Frequency selection. Connect to the central tap of a resistor divider to set the desired switching frequency. The pin cannot be left floating. See *Section 7: Device description on page 20*
9	VSNS	VDDQ output remote sensing. Discharge path for VDDQ in Non-Tracking Discharge. Input for internal resistor divider that provides VDDQ/2 to VTTREF and VTT. Connect as close as possible to the load via a low noise PCB trace.
10	MODE	Mode of operation selector. If MODE pin voltage is higher than 4 V, the fixed output mode is selected. If MODE pin voltage is lower than 4 V, it is used as negative input of the error amplifier. See *Section 7.1.4: Mode-of-operation selection on page 30*.
11	COMP	DC voltage error compensation Input for the switching section. Refer *Section 7.1.4: Mode-of-operation selection on page 30*.
12	DSCG	Discharge mode selection. Refer to *Section 7.1.8: VDDQ output discharge on page 34* for tracking/non-tracking discharge or no-discharge options.
13	S5	Switching controller enable. Connect to S5 system status signal to meet S0-S5 power management states compliance. See *Section 7.3: S3 and S5 power management pins on page 38*, S5 pin can't be left floating.
14	S3	Linear regulator enable. Connect to S3 system status signal to meet S0-S5 power management states compliance. See *Section 7.3: S3 and S5 power management pins on page 38*, S3 pin can't be left floating.
15	PG	Power Good signal (open drain output). High when VDDQ output voltage is within ±10 % of nominal value.
16	PGND	Power ground for the switching section.
17	LGATE	Low-side gate driver output.

Table 2. Pin functions (continued)

N°	Pin	Function
18	VCC	+5 V low-side gate driver supply. Bypass with a 100 nF capacitor to PGND.
19	CSNS	Current sense input for the switching section. This pin must be connected through a resistor to the drain of the synchronous rectifier (R_{DSon} sensing) to set the current limit threshold.
20	PHASE	Switch node connection and return path for the high-side gate driver.
21	HGATE	High-side gate driver output
22	BOOT	Bootstrap capacitor connection. Positive supply input of the high-side gate driver.
23	LDOIN	Linear regulator input. Connect to VDDQ in normal configuration or to a lower supply to reduce the power dissipation. A 10 µF bypass ceramic capacitor is suggested for noise rejection enhancement. See *Section 7: Device description on page 20*
24	VTT	LDO linear regulator output. Bypass with a 20 µF (2x10 µF MLCC) filter capacitor.

3 Electrical data

3.1 Maximum rating

Table 3. Absolute maximum ratings (1)

Symbol	Parameter	Value	Unit
V_{AVCC}	AVCC to SGND	-0.3 to 6	V
V_{VCC}	VCC to SGND	-0.3 to 6	
	PGND, VTTGND to SGND	-0.3 to 0.3	
	HGATE and BOOT to PHASE	-0.3 to 6	
	HGATE and BOOT to PGND	-0.3 to 44	
V_{PHASE}	PHASE to SGND (2)	-0.3 to 38	
	LGATE to PGND	-0.3 to V_{CC} +0.3	
	CSNS, PG, S3, S5, DSCG, COMP, VSNS, VOSC, VREF, MODE, DDRSEL to GND	-0.3 to V_{AVCC} + 0.3	
	VTTREF, VREF, VTT, VTTSNS to SGND	-0.3 to V_{AVCC} + 0.3	
	LDOIN, VTT, VTTREF, LDOIN to VTTGND	-0.3 to V_{AVCC} + 0.3	
P_{TOT}	Power dissipation @T_A = 25 °C	2.3	W

1. Free air operating conditions unless otherwise specified. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. PHASE to SGND up to -2.5 V for t < 10 ns

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	42	°C/W
T_{STG}	Storage temperature range	- 50 to 150	°C
T_A	Operating ambient temperature range	- 40 to 85	°C
T_J	Junction operating temperature range	- 40 to 125	°C

3.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Values			Unit
		Min	Typ	Max	
V_{IN}	Input voltage range	4.5	-	28	V
V_{AVCC}	IC supply voltage	4.5	-	5.5	
V_{VCC}	IC supply voltage	4.5	-	5.5	

4 Electrical characteristics

T_A = 0 °C to 85 °C, VCC = AVCC = +5 V and LDOIN connected to VDDQ output if not otherwise specified [a]

Table 6. Electrical characteristics

Symbol	Parameter	Test condition		Values			Unit
				Min	Typ	Max	
Supply section							
I_{IN}	Operating current	S3, S5, MODE and DDRSEL connected to AVCC, no load on VTT and VTTREF outputs. VCC connected to AVCC			0.8	2	mA
I_{STR}	Operating current in STR	S5, MODE and DDRSEL connected to AVCC, S3 tied to SGND, no load on VTTREF. VCC connected to AVCC			0.6	1	
I_{SH}	Operating current in shutdown	S3 and S5 tied to SGND. Discharge mode active. VCC connected to AVCC			1	10	µA
UVLO	AVCC under voltage lockout upper threshold			4.1	4.25	4.4	V
	AVCC under voltage lockout lower threshold			3.85	4.0	4.1	
	UVLO hysteresis			70			mV
ON-time (SMPS)							
t_{ON}	On-time duration	MODE and DDRSEL high, V_{VSNS} = 2 V	VOSC = 300 mV	650	750	850	ns
			VOSC = 500 mV	390	450	510	
OFF-time (SMPS)							
t_{OFFMIN}	Minimum Off time				300	350	ns
Voltage reference							
	Voltage accuracy	4.5 V < V_{IN} < 25 V		1.224	1.237	1.249	V
	Load regulation	-50 µA< I_{VREF} < 50 µA		-4		4	mV
	Undervoltage lockout fault threshold				800		

a. $T_A = T_J$. All parameters at operating temperature extremes are guaranteed by design and statistical analysis (not production tested)

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
VDDQ output						
V_{VDDQ}	VDDQ output voltage, DDR3	MODE connected to AVCC, DDRSEL tied to SGND, No load		1.5		V
	VDDQ output voltage, DDR2	MODE and DDRSEL connected to AVCC, no load		1.8		
	Feedback accuracy		-1.5		1.5	%
Current limit and zero crossing comparator						
I_{CSNS}	CSNS input bias current		110	120	130	µA
	Comparator offset		-6		6	mV
	Positive current limit threshold	Rsense = 1 kΩ V_{PGND} - V_{CSNS}		120		mV
	Fixed negative current limit threshold			110		mV
$V_{ZC,OFFS}$	Zero crossing comparator offset		-11	-5	1	mV
High and low side gate drivers						
	HGATE driver on-resistance	HGATE high state (pull-up)		2.0	3	Ω
		HGATE low state (pull-down)		1.8	2.7	
	LGATE driver on-resistance	LGATE high state (pull-up)		1.4	2.1	
		LGATE low state (pull-down)		0.6	0.9	
UVP/OVP protections and PGOOD SIGNAL (SMPS only)						
OVP	Over voltage threshold		112	115	118	%
UVP	Under voltage threshold		67	70	73	
PGOOD	Power Good upper threshold		107	110	113	
	Power Good lower threshold		86	90	93	
$I_{PG,LEAK}$	PG leakage current	PG forced to 5 V			1	µA
$V_{PG,LOW}$	PG low-level voltage	$I_{PG,SINK}$ = 4 mA		150	250	mV
Soft start section (SMPS)						
	Soft-start ramp time (4 steps current limit)		1.5	3	4	ms
	Soft-start current limit step			30		µA

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
Soft end section						
	VDDQ discharge resistance in non-tracking discharge mode		15	25	35	Ω
	VTT discharge resistance in non-tracking discharge mode		15	25	35	
	VTTREF discharge resistance in non-tracking discharge mode		1	1.5	2	kΩ
	VDDQ output threshold synchronous for final tracking to non-tracking discharge transition		0.2	0.4	0.6	V
V_{TT} LDO section						
$I_{LDOIN,ON}$	LDO input bias current in full-on state	S3 = S5 = +5 V, No load on VTT		1	10	µA
$I_{LDOIN, STR}$	LDO input bias current in suspend-to-RAM state	S3 = 0 V, S5 = +5 V, No Load on VTT			10	
$I_{LDOIN, STD}$	LDO input bias current in suspend-to-disk state	S3 = S5 = 0 V, No Load on VTT			1	
$I_{VTTSNS, BIAS}$	VTTSNS bias current	S3 = +5 V, S5 = +5 V, $V_{VTTSNS} = V_{VSNS}/2$			1	
$I_{VTTSNS, LEAK}$	VTTSNS leakage current	S3 = 0 V, S5 = +5 V, $V_{VTTSNS} = V_{VSNS}/2$			1	
$I_{VTT,LEAK}$	VTT leakage current	S3 = 0 V, S5 = +5 V, $V_{VTT} = V_{VSNS}/2$	-10		10	
V_{VTT}	LDO linear regulator output voltage (DDR2)	S3 = S5= +5 V, I_{VTT} = 0 A, MODE = DDRSEL = +5 V		0.9		V
	LDO linear regulator output voltage (DDR3)	S3 = S5= +5 V, I_{VTT} = 0 A, MODE = +5 V, DDRSEL = 0 V		0.75		
	LDO output accuracy respect to VTTREF	S3 = S5 = MODE = + 5 V, -1 mA < I_{VTT} < 1 mA	-20		20	mV
		S3 = S5 = MODE = +5 V, -1 A < I_{VTT} < 1 A	-25		25	
		S3 = S5 = MODE = +5 V, -2 A < I_{VTT} < 2 A	-35		35	

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
$I_{VTT,CL}$	LDO source current limit	V_{VTT} < 1.10*(V_{VSNS} /2)	2	2.3	3	A
		V_{VTT} > 1.10*(V_{VSNS} /2)	1	1.15	1.4	
	LDO sink current limit	V_{VTT} > 0.90*(V_{VSNS} /2)	-3	-2.3	-2	
		V_{VTT} < 0.90*(V_{VSNS} /2)	-1.4	-1.15	-1	
VTTREF section						
V_{VTTREF}	VTTREF output voltage	I_{VTTREF} = 0 A, V_{VSNS} = 1.8 V		0.9		V
	VTTREF output voltage accuracy respect to VSNS/2	-15 mA < I_{VTTREF} < 15 mA, V_{VSNS} = 1.8 V	-2		2	%
I_{VTTREF}	VTTREF current limit	VTTREF= 0 or VSNS		±40		mA
Power management section						
S3,S5	Turn OFF level		0.4			V
	Turn ON level				1.6	
V_{MODE}	MODE pin high level threshold		V_{AVCC} -0.7			
	MODE pin low level threshold				V_{AVCC} - 1.3	
V_{DDRSEL}	DDRSEL pin high level threshold		V_{AVCC} -0.8			
	DDRSEL pin middle level window		1.0		V_{AVCC} - 1.5	
	DDRSEL pin low level threshold				0.5	
V_{DSCG}	DSCG pin high level threshold		V_{AVCC} -0.8			
	DSCG pin middle level window		1.0		2.0	
	DSCG pin low level threshold				0.5	
$I_{IN,LEAK}$	Logic inputs leakage current	S3, S5 = 5 V			10	µA
$I_{IN3,LEAK}$	Multilevel inputs leakage current	MODE, DDRSEL and DSCG = 5 V			10	
$I_{OSC,LEAK}$	VOSC input leakage current	VOSC = 500 mV			1	
Thermal shutdown						
T_{SHDN}	Shutdown temperature (1)			150		°C

1. Guaranteed by design. Not production tested.

5 Typical operating characteristics

Figure 3. Efficiency vs load - 1.5 V and 1.8 V, V_{IN} = 12 V

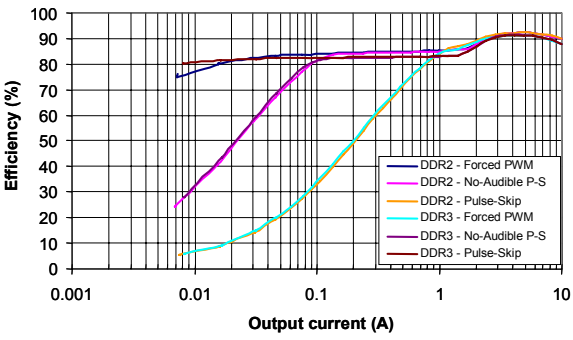


Figure 4. Switching frequency vs load - 1.8 V, V_{IN} = 12 V

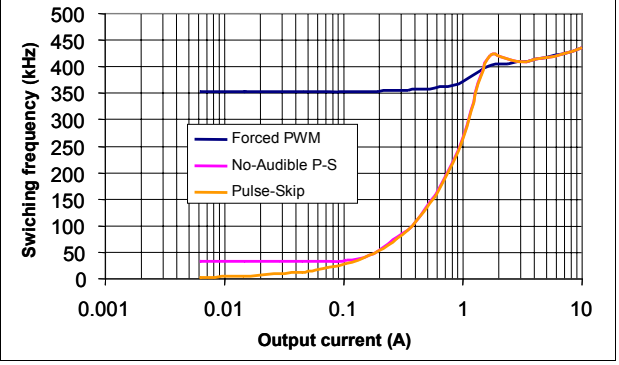


Figure 5. Switching frequency vs input voltage, 1.8 V

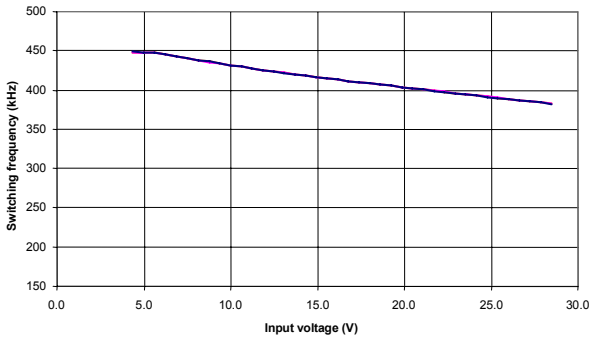


Figure 6. Switching frequency vs input voltage, 1.5 V

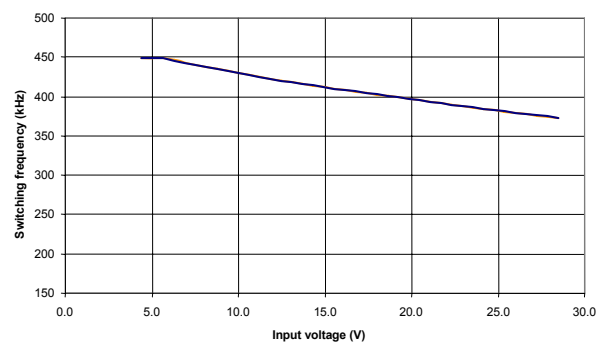


Figure 7. VDDQ line regulation, 1.8 V, 7 A

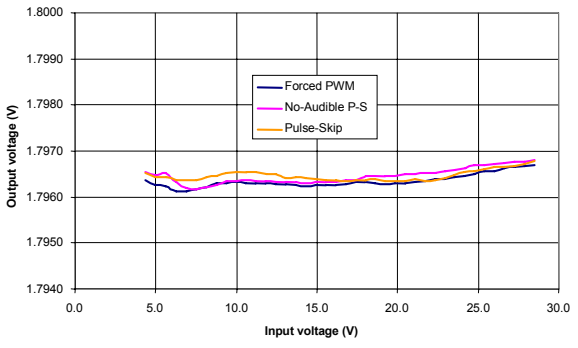


Figure 8. VDDQ line regulation, 1.5 V, 7 A

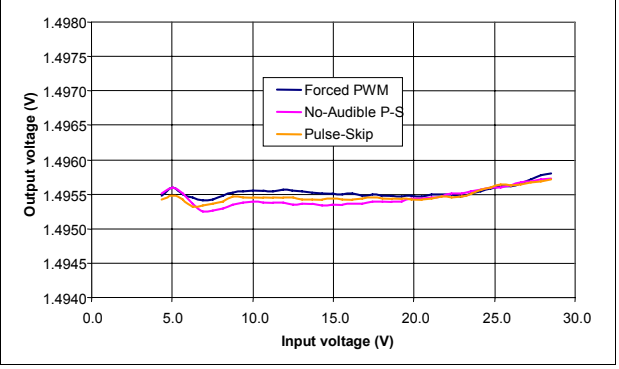


Figure 9. VDDQ load regulation, 1.8 V, V_{IN} = 12 V

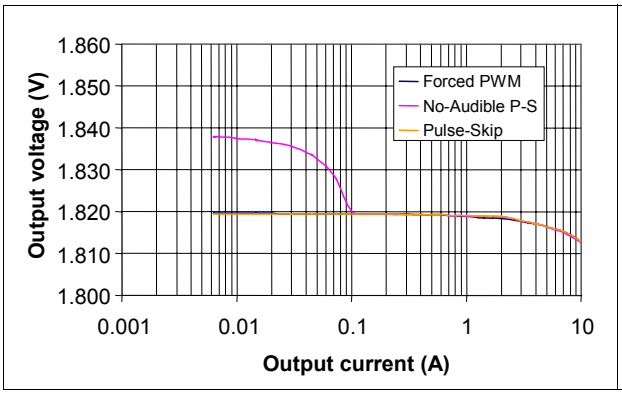


Figure 10. VDDQ load regulation, 1.5 V, V_{IN} = 12 V

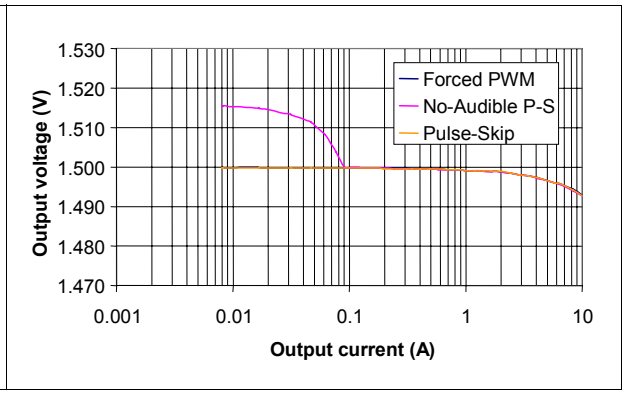


Figure 11. VTT load regulation, 0.9 V, LDOIN = 1.8 V

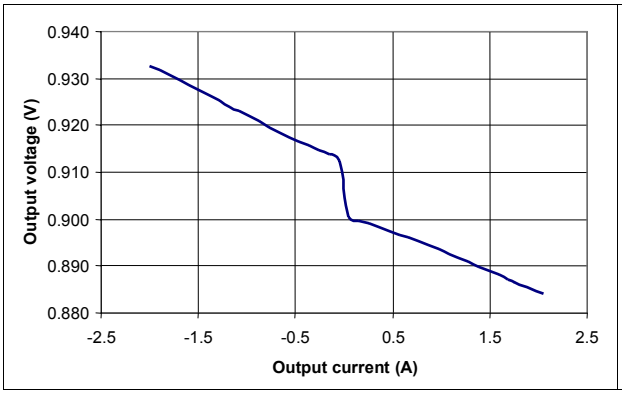


Figure 12. VTT load regulation, 0.75 V, LDOIN = 1.5 V

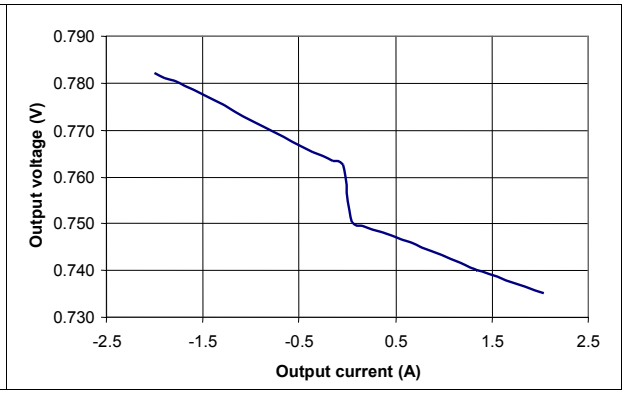


Figure 13. VTTREF load regulation, 0.9 V, VSNS = 1.8 V

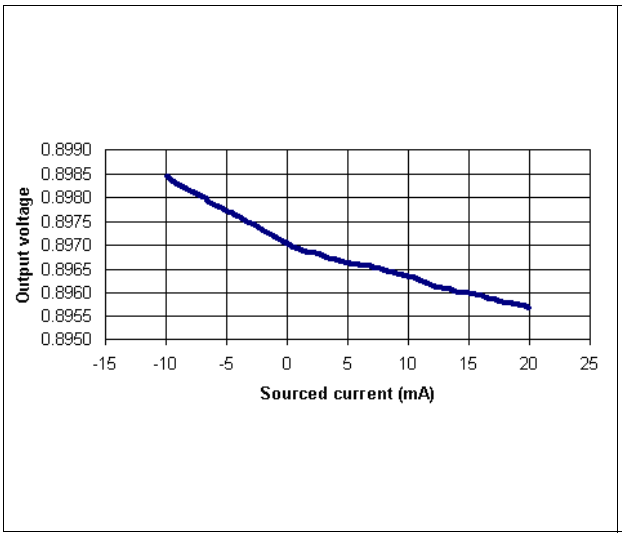


Figure 14. No-audible pulse-skip waveforms

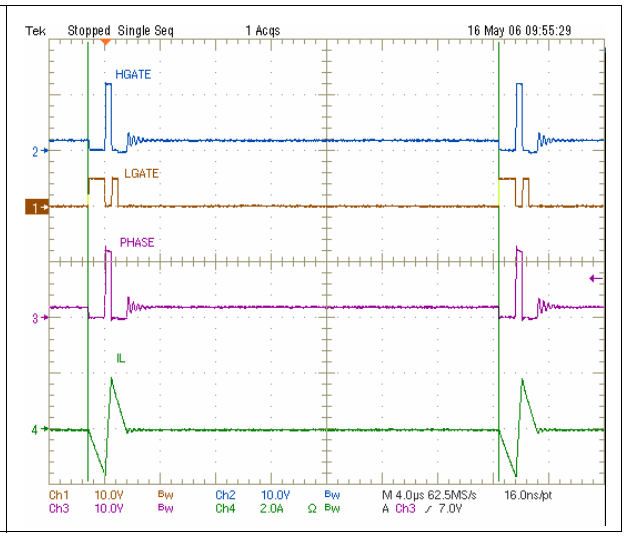


Figure 15. Power-up sequence - AVCC above UVLO

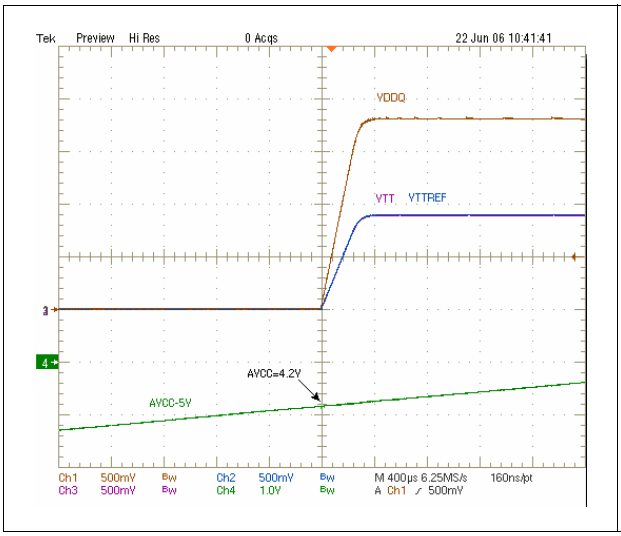


Figure 16. VDDQ soft-start, 1.8 V, heavy load

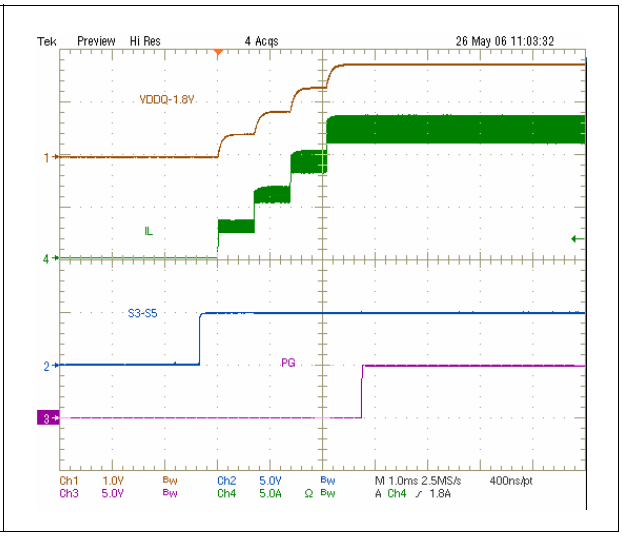


Figure 17. -1.8 A to 1.8 A VTT load transient, 0.9 V

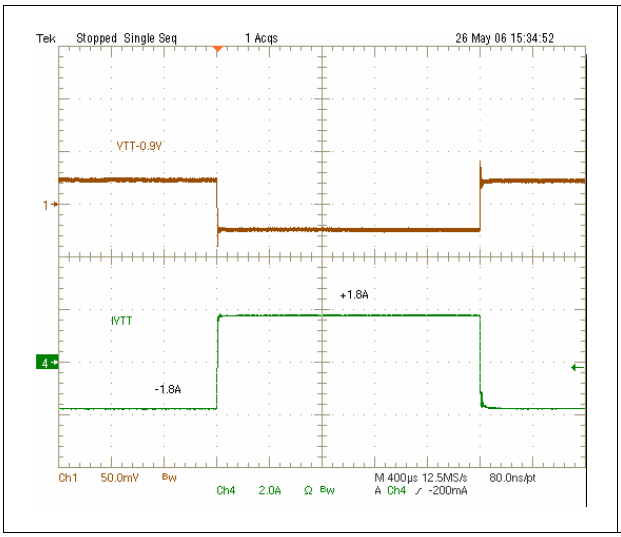


Figure 18. 0 mA to 9 mA VTTREF load transient, 0.9 V

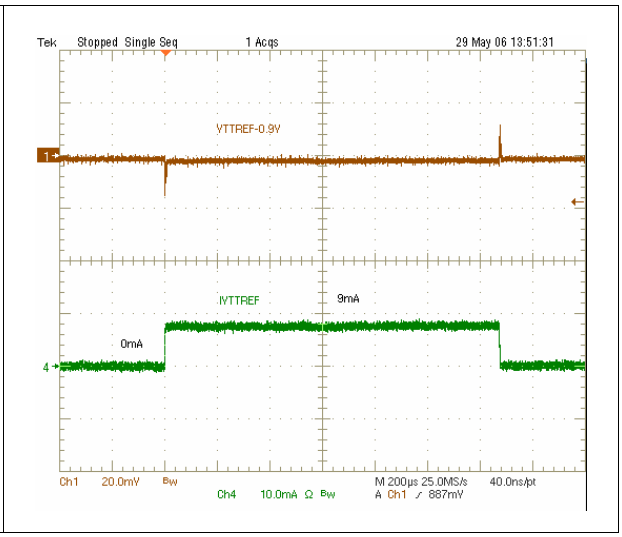


Figure 19. Non-tracking (soft) discharge

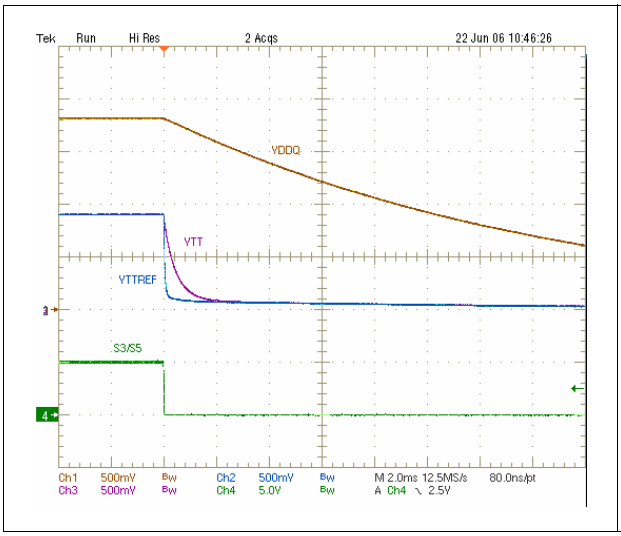


Figure 20. Tracking (fast) discharge, LDOIN = VDDQ

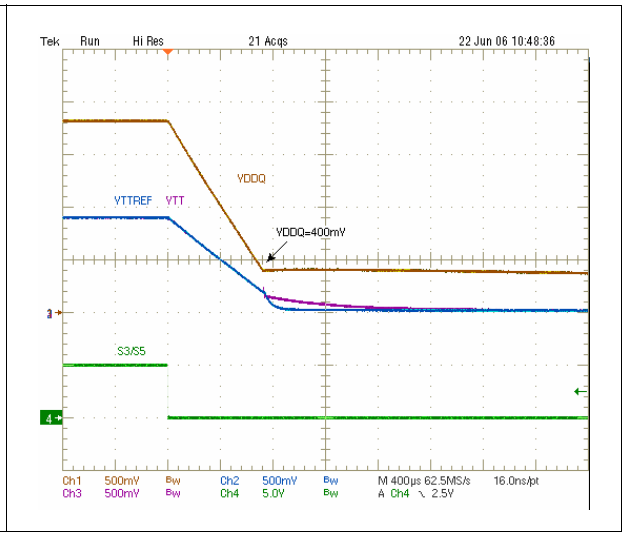


Figure 21. 0 A to 10 A VDDQ load transient, PWM

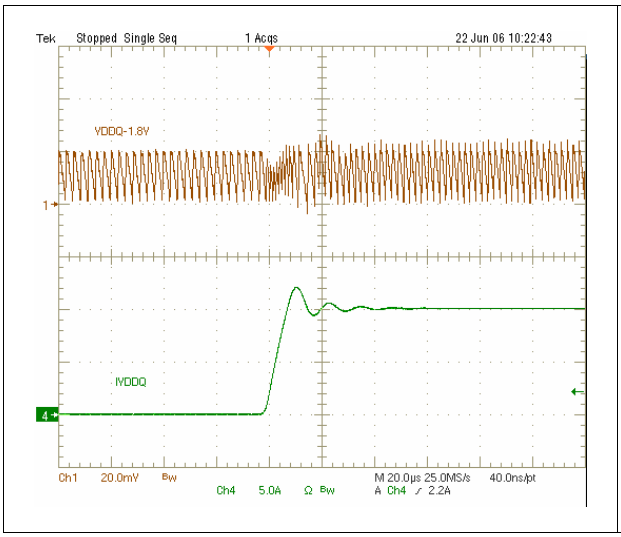


Figure 22. 10 A to 0 A VDDQ load transient, PWM

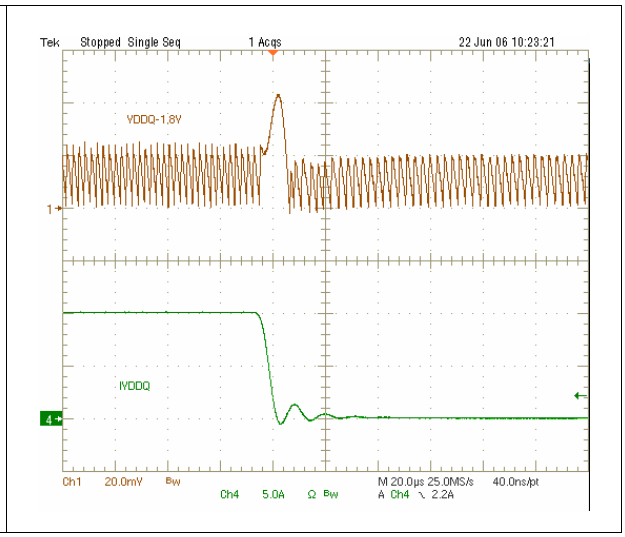


Figure 23. 0 A to 10 A VDDQ load transient, pulse-skip

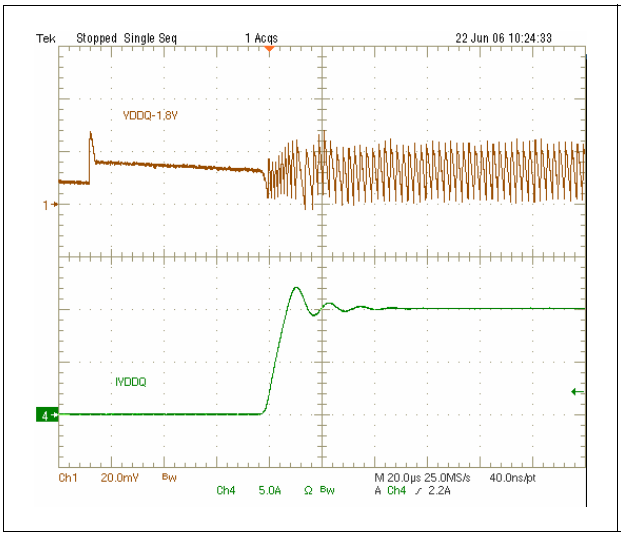


Figure 24. 10 A to 0 A VDDQ load transient, pulse-skip

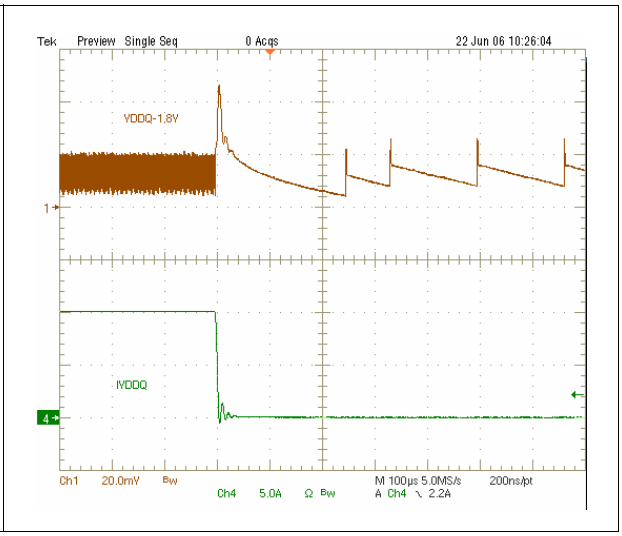


Figure 25. Over-voltage protection, VDDQ = 1.8 V

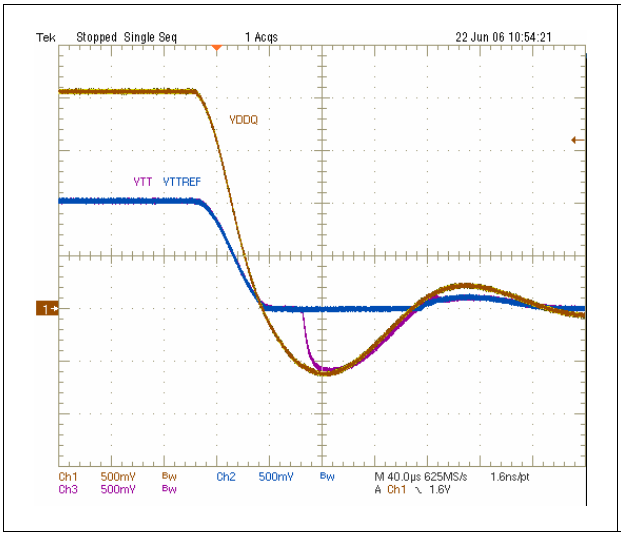
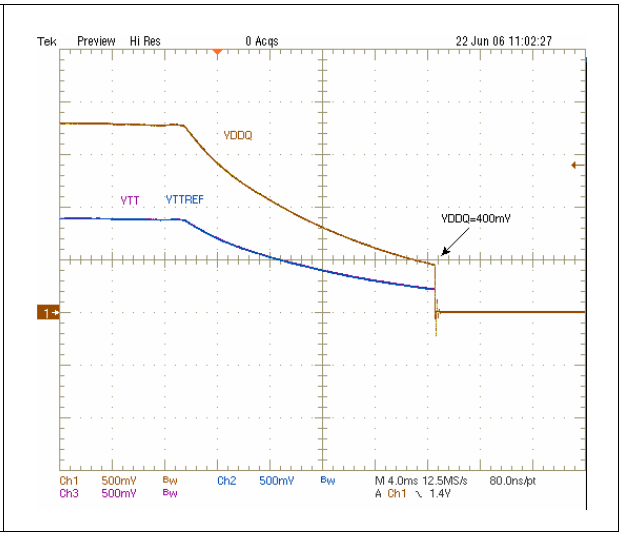


Figure 26. Under-voltage protection, VDDQ = 1.8 V



6 Block diagram

Figure 27. Functional and block diagram

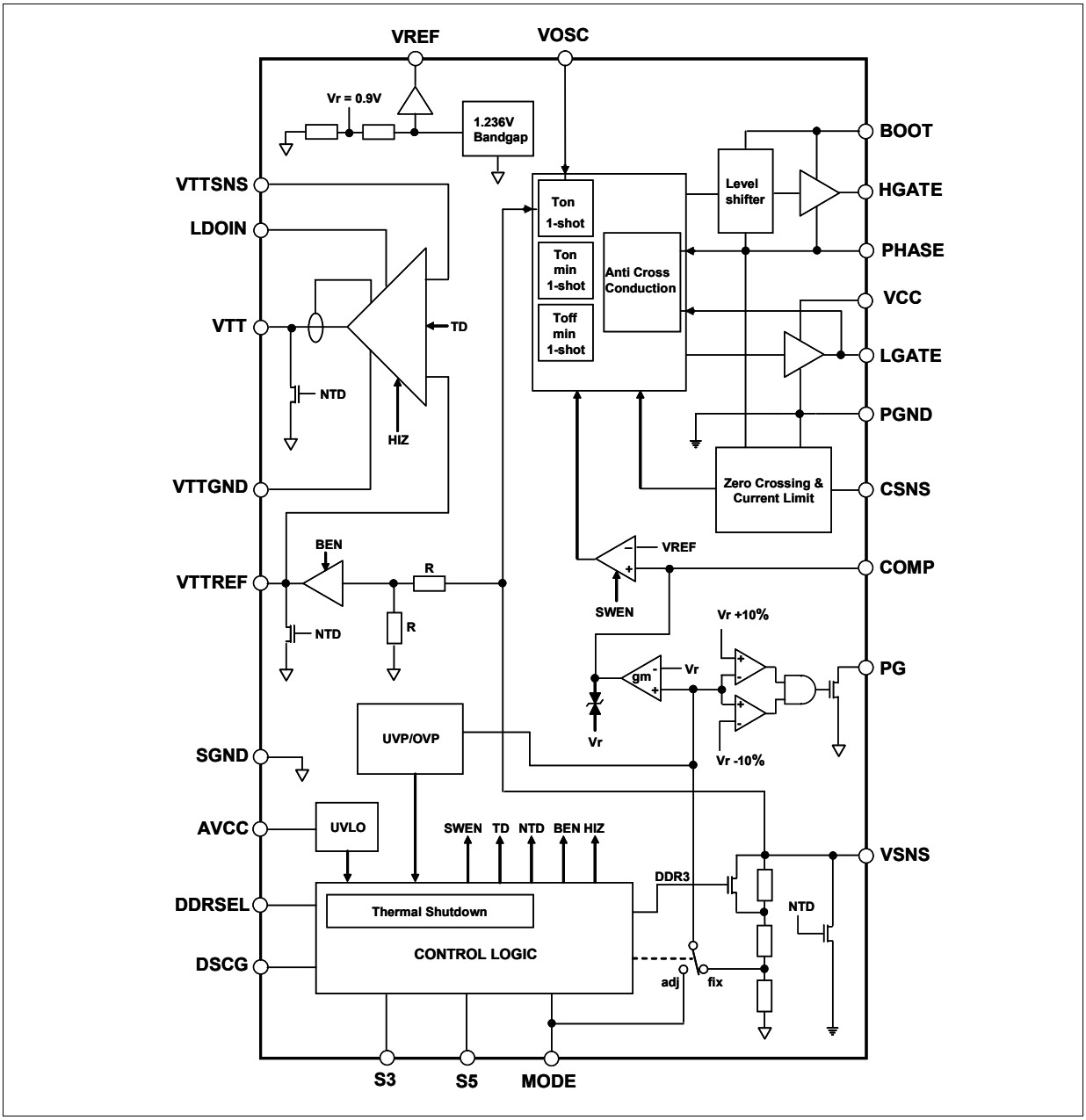


Table 7. Legend

SWEN	Switching controller enable
TD	Tracking discharge enable
NTD	Non-tracking discharge enable
BEN	VTTREF buffer enable
HIZ	LDO high impedance mode enable

7 Device description

The PM6670SS is designed to satisfy DDR2-3 power supply requirements combining a synchronous buck controller, a 15 mA buffered reference and a high-current low-drop out (LDO) linear regulator capable of sourcing and sinking up to 2 Apk. The switching controller section is a high-performance, pseudo-fixed frequency, constant-on-time (COT) based regulator specifically designed for handling fast load transient over a wide range of input voltages.

The DDR2-3 supply voltage VDDQ can be easily set to 1.8 V (DDR2) or 1.5 V (DDR3) without additional components. The output voltage can also be adjusted in the 0.9 V to 2.6 V range using an external resistor divider. The switching mode power supply (SMPS) can handle different modes of operation in order to minimize noise or power consumption, depending on the application needs.

A lossless current sensing scheme, based on the Low-Side MOSFET's on resistance avoids the need for an external current sense resistor.

The output of the linear regulator (VTT) tracks the memory's reference voltage VTTREF within ±30 mV over the full operating load conditions. The input of the LDO can be either VDDQ or a lower voltage rail in order to reduce the total power dissipation. Linear regulator stability is achieved by filtering its output with a ceramic capacitor (20 µF or greater).

The reference voltage (VTTREF) section provides a voltage equal to one half of VSNS with an accuracy of 1 %. This regulator can source and sink up to ±15 mA. A 10 nF to 100 nF bypass capacitor is required between VTTREF and SGND for stability.

According to DDR2/3 JEDEC specifications, when the system enters the suspend-to-RAM state the LDO output is left in high impedance while VTTREF and VDDQ are still alive. When the suspend-to-disk state (S3 and S5 tied to ground) is entered, all outputs are actively discharged when either tracking or non-tracking discharge is selected.

7.1 VDDQ section - constant on-time PWM controller

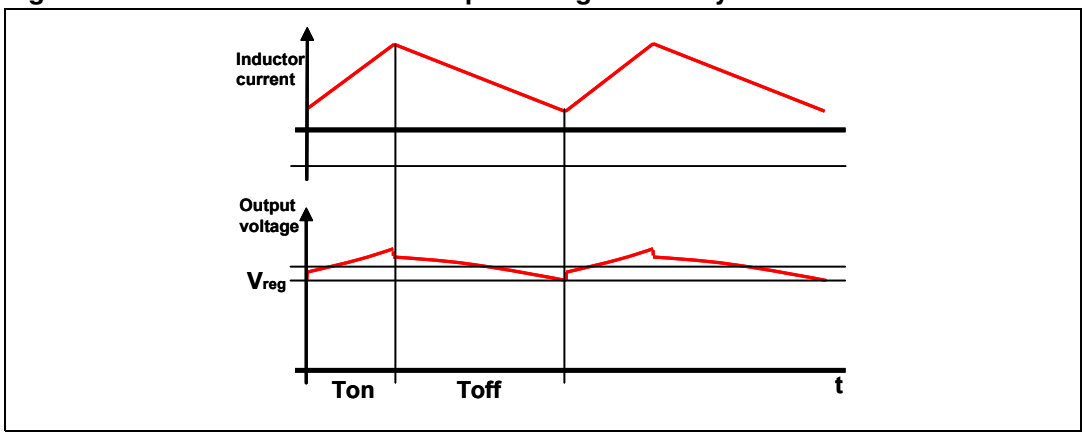
The PM6670S uses a pseudo-fixed frequency, constant on-time (COT) controller as the core of the switching section. It is well known that the COT controller uses a relatively simple algorithm and uses the ripple voltage derived across the output capacitor's ESR to trigger the on-time one-shot generator. In this way, the output capacitor's ESR acts as a current sense resistor providing the appropriate ramp signal to the PWM comparator. Nearly constant switching frequency is achieved by the system's loop in steady-state operating conditions by varying the on-time duration, avoiding thus the need for a clock generator. The on-time one shot duration is directly proportional to the output voltage, sensed at VSNS pin, and inversely proportional to the input voltage, sensed at the VOSC pin, as follows:

Equation 1

$$T_{ON} = K_{OSC} \frac{V_{SNS}}{V_{OSC}} + \tau$$

where K_{OSC} is a constant value (130 ns typ.) and τ is the internal propagation delay (40ns typ.). The one-shot generator directly drives the high-side MOSFET at the beginning of each switching cycle allowing the inductor current to increase; after the on-time has expired, an Off-Time phase, in which the low-side MOSFET is turned on, follows. The off-time duration is solely determined by the output voltage: when lower than the set value (i.e. the voltage at VSNS pin is lower than the internal reference V_R = 0.9 V), the synchronous rectifier is turned off and a new cycle begins (*Figure 28*).

Figure 28. Inductor current and output voltage in steady state conditions



The duty-cycle of the buck converter is, in steady-state conditions, given by

Equation 2

$$D = \frac{V_{OUT}}{V_{IN}}$$

The switching frequency is thus calculated as

Equation 3

$$f_{SW} = \frac{D}{T_{ON}} = \frac{\frac{V_{OUT}}{V_{IN}}}{K_{OSC}\frac{V_{SNS}}{V_{OSC}}} = \frac{\alpha_{OSC}}{\alpha_{OUT}} \cdot \frac{1}{K_{OSC}}$$

where

Equation 4a

$$\alpha_{OSC} = \frac{V_{OSC}}{V_{IN}}$$

Equation 4b

$$\alpha_{OUT} = \frac{V_{SNS}}{V_{OUT}}$$

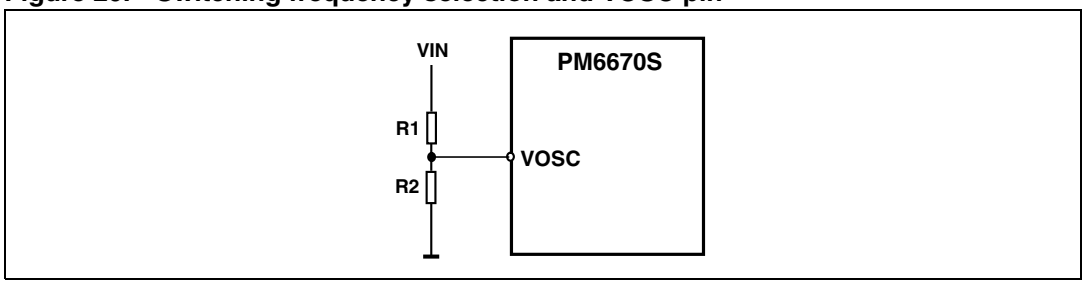
Referring to the typical application schematic (figures on cover page and *Figure 29*), the final expression is then:

Equation 5

$$f_{SW} = \frac{\alpha_{OSC}}{K_{OSC}} = \frac{R_2}{R_1 + R_2} \cdot \frac{1}{K_{OSC}}$$

Even if the switching frequency is theoretically independent from battery and output voltages, parasitic parameters involved in power path (like MOSFETs' on-resistance and inductor's DCR) introduce voltage drops responsible for slight dependence on load current. In addition, the internal delay is due to a small dependence on input voltage. The PM6670S switching frequency can be set by an external divider connected to the VOSC pin.

Figure 29. Switching frequency selection and VOSC pin



The suggested voltage range for VOSC pin is 0.3 V to 2 V, for better switching frequency programmability.

7.1.1 Constant-on-time architecture

Figure 30 shows the simplified block diagram of the constant-on-time controller.

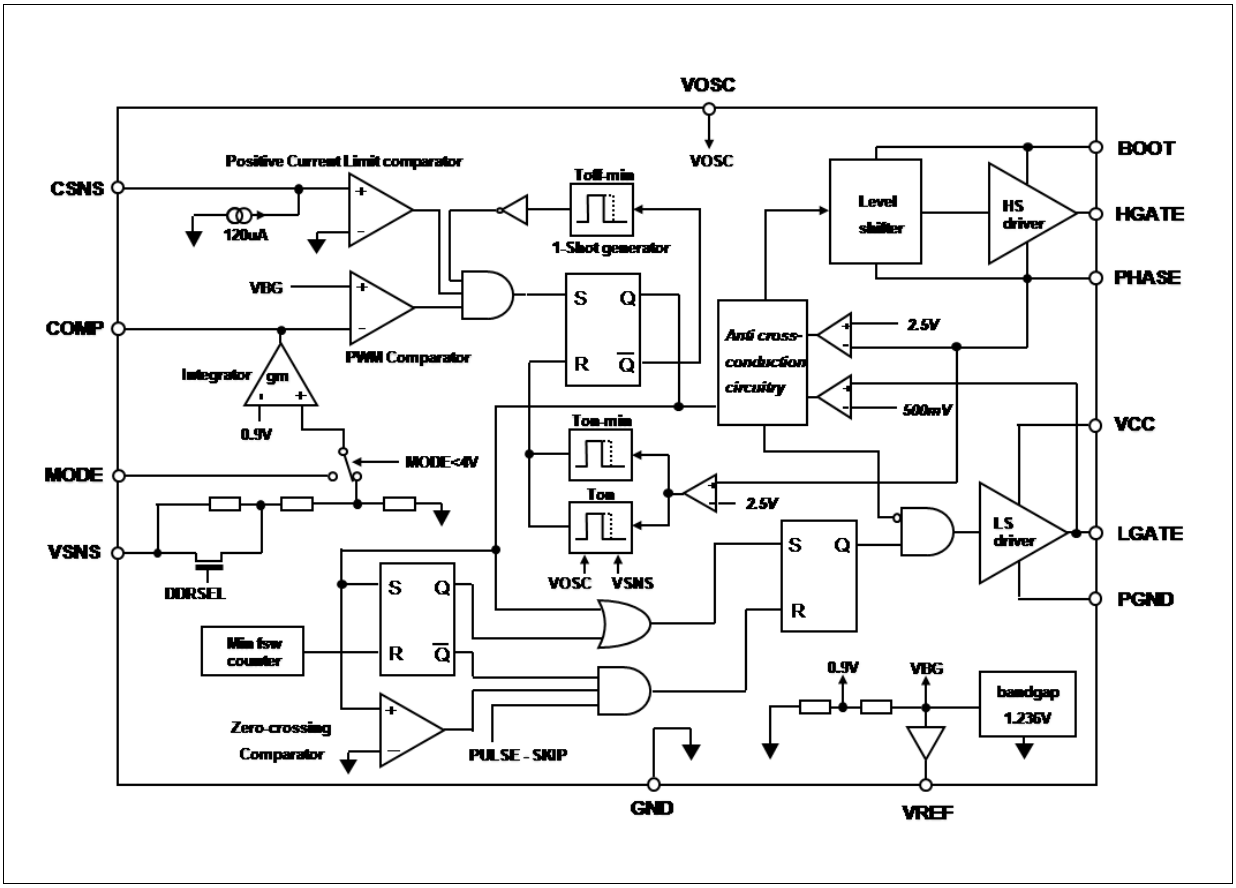
The switching regulator of the PM6670S owns a one-shot generator that ignites the high-side MOSFET when the following conditions are simultaneously satisfied: the PWM comparator is high (i.e. output voltage is lower than Vr = 0.9 V), the synchronous rectifier current is below the current limit threshold and the minimum off-time has expired.

A minimum off-time constraint (300 ns typ.) is introduced to assure the boot capacitor charge and allow inductor valley current sensing on low-side MOSFET. A minimum on-time is also introduced to assure the start-up switching sequence.

Once the on-time has timed out, the high side switch is turned off, while the synchronous rectifier is ignited according to the anti-cross conduction management circuitry.

When the output voltage reaches the valley limit (determined by internal reference Vr = 0.9 V), the low-side MOSFET is turned off according to the anti-cross conduction logic once again, and a new cycle begins.

Figure 30. Switching section simplified block diagram

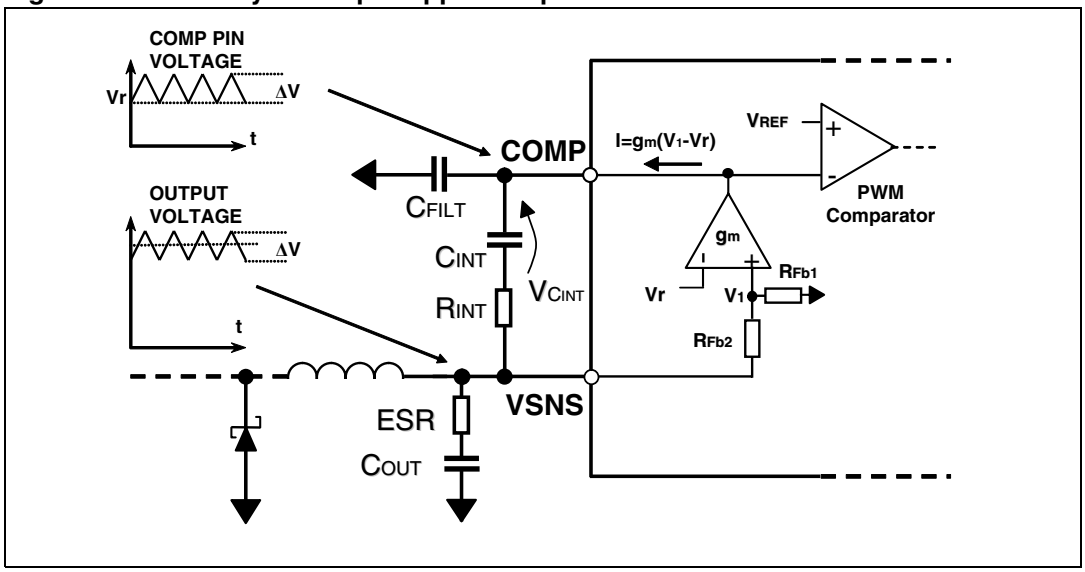


7.1.2 Output ripple compensation and loop stability

The loop is closed connecting the center tap of the output divider (internally, when the fixed output voltage is chosen, or externally, using the MODE pin in the adjustable output voltage mode). The feedback node is the negative input of the error comparator, while the positive input is internally connected to the reference voltage (Vr = 0.9 V). When the feedback voltage becomes lower than the reference voltage, the PWM comparator goes to high and sets the control logic, turning on the high-side MOSFET. After the on-time (calculated as previously described) the system releases the high-side MOSFET and turns on the synchronous rectifier.

The voltage drop along ground and supply PCB paths, used to connect the output capacitor to the load, is a source of DC error. Furthermore the system regulates the output voltage valley, not the average, as shown in *Figure 28*. Thus, the voltage ripple on the output capacitor is an additional source of DC error. To compensate this error, an integrative network is introduced in the control loop, by connecting the output voltage to the COMP pin through a capacitor (C_{INT}) as shown in *Figure 31*.

Figure 31. Circuitry for output ripple compensation



The additional capacitor is used to reduce the voltage on the COMP pin when higher than 300 mVpp and is unnecessary for most of applications. The trans conductance amplifier (gm) generates a current, proportional to the DC error, used to charge the CINT capacitor. The voltage across the CINT capacitor feeds the negative input of the PWM comparator, forcing the loop to compensate the total static error. An internal voltage clamp forces the COMP pin voltage range to ±150 mV with respect to VREF. This is useful to avoid or smooth output voltage overshoot during a load transient. When the pulse-skip mode is entered, the clamping range is automatically reduced to 60 mV in order to enhance the recovering capability. In the ripple amplitude is larger than 150 mV, an additional capacitor CFILT can be connected between the COMP pin and ground to reduce ripple amplitude, otherwise the integrator will operate out of its linearity range. This capacitor is unnecessary for most of applications and can be omitted.

The design of the external feedback network depends on the output voltage ripple. If the ripple is higher than approximately 20 mV, the correct CINT capacitor is usually enough to keep the loop stable. The stability of the system depends firstly on the output capacitor zero frequency.

The following condition must be satisfied:

Equation 6

$$f_{SW} > k \cdot f_{Zout} = \frac{k}{2\pi \cdot C_{out} \cdot ESR}$$

where k is a fixed design parameter (k > 3). It determines the minimum integrator capacitor value:

Equation 7

$$C_{INT} > \frac{g_m}{2\pi \cdot \left(\frac{f_{SW}}{k} - f_{Zout} \right)} \cdot \frac{Vr}{Vout}$$

where gm = 50 µs is the integrator trans conductance.

In order to ensure stability it must be also verified that:

Equation 8

$$C_{INT} > \frac{g_m}{2\pi \cdot f_{Zout}} \cdot \frac{Vr}{V_{OUT}}$$

If the ripple on the COMP pin is greater than the integrator 150 mV, the auxiliary capacitor C_{FILT} can be added. If q is the desired attenuation factor of the output ripple, C_{FILT} is given by:

Equation 9

$$C_{FILT} = \frac{C_{INT} \cdot (1 - q)}{q}$$

In order to reduce the noise on the COMP pin, it is possible to add a resistor R_{INT} that, together with CINT and C_{FILT}, becomes a low pass filter. The cutoff frequency f_{CUT} must be much greater (10 or more times) than the switching frequency:

Equation 10

$$R_{INT} = \frac{1}{2\pi \cdot f_{CUT} \cdot \frac{C_{INT} \cdot C_{FILT}}{C_{INT} + C_{FILT}}}$$

If the ripple is very small (lower than approximately 20 mV), a different compensation network, called “Virtual-ESR” network, is needed. This additional circuit generates a triangular ripple that is added to the output voltage ripple at the input of the integrator. The complete control scheme is shown in *Figure 32*.