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PM6675AS

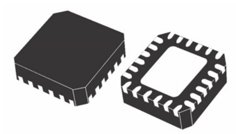
High efficiency step-down controller with embedded 2 A LDO regulator

Features

- Switching section
  - 4.5 V to 36 V input voltage range
  - 0.6 V, ±1 % voltage reference
  - Selectable 1.5 V fixed output voltage
  - Adjustable 0.6 V to 3.3 V output voltage
  - 1.237 V ±1 % reference voltage available
  - Very fast load transient response using constant-on-time control loop
  - No R_{SENSE} current sensing using low side MOSFETs' $R_{DS(ON)}$
  - Negative current limit
  - Latched OVP and UVP
  - Soft-start internally fixed at 3 ms
  - Selectable pulse skipping at light load
  - Selectable No-audible (33 kHz) pulse skip mode
  - Ceramic output capacitors supported
  - Output voltage ripple compensation
  - Output soft-end
- LDO regulator section
  - Adjustable 0.6 V to 3.3 V output voltage
  - Selectable ±1 Apk or ±2 Apk current limit
  - Dedicated power-good signal
  - Ceramic output capacitors supported
  - Output soft-end

Applications

- Industrial application on 24 V
- Graphic cards
- Embedded computer systems



VFQFPN-24 4x4

Description

The PM6675AS device consists of a single high efficiency step-down controller and an independent low drop-out (LDO) linear regulator.

The constant on-time (COT) architecture assures fast transient response supporting both electrolytic and ceramic output capacitors. An embedded integrator control loop compensates the DC voltage error due to the output ripple.

Selectable low-consumption mode allows the highest efficiency over a wide range of load conditions. The low-noise mode sets the minimum switching frequency to 33 kHz for audio-sensitive applications. The LDO linear regulator can sink and source up to 2 Apk. Two fixed current limit (±1 A- ±2 A) can be chosen.

An active soft-end is independently performed on both the switching and the linear regulators outputs when disabled.

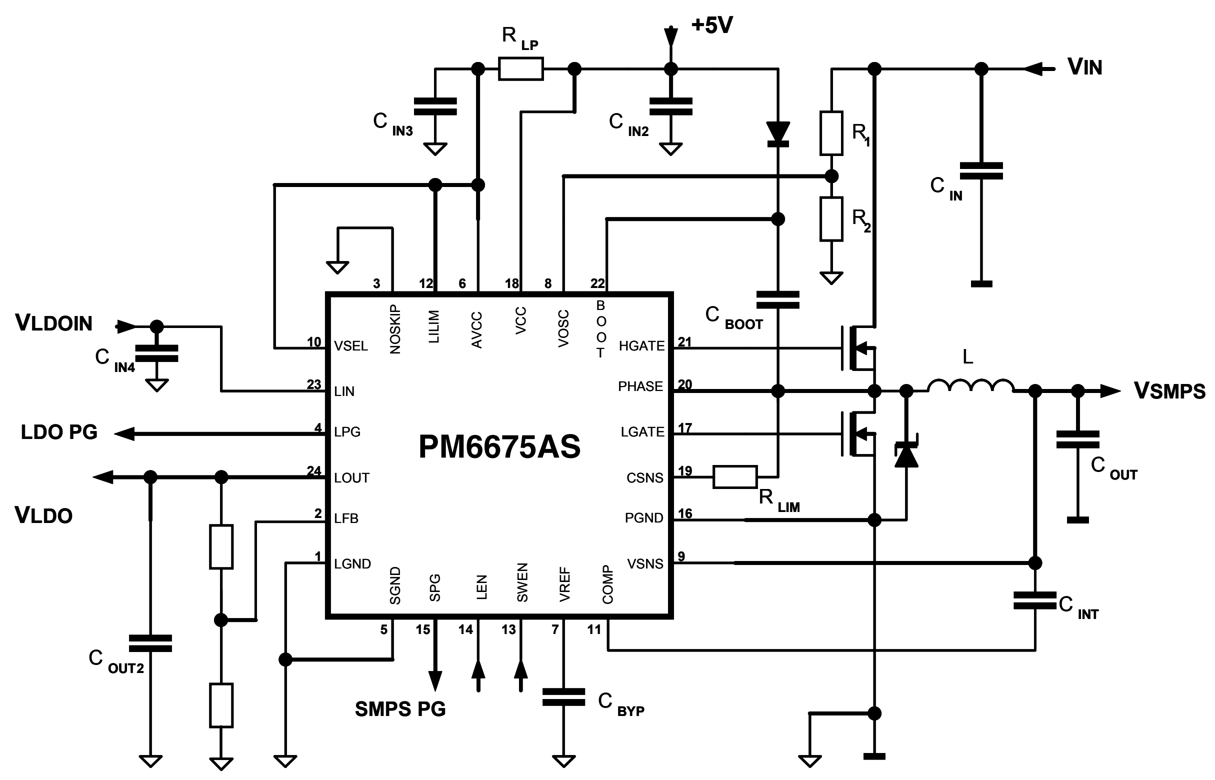
Table 1. Device summary

Order codes	Package	Packaging
PM6675AS	VFQFPN-24 4x4 (exposed pad)	Tube
PM6675ASTR		Tape and reel

Contents

1 Typical application circuit

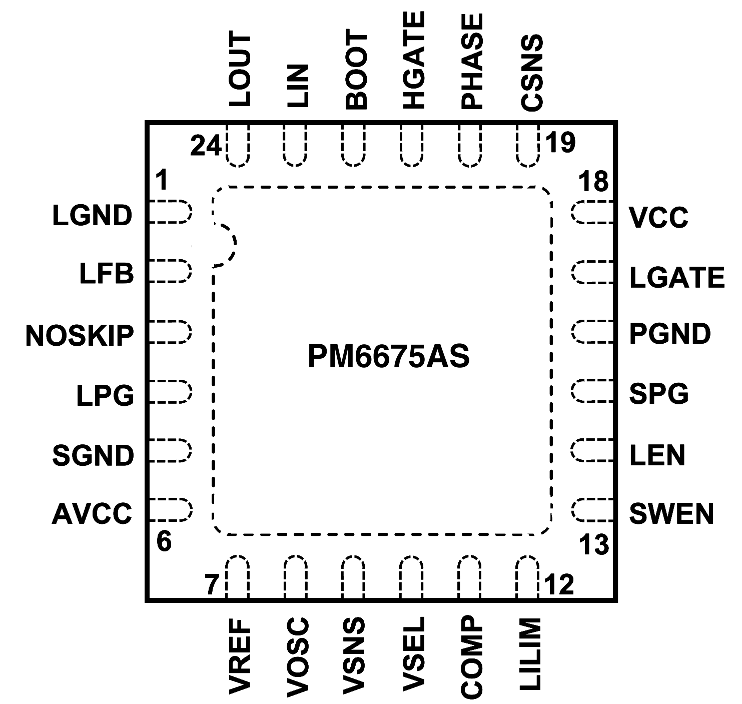
Figure 1. Application circuit



2 Pin settings

2.1 Connections

Figure 2. Pin connection (through top view)



2.2 Pin description

Table 2. Pin functions

N°	Pin	Function
1	LGND	LDO power ground. Connect to negative terminal of VTT output capacitor.
2	LFB	LDO remote sensing. Connect as close as possible to the load via a low noise PCB trace.
3	NOSKIP	Pulse-skip/no-audible pulse-skip modes selector. See *Section 7.1.4: Mode-of-operation selection*
4	LPG	LDO section power-good signal (open drain output). High when LDO output voltage is within ±10 % of nominal value.
5	SGND	Ground Reference for analog circuitry, control logic and VTTREF buffer. Connect together with the thermal pad and VTTGND to a low impedance ground plane. See the *Application Note* for details.
6	AVCC	+5 V supply for internal logic. Connect to +5 V rail through a simple RC filtering network.
7	VREF	High accuracy output voltage reference (1.237 V) for multilevel pins setting. It can deliver up to 50 uA. Connect a 100 nF capacitor between VREF and SGND in order to enhance noise rejection.
8	VOSC	Frequency Selection. Connect to the central tap of a resistor divider to set the desired switching frequency. The pin cannot be left floating. See *Section 7: Device description* for details.
9	VSNS	Switching section output remote sensing and discharge path during output soft-end. Connect as close as possible to the load via a low noise PCB trace.
10	VSEL	Fixed output selector and feedback input for the switching controller. If VSEL pin voltage is higher than 4 V, the fixed 1.5 V output is selected. If VSEL pin voltage is lower than 4 V, it is used as negative input of the error amplifier. See *Section 7.1.4: Mode-of-operation selection* for details.
11	COMP	DC voltage error compensation input pin for the switching section. Refer to Mode of Operation Selection section for more details.
12	LILIM	Current limit selector for the LDO. Connect to SGND for ±1 A current limit or to +5 V for ±2 A current limit.
13	SWEN	Switching Controller Enable. When tied to ground, the switching output is turned off and a soft-end is performed.
14	LEN	Linear Regulator Enable. When tied to ground, the LDO output is turned off and a soft-end is performed.
15	SPG	Switching Section power-good signal (open drain output). High when the switching regulator output voltage is within ±10 % of nominal value.
16	PGND	Power ground for the switching section.
17	LGATE	Low-side gate driver output.
18	VCC	+5 V low-side gate driver supply. Bypass with a 100 nF capacitor to PGND.

Table 2. Pin functions (continued)

N°	Pin	Function
19	CSNS	Current sense input for the switching section. This pin must be connected through a resistor to the drain of the synchronous rectifier (RDSon sensing) to set the current limit threshold.
20	PHASE	Switch node connection and return path for the high side gate driver.
21	HGATE	High-Side Gate Driver Output
22	BOOT	Bootstrap capacitor connection. Input for the supply voltage of the high-side gate driver.
23	LIN	Linear Regulator Input. Bypass to LGND by a 10 µF ceramic capacitor for noise rejection enhancement.
24	LOUT	LDO linear regulator output. Bypass with a 20 µF (2x10 µF MLCC) filter capacitor.

3 Electrical data

3.1 Maximum rating

Table 3. Absolute maximum ratings [(1)]

Symbol	Parameter	Value	Unit
V_{AVCC}	AVCC to SGND	-0.3 to 6	V
V_{VCC}	VCC to SGND	-0.3 to 6	
	PGND, LGND to SGND	-0.3 to 0.3	
	HGATE and BOOT to PHASE	-0.3 to 6	
	HGATE and BOOT to PGND	-0.3 to 44	
V_{PHASE}	PHASE to SGND	-0.3 to 38	
	LGATE to PGND	-0.3 to V_{VCC} +0.3	
	CSNS, SPG, LEN, SWEN, LILIM, COMP, VSEL, VSNS, VOSC, VREF, NOSKIP to SGND	-0.3 to V_{AVCC} + 0.3	
	LPG,VREF, LOUT, LFB to SGND	-0.3 to V_{AVCC} + 0.3	
	LIN, LOUT, LPG, LIN to LGND	-0.3 to V_{AVCC} + 0.3	
P_{TOT}	Power dissipation @T_A = 25°C	2.3	W

1. Free air operating conditions unless otherwise specified. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	42	°C/W
T_{STG}	Storage temperature range	-50 to 150	°C
T_A	Operating ambient temperature range	-40 to 85	
T_J	Junction operating temperature range	-40 to 125	

3.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Input voltage range	4.5		36	V
V_{AVCC}	IC supply voltage	4.5		5.5	
V_{VCC}	IC supply voltage	4.5		5.5	

4 Electrical characteristics

Table 6. Electrical characteristics
T_A = - 25 °C to 85 °C , VCC = AVCC = +5 V, LIN = 1.5 V and LOUT= 0.6 V if not otherwise specified [1].

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
Supply section							
I_{IN}	Operating current (Switching + LDO)	SWEN, LEN, VSEL and NOSKIP connected to AVCC, No load on LOUT output.				2	mA
I_{SW}	Operating current (switching)	SWEN, VSEL and NOSKIP connected to AVCC, LEN coneected to SGND.				1	mA
I_{SHDN}	Shutdown operating current	SWEN and LEN tied to SGND.				10	µA
UVLO	AVCC Under Voltage Lockout upper threshold			4.1	4.25	4.4	V
UVLO	AVCC Under Voltage Lockout lower threshold			3.85	4.0	4.1	V
UVLO	UVLO hysteresis			70			mV
On-time (SMPS)							
t_{ON}	On-time duration	VSEL low, NOSKIP low, VVSNS = 2 V	V_{OSC} = 300 mV	530	630	730	ns
t_{ON}	On-time duration	VSEL low, NOSKIP low, VVSNS = 2 V	V_{OSC} = 500 mV	320	380	440	ns
OFF-TIME (SMPS)							
t_{OFFMIN}	Minimum Off-Time				300	350	ns
Voltage reference							
	Voltage accuracy	4.5 V< V_{IN} < 36 V		1.224	1.237	1.249	V
	Load regulation	-50 µA < I_{VREF} < 50 µA		-4		4	mV
	Undervoltage Lockout Fault Threshold				800		mV
SMPS output							
V_{OUT}	SMPS fixed output voltage	VSEL connected to AVCC, NOSKIP tied to SGND, No Load			1.5		V
	Feedback output voltage accuracy	VSEL connected to AVCC, NOSKIP tied to SGND, No Load		-1.5		1.5	%

Table 6. Electrical characteristics (continued)
T_A = -25 °C to 85 °C , VCC = AVCC = +5 V, LIN = 1.5 V and LOUT= 0.6 V if not otherwise specified. (1)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Current limit and zero crossing comparator						
I_{CSNS}	CSNS input bias current		90	100	110	µA
	Comparator offset		-6		6	mV
	Positive current limit threshold	V_{PGND} - V_{CSNS}		100		
	fixed negative current limit threshold			110		
$V_{ZC,OFFS}$	Zero crossing comparator offset		-11	-5	1	
High and low side gate drivers						
	HGATE driver on-resistance	HGATE high state (pullup)		2.0	3	Ω
		HGATE low state (pulldown)		1.8	2.7	
	LGATE driver on-resistance	LGATE high state (pullup)		1.4	2.1	
		LGATE low state (pulldown)		0.6	0.9	
UVP/OVP protections and PGOOD signals						
OVP	Over voltage threshold		112	115	118	%
UVP	Under voltage threshold		67	70	73	
PGOOD	SMPS upper threshold		107	110	113	
	SMPS lower threshold		86	90	93	
	LDO upper threshold		107	110	113	
	LDO lower threshold		86	90	93	
$I_{PG,LEAK}$	SPG and LPG leakeage current	SPG and LPG forced to 5.5 V			1	µA
$V_{PG,LOW}$	SPG and LPG low level voltage	$I_{LPG,SINK} = I_{SPG,SINK} = 4$ mA		150	250	mV
Soft-start section (SMPS)						
	Soft-start ramp time (4 steps current limit)		2	3	4	ms
	Soft-start current limit step			25		µA
Soft end section						
	Switching section discharge resistance		15	25	35	Ω
	LDO section discharge resistance		15	25	35	
LDO section						
V_{LREF}	LDO reference voltage			600		mV
	LDO output accuracy respect to VREF	-1 mA < I_{LDO} < 1 mA	-20		20	
		-1 A < I_{LDO} < 1 A	-25		25	

Table 6. Electrical characteristics (continued)
T_A = -25 °C to 85 °C , VCC = AVCC = +5 V, LIN = 1.5 V and LOUT= 0.6 V if not otherwise specified. (1)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$I_{LDO,CL}$	LDO sink current limit	$V_{LFB} > V_{LREF}$, LILIM = 5 V	-3	-2.3	-2	A
		$V_{LFB} > V_{LREF}$, LILIM = 0 V	-1.6	-1.3	-1	
	LDO source current limit	$0.9 \cdot V_{LREF} < V_{LFB} < V_{LREF}$, LILIM=5V	2	2.4	3	
		$0.9 \cdot V_{LREF} < V_{LFB} < V_{LREF}$, LILIM = 0 V	1	1.3	1.6	
		$V_{LFB} < 0.9 \cdot V_{LREF}$, LILIM = 5 V	1	1.3	1.6	
		$V_{LFB} < 0.9 \cdot V_{LREF}$, LILIM = 0 V	0.5	0.8	1.1	
$I_{LIN,BIAS}$	LDO input bias current, on	LEN connected to AVCC, no load		1	10	µA
	LDO input bias current, off	LEN = 0 V, no load			1	
$I_{LFB,BIAS}$	LFB input bias current	LEN connected to AVCC VLFB = 0.6 V	-1		1	
$I_{LFB,LEAK}$	LFB leakage current	LEN=0V, V_{LFB} = 0.6V	-1		1	
Power management section						
$V_{VTHVSEL}$	VSEL pin thresholds	Fixed mode	V_{AVCC} -0.7			V
		Adjustable mode			V_{AVCC} -1.3	
$V_{VTHNOSKIP}$	NOSKIP pin thresholds	Forced-PWM mode	V_{AVCC} -0.8			
		No-audible mode	1.0		V_{AVCC} -1.5	
		Pulse-skip mode			0.5	
V_{VTHLEN}, $V_{VTHSWEN}$	LEN, SWEN turn off level		0.4			
	LEN, SWEN turn on level				1.6	
$V_{VTHLILIM}$	LILIM pin thresholds	±2A LDO current limit	V_{AVCC} -0.8			
		±1A LDO current limit			0.5	
$I_{IN,LEAK}$	Logic input leakage current	LEN, SWEN and LILIM = 5 V			10	µA
$I_{IN3,LEAK}$	Multilevel input leakage current	VSEL and NOSKIP = 5 V			10	
$I_{OSC,LEAK}$	VOSC pin leakage current	VOSC = 1 V			1	
Thermal shutdown						
T_{SHDN}	Shutdown temperature (2)			150		°C

1. Specifications referred to $T_J = T_A$. All the parameters at operating temperatures extremes are guaranteed by design and statistical correlation (not production tested).
2. Guaranteed by design. Not production tested.

5 Block diagram

Figure 3. Functional and block diagram

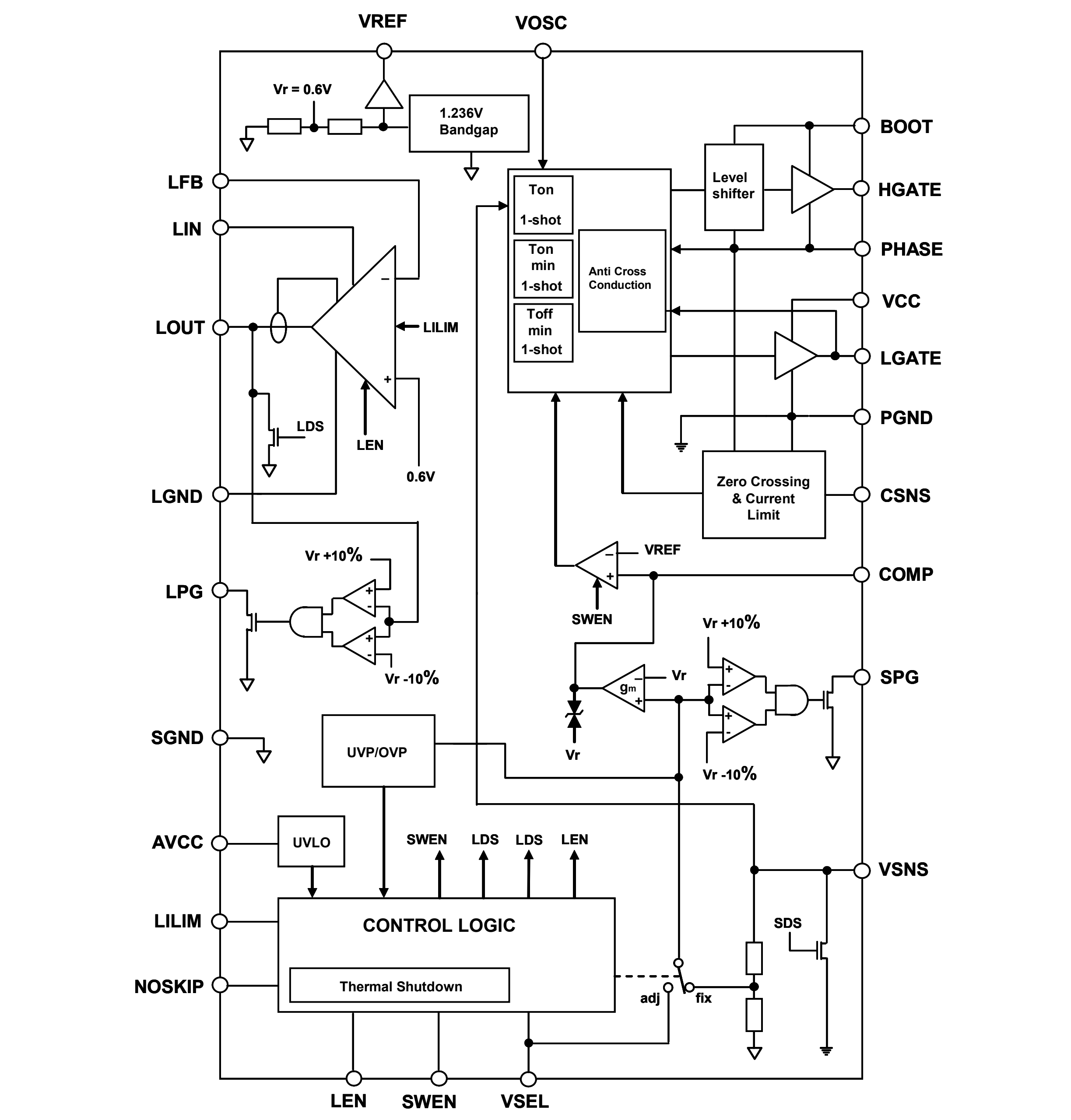


Table 7. Legend

SWEN	Switching controller enable
LEN	LDO regulator enable
LDS	LDO output discharge enable
SDS	Switching output discharge enable
LILIM	LDO regulator current limit

6 Typical operating characteristics

Figure 4. Efficiency vs output load F_{SW} = 330 kHz VOUT=1.5 V, VIN = 24 V

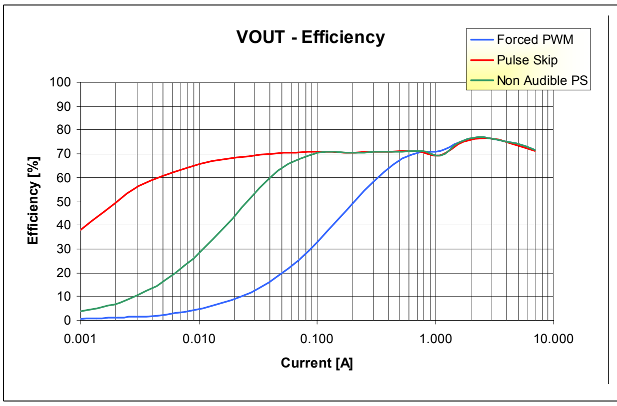


Figure 5. Switching frequency vs output current, VOUT = 1.5 V, VIN = 24 V

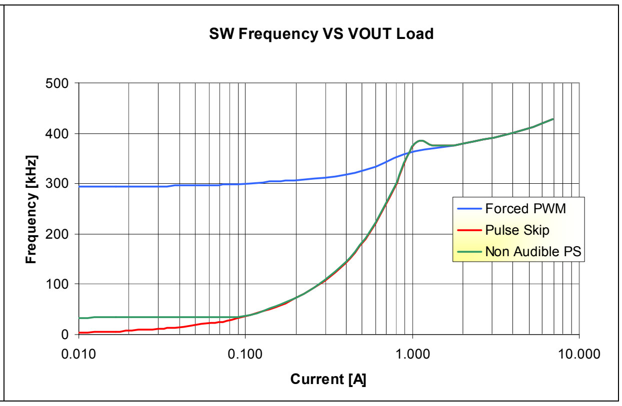


Figure 6. Switching frequency vs input voltage, VOUT = 1.5 V, IVOUT = 2 A, forced PWM mode

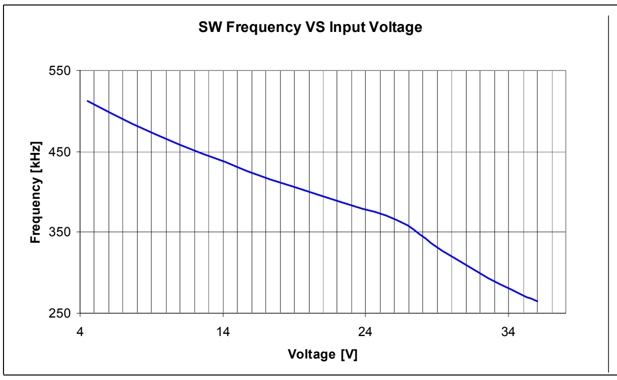


Figure 7. VOUT load regulation, VIN = 24 V

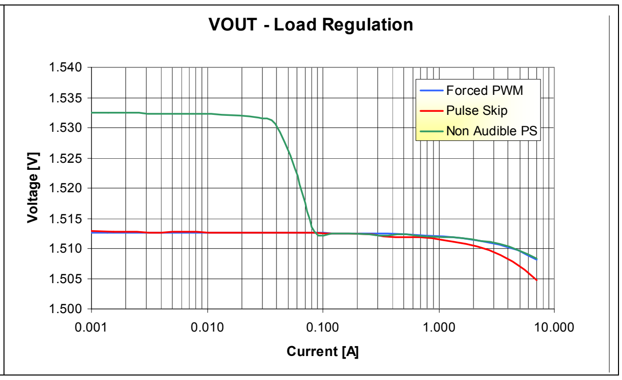


Figure 8. LOUT load regulation LDOIN = VOUT, VOUT in forced PWM mode

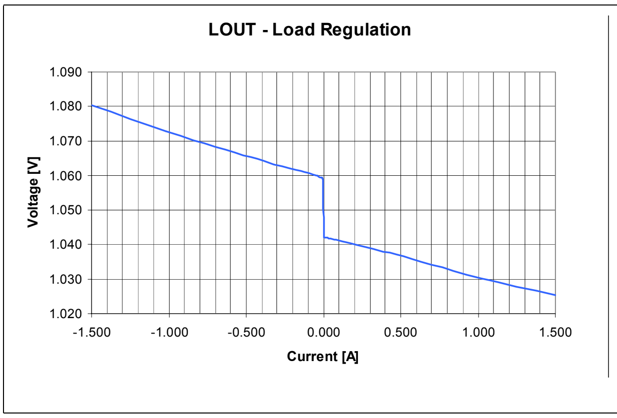


Figure 9. VOUT = 1.5 V, VIN = 24 V, IVOUT = 0 A, pulse-skip mode

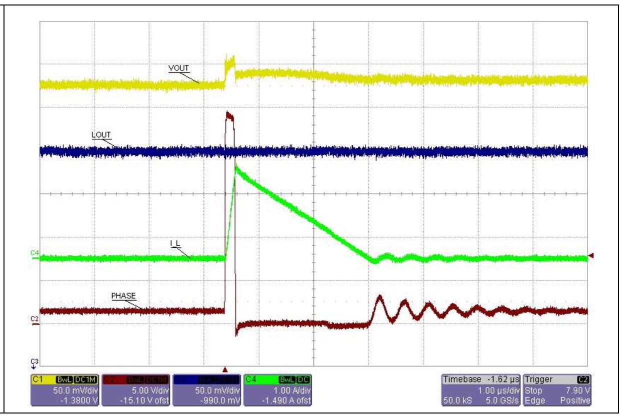


Figure 10. VOUT = 1.5V , VIN = 24V, IVOUT = 0 A, forced-PWM mode

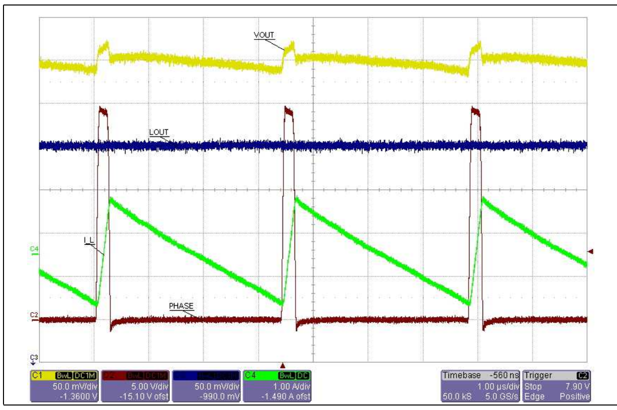


Figure 11. VOUT = 1.5 V, VIN = 24 V, no load, Non-audible pulse-skip mode (33 kHz)

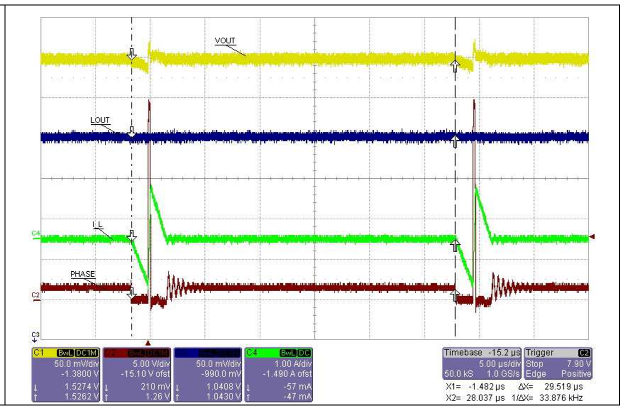


Figure 12. VOUT Soft-start @150mΩ load, pulse-skip mode

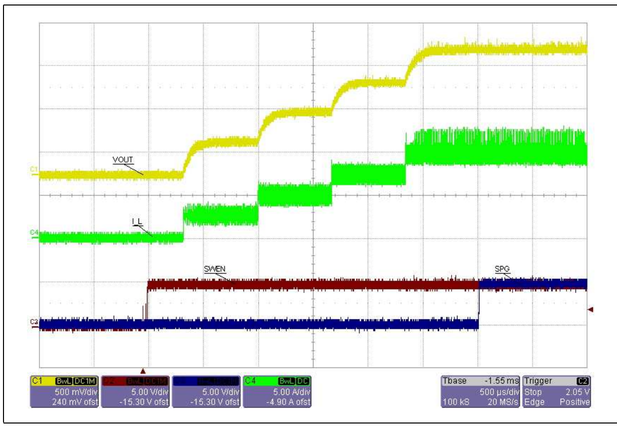


Figure 13. LOUT turn on, VOUT in pulse-skip mode

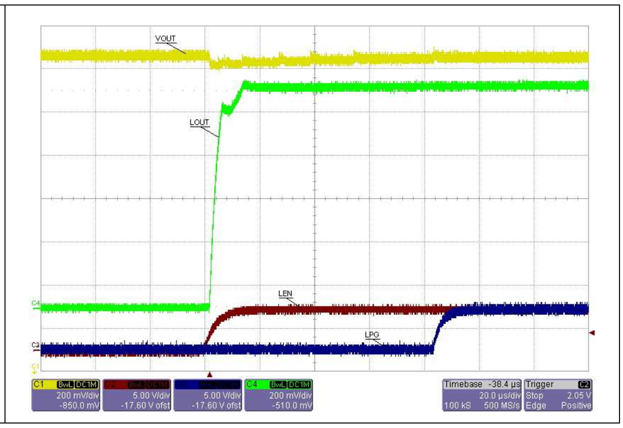


Figure 14. VOUT Load Transient (VIN = 24 V, LOAD = 0 A -> 7 A @2.5 A/µs). pulse-skip mode

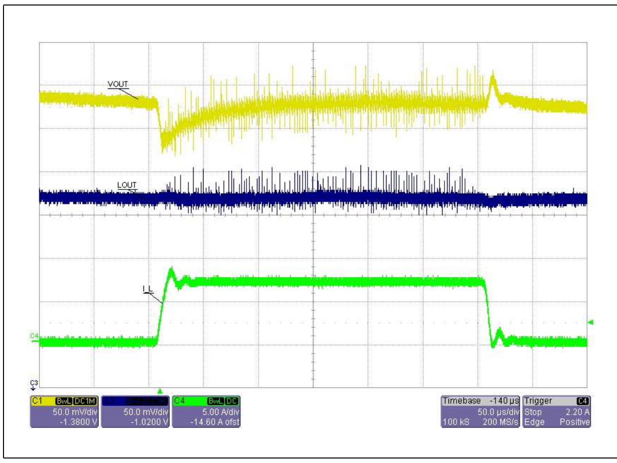


Figure 15. LOUT load transient (VIN = 24 V, LOAD = -1.5 A -> 1.5 A @2.5 A/µs). pulse-skip mode

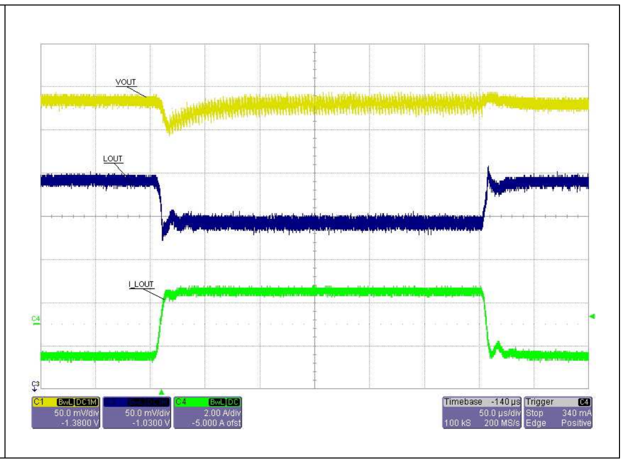


Figure 16. VOUT and LOUT output voltages. VOUT soft-end. LOUT powered by an auxiliary rail

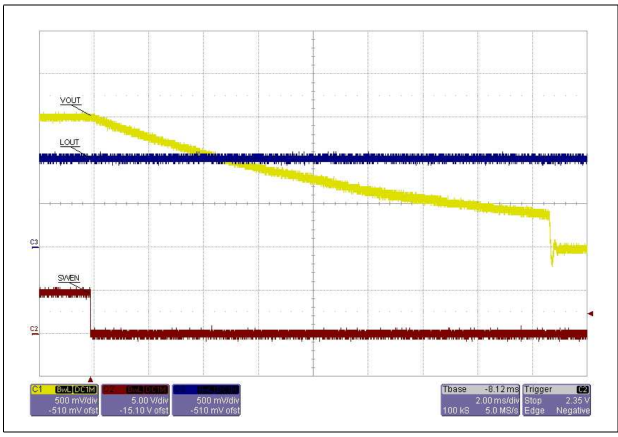


Figure 17. VOUT and LOUT output voltages LOUT soft-end

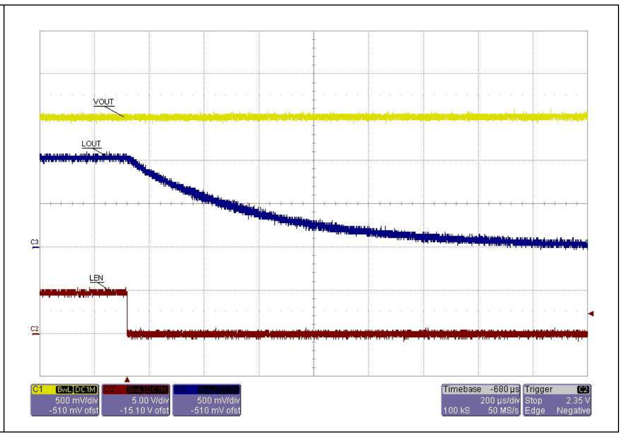


Figure 18. UV protection, pulse-skip mode LOUT powered by an auxiliary rail

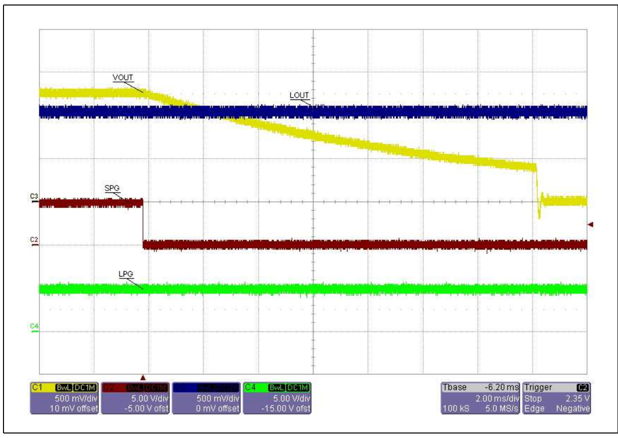


Figure 19. OV protection, pulse-skip mode

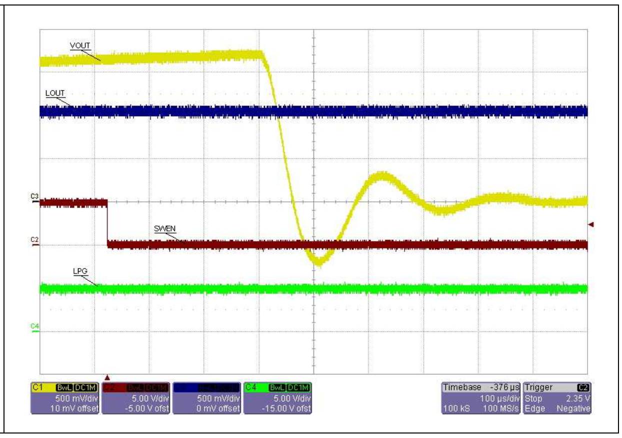


Figure 20. VOUT current limit protection during a load transient (0 A to 9 A @2.5A/µs)

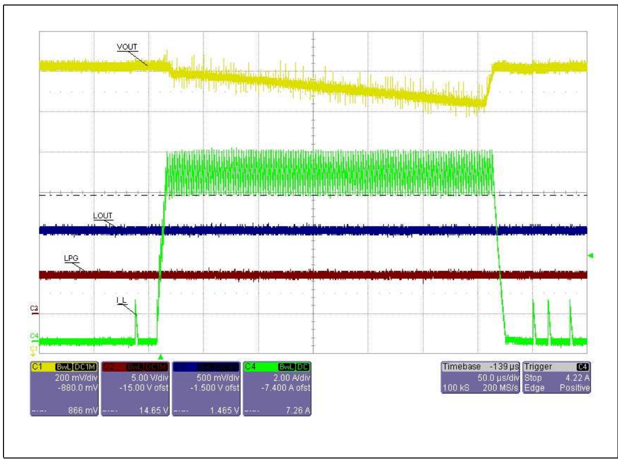
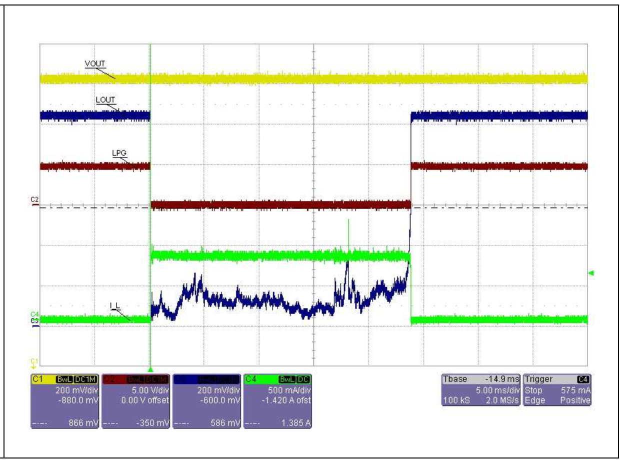


Figure 21. LOUT current limit during an output short



7 Device description

The PM6675AS combines a single high efficiency step-down controller and an independent Low Drop-Out (LDO) linear regulator in the same package.

The switching controller section is a high-performance, pseudo-fixed frequency, Constant-On-Time (COT) based regulator specifically designed for handling fast load transient over a wide range of input voltage.

The switching section output can be easily set to a fixed 1.5 V voltage without additional components or adjusted in the 0.6 V to 3.3 V range using an external resistor divider. The Switching Mode Power Supply (SMPS) can handle different modes of operation in order to minimize noise or power consumption, depending on the application needs. Selectable low-consumption and low-noise modes allow the highest efficiency and a 33 kHz minimum switching frequency respectively at light loads.

The current sensing is lossless, based on the Low-Side MOSFET turn-on resistance.

The input of the LDO can be either the switching section output or a lower voltage rail in order to reduce the total power dissipation. Linear regulator stability is achieved by filtering its output with a ceramic capacitor (20 µF or greater). The LDO linear regulator can sink and source up to 2 Apk.

Two fixed current limit (±1A-±2A) can be chosen.

An active soft-end is independently performed on both the switching and the linear regulators outputs when disabled.

7.1 Switching section - constant on-time pwm controller

The PM6675AS employes a pseudo-fixed frequency, Constant On-Time (COT) controller as the core of the switching section. As well known, the COT controller concerns of a relatively simple algorithm and uses the ripple voltage derived across the output capacitor ESR to trigger the On-Time one-shot generator. In this way, the output capacitor ESR acts as a current sense resistor providing the appropriate ramp signal to the PWM comparator. Nearly constant switching frequency is achieved by the system loop in steady-state operating conditions by varying the On-Time duration, avoiding thus the need for a clock generator. The On-Time one shot duration is directly proportional to the output voltage, sensed at VSNS pin, and inversely proportional to the input voltage, sensed at the VOSC pin, as follows:

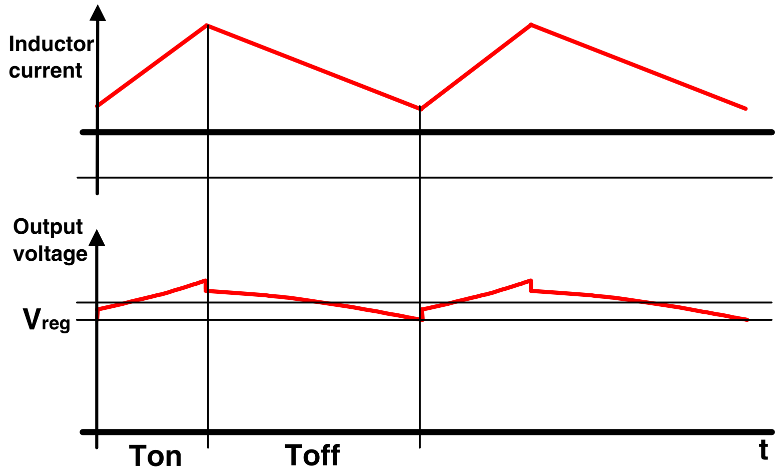
Equation 1

$$T_{ON} = K_{OSC}\frac{V_{SNS}}{V_{OSC}} + \tau$$

where K_{OSC} is a constant value (130 ns typ.) and τ is the internal propagation delay (40ns typ.). The one-shot generator directly drives the high-side MOSFET at the beginning of each switching cycle allowing the inductor current to increase; after the On-Time has expired, an Off-Time phase, in which the low-side MOSFET is turned on, follows.

The Off-Time duration is solely determined by the output voltage: when lower than the set value (i.e. the voltage at VSNS pin is lower than the internal reference = 0.6 V), the synchronous rectifier is turned off and a new cycle begins (*Figure 22*).

Figure 22. Inductor current and output voltage in steady state conditions



The duty-cycle of the buck converter is, in steady-state conditions, given by

Equation 2

$$D = \frac{V_{OUT}}{V_{IN}}$$

The switching frequency is thus calculated as

Equation 3

$$f_{SW} = \frac{D}{T_{ON}} = \frac{\frac{V_{OUT}}{V_{IN}}}{K_{OSC}\frac{V_{SNS}}{V_{OSC}}} = \frac{\alpha_{OSC}}{\alpha_{OUT}} \cdot \frac{1}{K_{OSC}}$$

where

Equation 4 a

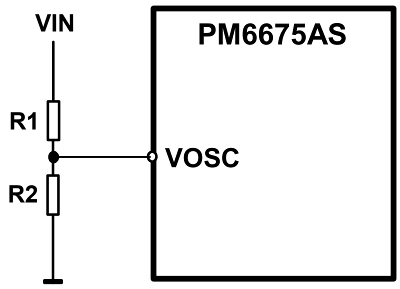
$$\alpha_{OSC} = \frac{V_{OSC}}{V_{IN}}$$

Equation 4 b

$$\alpha_{OUT} = \frac{V_{SNS}}{V_{OUT}}$$

Referring to the typical application schematic (fig. 1 and 23), the final expression is then:

Figure 23. Switching frequency selection and VOSC pin



Equation 5

$$f_{SW} = \frac{\alpha_{OSC}}{K_{OSC}} = \frac{R_2}{R_1 + R_2} \cdot \frac{1}{K_{OSC}}$$

Even if the switching frequency is theoretically independent from input and output voltages, parasitic parameters involved in power path (like MOSFET on-resistance and inductor DCR) introduce voltage drops responsible of a slight dependence on load current.

In addition, the internal delay is cause of a light dependence from input voltage.

The PM6675AS switching frequency can be set by an external divider connected to the VOSC pin.

The voltage seen at this pin must be greater than 0.8 V and lower than 2 V in order to ensure system's linearity.

7.1.1 Constant-on-time architecture

Figure 24 shows the simplified block diagram of the Constant-On-Time controller.

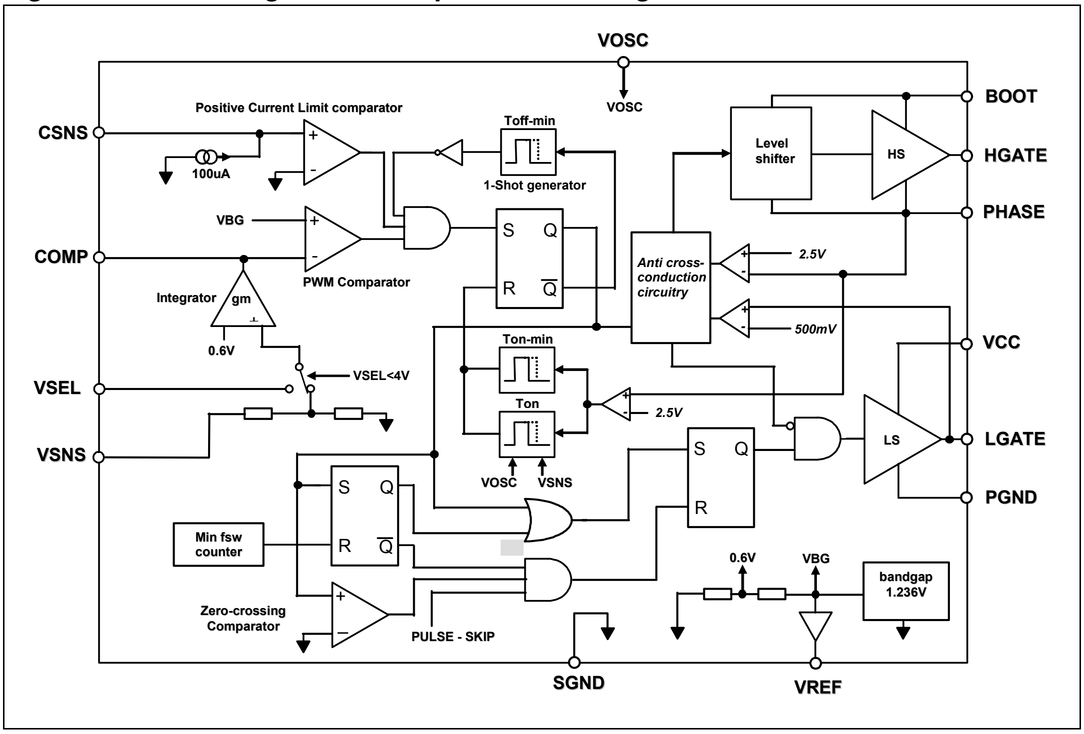
The switching regulator of the PM6675AS owns a one-shot generator that turns on the high-side MOSFET when the following conditions are simultaneously satisfied: the PWM comparator is high (i.e. output voltage is lower than Vr = 0.6 V), the synchronous rectifier current is below the current limit threshold and the minimum off-time has expired.

A minimum off-time constrain (300 ns typ.) is introduced to assure the boot capacitor charge and allow inductor valley current sensing on low-side MOSFET. A minimum On-Time is also introduced to assure the start-up switching sequence.

Once the on-time has timed out, the high side switch is turned off, while the synchronous rectifier is ignited according to the anti-cross conduction management circuitry.

When the output voltage reaches the valley limit (determined by internal reference Vr=0.6 V), the low-side MOSFET is turned off according to the anti-cross conduction logic once again, and a new cycle begins.

Figure 24. Switching section simplified block diagram

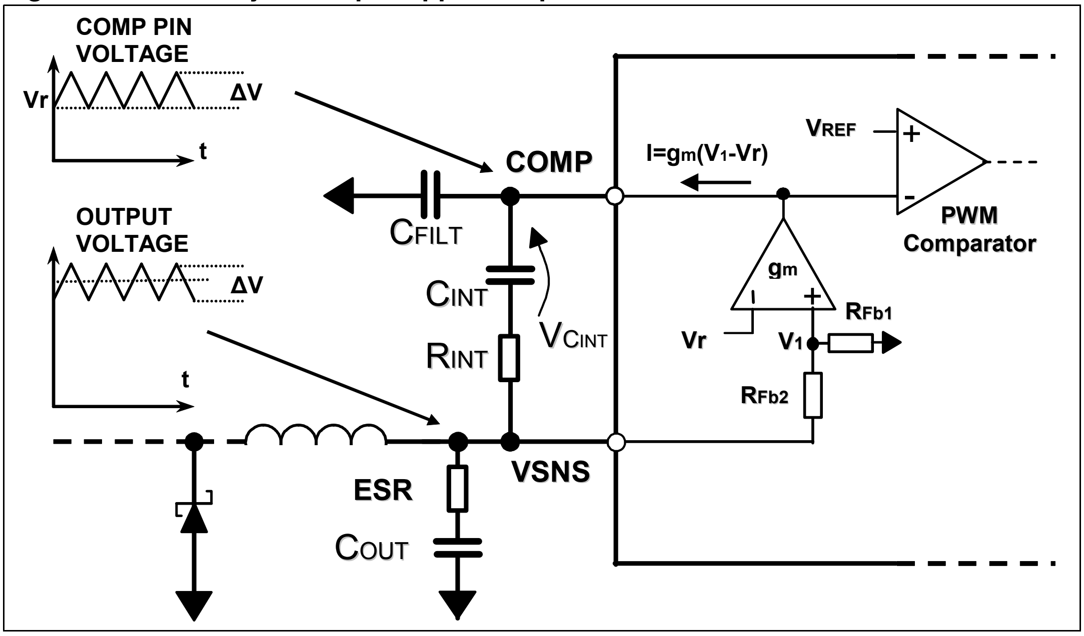


7.1.2 Output ripple compensation and loop stability

The loop is closed connecting the center tap of the output divider (internally, when the fixed output voltage is chosen, or externally, using the VSEL pin in the adjustable output voltage mode). The feedback node is the negative input of the error comparator, while the positive input is internally connected to the reference voltage (Vr = 0.6 V). When the feedback voltage becomes lower than the reference voltage, the PWM comparator goes high and sets the control logic, turning on the high-side MOSFET. After the On-Time (calculated as previously described) the system releases the high-side MOSFET and turns-on the synchronous rectifier.

The voltage drop along ground and supply PCB paths, used to connect the output capacitor to the load, is a source of DC error. Further the system regulates the output voltage valley, not the average, as shown in *Figure 22*. Thus, the voltage ripple on the output capacitor is an additional source of DC error. To compensate this error, an integrative network is introduced in the control loop, by connecting the output voltage to the COMP pin through a capacitor (CINT) as shown in *Figure 25*.

Figure 25. Circuitry for output ripple compensation



The additional capacitor is used to reduce the voltage on the COMP pin when higher than 300 mVpp and is unnecessary for most of applications. The transconductance amplifier (gm) generates a current, proportional to the DC error, used to charge the CINT capacitor. The voltage across the C_{INT} capacitor feeds the negative input of the PWM comparator, forcing the loop to compensate the total static error. An internal voltage clamp forces the COMP pin voltage range to ±150 mV respect to VREF. This is useful to avoid or smooth output voltage overshoot during a load transient. When the Pulse-Skip Mode is entered, the clamping range is automatically reduced to 60 mV in order to enhance the recovering capability. In case the ripple amplitude is larger than 150 mV, an additional capacitor C_{FILT} can be connected between the COMP pin and ground to reduce ripple amplitude, otherwise the integrator will operate out of its linearity range. This capacitor is unnecessary for most of applications and can be omitted.

The design of the external feedback network depends on the output voltage ripple. If the ripple is higher than approximately 20 mV, the correct C_{INT} capacitor is usually enough to keep the loop stable. The stability of the system depends firstly on the output capacitor zero frequency.

The following condition must be satisfied:

Equation 6

$$f_{SW} > k \times f_{Zout} = \frac{k}{2\pi \times C_{out} \times ESR}$$

where k is a fixed design parameter (k > 3). It determinates the minimum integrator capacitor value:

Equation 7

$$C_{INT} > \frac{g_m}{2\pi \cdot \left(\frac{f_{SW}}{k} - f_{Zout}\right)} \cdot \frac{Vr}{Vout}$$

where gm = 50 µs is the integrator transconductance.

If the ripple on the COMP pin is greater than the integrator 150 mV, the auxiliary capacitor C_{FILT} can be added. If q is the desired attenuation factor of the output ripple, C_{FILT} is given by:

Equation 8

$$C_{FILT} = \frac{C_{INT} \cdot (1 - q)}{q}$$

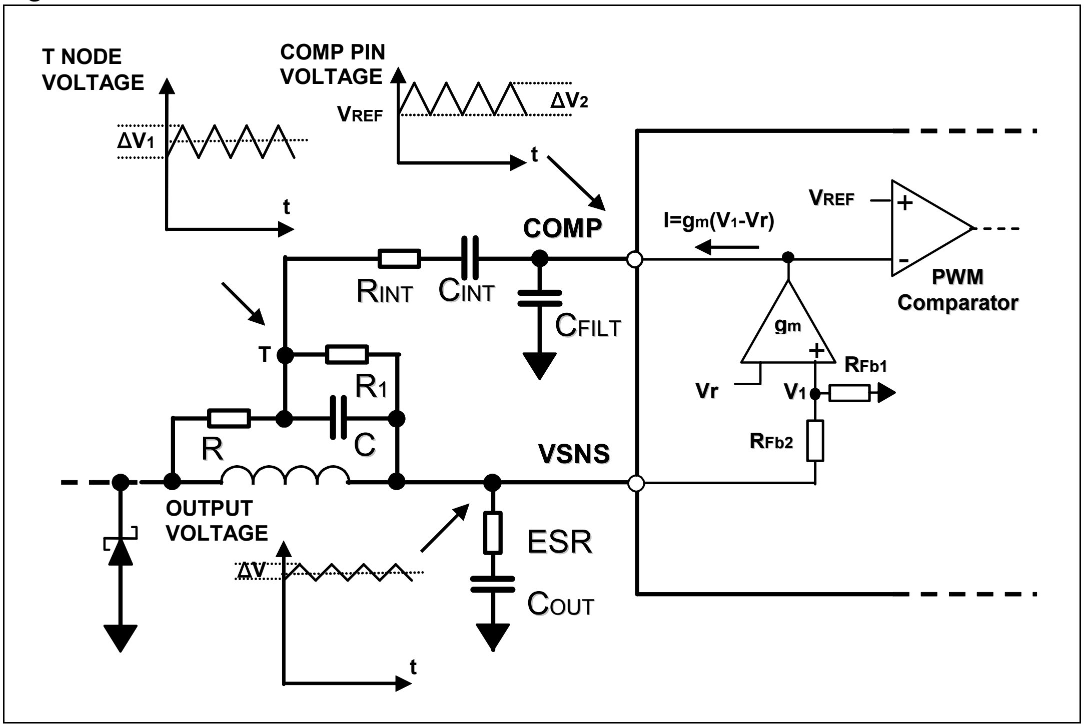
In order to reduce the noise on the COMP pin, it is possible to add a resistor R_{INT} that, together with C_{INT} and C_{FILT}, realizes a low pass filter. The cutoff frequency f_{CUT} must be greater (10 or more times) than the switching frequency:

Equation 9

$$R_{INT} = \frac{1}{2\pi \cdot f_{CUT} \cdot \frac{C_{INT} \cdot C_{FILT}}{C_{INT} + C_{FILT}}}$$

If the ripple is very small (lower than approximately 20 mV), a different compensation network, called "Virtual-ESR" Network, is needed. This additional circuit generates a triangular ripple that is added to the output voltage ripple at the input of the integrator. The complete control scheme is shown in *Figure 26*.

Figure 26. "Virtual-ESR" network



The ripple on the COMP pin is the sum of the output voltage ripple and the triangular ripple generated by the Virtual-ESR Network. In fact the Virtual-ESR Network behaves like a further equivalent series resistor RVESR.

A good trade-off is to design the network in order to achieve an RVESR given by:

Equation 10

$$R_{VESR} = \frac{V_{RIPPLE}}{\Delta I_L} - ESR$$

where ΔIL is the inductor current ripple and VRIPPLE is the total ripple at the T node, chosen greater than approximately 20 mV.

The new closed-loop gain depends on C_{INT}. In order to ensure stability it must be verified that:

Equation 11

$$C_{INT} > \frac{g_m}{2\pi \cdot f_Z} \cdot \frac{Vr}{Vout}$$

where:

Equation 12

$$f_Z = \frac{1}{2\pi \cdot C_{out} \cdot R_{TOT}}$$

and

Equation 13

$$R_{TOT} = ESR + R_{VERS}$$

Moreover, the C_{INT} capacitor must meet the following condition:

Equation 14

$$f_{SW} > k \cdot f_Z = \frac{k}{2\pi \cdot C_{out} \cdot R_{TOT}}$$

where R_{TOT} is the sum of the ESR of the output capacitor and the equivalent ESR given by the Virtual-ESR Network (R_{VESR}). The k parameter must be greater than unity (k > 3) and determines the minimum integrator capacitor value C_{INT}:

Equation 15

$$C_{INT} > \frac{g_m}{2\pi \cdot \left(\frac{f_{SW}}{k} - f_Z\right)} \cdot \frac{Vr}{Vout}$$

The capacitor of the Virtual-ESR Network, C, is chosen as follow

Equation 16

$$C > 5 \cdot C_{INT}$$

and R is calculated to provide the desired triangular ripple voltage:

Equation 17

$$R = \frac{L}{R_{VESR} \cdot C}$$

Finally, the R1 resistor can be selected according to expression 18:

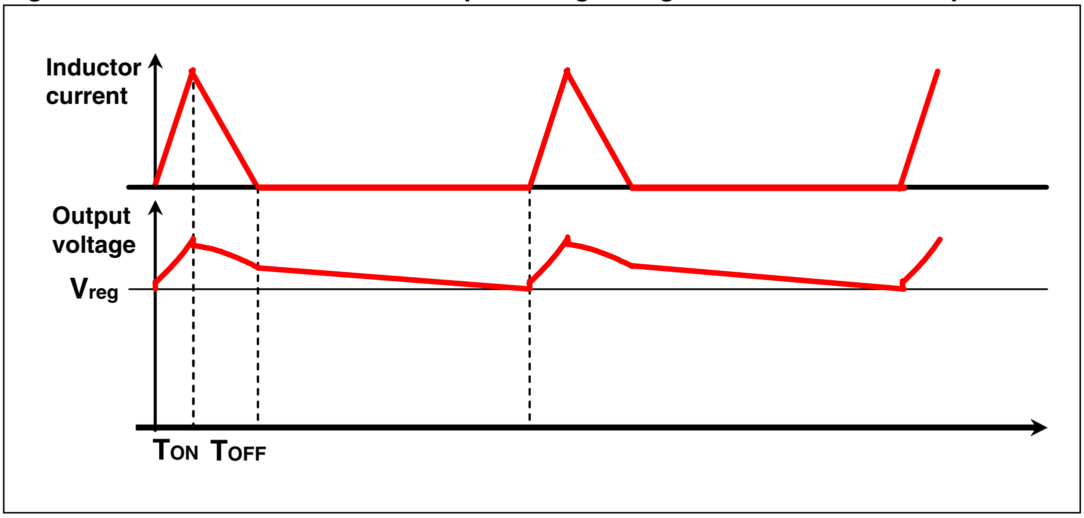
Equation 18

$$R1 = \frac{R \cdot \left(\frac{1}{\pi \cdot f_Z \cdot C}\right)}{R - \frac{1}{\pi \cdot f_Z \cdot C}}$$

7.1.3 Pulse-skip and no-audible pulse-skip modes

High efficiency at light load conditions is achieved by PM6675AS entering the Pulse-Skip Mode (if enabled). At light load conditions the zero-crossing comparator truncates the low-side switch On-Time as soon as the inductor current becomes negative; in this way the comparator determines the On-Time duration instead of the output ripple (see *Figure 27*).

Figure 27. Inductor current and output voltage at light load with Pulse-Skip



As a consequence, the output capacitor is left floating and its discharge depends solely on the current drained from the load. When the output ripple on the pin COMP falls under the reference, a new shot is triggered and the next cycle begins. The Pulse-Skip mode is naturally obtained enabling the zero-crossing comparator and automatically takes part in the COT algorithm when the inductor current is about half the ripple current amount, i.e. migrating from continuous conduction mode (C.C.M.) to discontinuous conduction mode (D.C.M.).

The output current threshold related to the transition between PWM Mode and Pulse-Skip Mode can be approximately calculated as:

Equation 19

$$I_{LOAD}(PWM2Skip) = \frac{V_{IN} - V_{OUT}}{2 \cdot L} \cdot T_{ON}$$

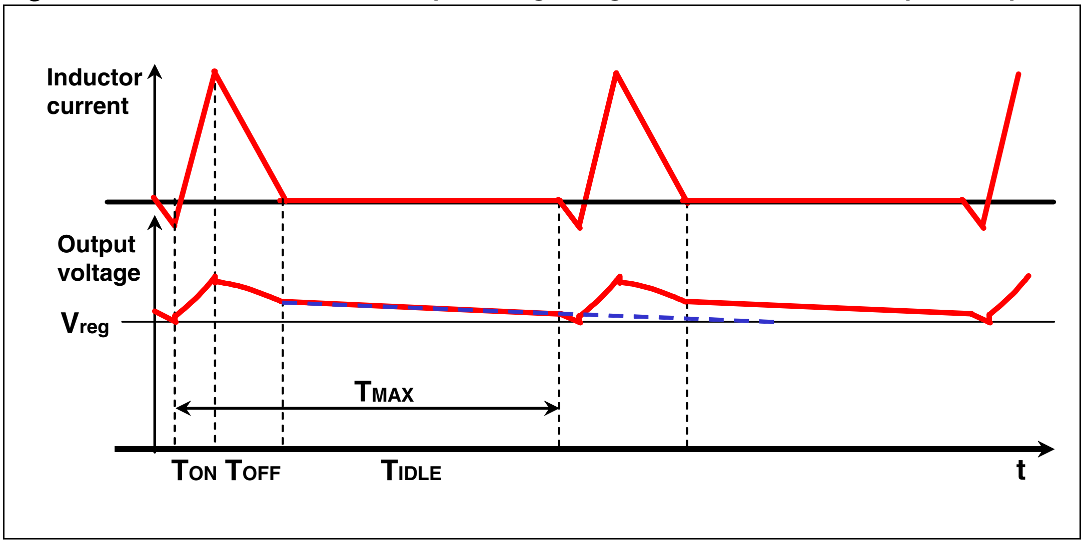
At higher loads, the inductor current never crosses the zero and the device works in pure PWM mode with a switching frequency around the nominal value.

A physiological consequence of Pulse-Skip Mode is a more noisy and asynchronous (than normal conditions) output, mainly due to very low load. If the Pulse-Skip is not compatible with the application, the PM6675AS allows the user to choose also between forced-PWM and No-Audible Pulse-Skip alternative modes (see *Chapter 7.1.4* for details).

No-audible pulse-skip mode

Some audio-noise sensitive applications cannot accept the switching frequency to enter the audible range as is possible in Pulse-Skip mode with very light loads. For this reason, the PM6675AS implements an additional feature to maintain a minimum switching frequency of 33 kHz despite of a slight efficiency loss. At very light load conditions, if any switching cycle has taken place within 30 µs (typ.) since the last one (because of the output voltage is still higher than the reference), a No-audible pulse-skip cycle begins. The low-side MOSFET is turned on and the output is driven to fall until the reference has been crossed. Then, the high-side switch is turned on for a Ton period and, once it has expired, the synchronous rectifier is enabled until the inductor current reaches the zero-crossing threshold (see *Figure 28*).

Figure 28. Inductor current and output voltage at light load with non-audible pulse-skip



For frequencies higher than 33 kHz (due to heavier loads) the device works in the same way as in Pulse-Skip mode. It is important to notice that in both pulse-skip and no-audible Pulse-Skip modes the switching frequency changes not only with the load but also with the input voltage.