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PM6675S

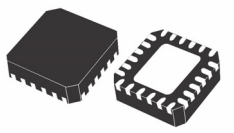
High efficiency step-down controller with embedded 2 A LDO regulator

Features

- Switching section
  - 4.5 V to 28 V input voltage range
  - 0.6 V, ±1 % voltage reference
  - Selectable 1.5 V fixed output voltage
  - Adjustable 0.6 V to 3.3 V output voltage
  - 1.237 V ±1 % reference voltage available
  - Very fast load transient response using constant on-time control loop
  - No R_{SENSE} current sensing using low side MOSFETs' $R_{DS(ON)}$
  - Negative current limit
  - Latched OVP and UVP
  - Soft-start internally fixed at 3 ms
  - Selectable pulse skipping at light load
  - Selectable No-Audible (33 kHz) pulse skip mode
  - Ceramic output capacitors supported
  - Output voltage ripple compensation
  - Output soft-end
- LDO regulator section
  - Adjustable 0.6 V to 3.3 V output voltage
  - Selectable ±1 Apk or ±2 Apk current limit
  - Dedicated power-good signal
  - Ceramic output capacitors supported
  - Output soft-end

Applications

- Notebook computers
- Graphic cards
- Embedded computers



VFQFPN-24 4x4

Description

The PM6675S device consists of a single high efficiency step-down controller and an independent Low Drop-Out (LDO) linear regulator.

The Constant On-Time (COT) architecture assures fast transient response supporting both electrolytic and ceramic output capacitors. An embedded integrator control loop compensates the DC voltage error due to the output ripple.

A selectable low-consumption mode allows the highest efficiency over a wide range of load conditions. The low-noise mode sets the minimum switching frequency to 33 kHz for audio-sensitive applications.

The LDO linear regulator can sink and source up to 2 Apk. Two fixed current limits (±1 A-±2 A) can be chosen.

An active soft-end is independently performed on both the switching and the linear regulators outputs when disabled.

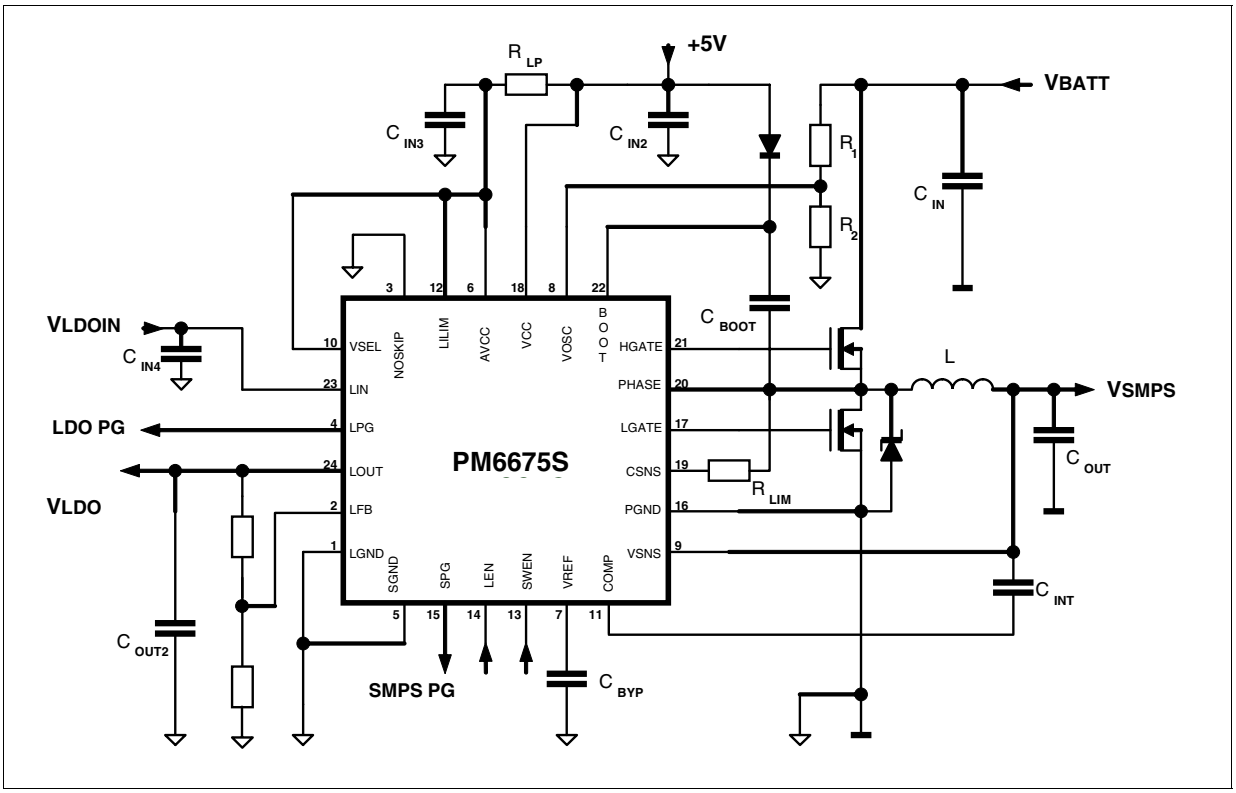
Table 1. Device summary

Order codes	Package	Packaging
PM6675S	VFQFPN-24 4x4 (exposed pad)	Tube
PM6675STR		Tape and reel

Contents

1 Typical application circuit

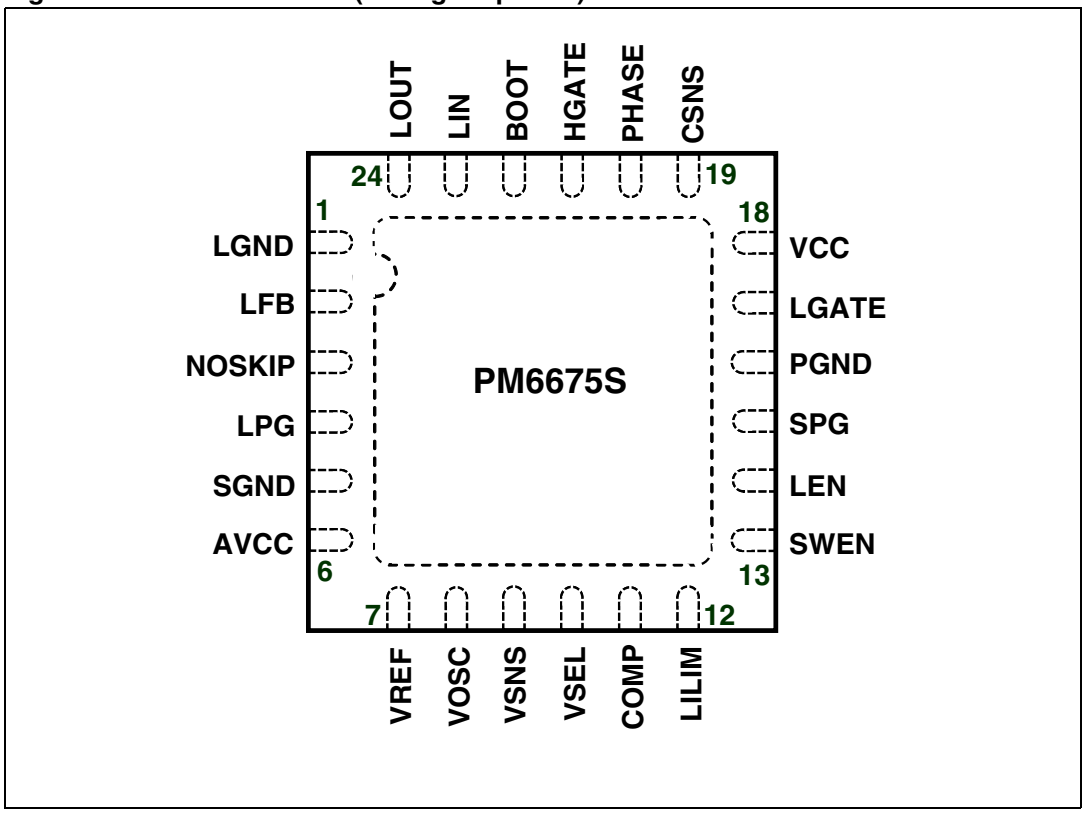
Figure 1. Application circuit



2 Pin settings

2.1 Connections

Figure 2. Pin connection (through top view)



2.2 Pin description

Table 2. Pin functions

N°	Pin	Function
1	LGND	LDO power ground. Connect to the negative terminal of VTT output capacitor.
2	LFB	LDO remote sensing. Connect as close as possible to the load via a low noise PCB trace.
3	NOSKIP	Pulse-Skip/No-Audible Pulse-Skip Modes selector. See *Section 7.1.4: Mode-of-operation selection on page 30*
4	LPG	LDO section power-good signal (open drain output). High when LDO output voltage is within ±10 % of nominal value.
5	SGND	Ground reference for analog circuitry, control logic and VTTREF buffer. Connect together with the thermal pad and VTTGND to a low impedance ground plane. See the *Application Note* for details.
6	AVCC	+5 V supply for internal logic. Connect to +5 V rail through a simple RC filtering network.
7	VREF	High accuracy output voltage reference (1.237 V) for multilevel pins setting. It can deliver up to 50 µA. Connect a 100 nF capacitor between VREF and SGND in order to enhance noise rejection.
8	VOSC	Frequency selection. Connect to the central tap of a resistor divider to set the desired switching frequency. The pin cannot be left floating. See *Section 7: Device description on page 19* for details.
9	VSNS	Switching section output remote sensing and discharge path during output soft-end. Connect as close as possible to the load via a low noise PCB trace.
10	VSEL	Fixed output selector and feedback input for the switching controller. If VSEL pin voltage is higher than 4 V, the fixed 1.5 V output is selected. If VSEL pin voltage is lower than 4 V, it is used as negative input of the error amplifier. See *Section 7.1.4: Mode-of-operation selection on page 30* for details.
11	COMP	DC voltage error compensation input pin for the switching section. Refer to *Section 7.1.4: Mode-of-operation selection on page 30* for more details.
12	LILIM	Current limit selector for the LDO. Connect to SGND for ±1 A current limit or to +5 V for ±2 A current limit.
13	SWEN	Switching controller enable. When tied to ground, the switching output is turned off and a soft-end is performed.
14	LEN	Linear regulator enable. When tied to ground, the LDO output is turned off and a soft-end is performed.
15	SPG	Switching section power good signal (open drain output). High when the switching regulator output voltage is within ±10 % of nominal value.
16	PGND	Power ground for the switching section.
17	LGATE	Low-side gate driver output.
18	VCC	+5 V low-side gate driver supply. Bypass with a 100 nF capacitor to PGND.

Table 2. Pin functions (continued)

N°	Pin	Function
19	CSNS	Current sense input for the switching section. This pin must be connected through a resistor to the drain of the synchronous rectifier ($R_{DS(ON)}$ sensing) to set the current limit threshold.
20	PHASE	Switch node connection and return path for the high side gate driver.
21	HGATE	High-Side Gate Driver Output
22	BOOT	Bootstrap capacitor connection. Input for the supply voltage of the high-side gate driver.
23	LIN	Linear Regulator Input. Bypass to LGND by a 10µF ceramic capacitor for noise rejection enhancement.
24	LOUT	LDO linear regulator output. Bypass with a 20µF (2 x 10 µF MLCC) filter capacitor.

3 Electrical data

3.1 Maximum rating

Table 3. Absolute maximum ratings (1)

Symbol	Parameter	Value	Unit
V_{AVCC}	AVCC to SGND	-0.3 to 6	V
V_{VCC}	VCC to SGND	-0.3 to 6	
	PGND, LGND to SGND	-0.3 to 0.3	
	HGATE and BOOT to PHASE	-0.3 to 6	
	HGATE and BOOT to PGND	-0.3 to 44	
V_{PHASE}	PHASE to SGND	-0.3 to 38	
	LGATE to PGND	-0.3 to V_{CC} +0.3	
	CSNS, SPG, LEN, SWEN, LILIM, COMP, VSEL, VSNS, VOSC, VREF, NOSKIP to SGND	-0.3 to V_{AVCC} + 0.3	
	LPG,VREF, LOUT, LFB to SGND	-0.3 to V_{AVCC} + 0.3	
	LIN, LOUT, LPG, LIN to LGND	-0.3 to V_{AVCC} + 0.3	
	Maximum withstanding Voltage range test condition: CDF-AEC-Q100-002- “Human Body Model” acceptance criteria: “Normal Performance”	± 1250	V

1. Free air operating conditions unless otherwise specified. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	42	°C/W
T_{STG}	Storage temperature range	- 50 to 150	°C
T_A	Operating ambient temperature range	- 40 to 85	°C
T_J	Junction operating temperature range	- 40 to 125	°C

3.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Values			Unit
		Min	Typ	Max	
V_{IN}	Input voltage range	4.5		28	V
V_{AVCC}	IC supply voltage	4.5		5.5	
V_{VCC}	IC supply voltage	4.5		5.5	

4 Electrical characteristics

Table 6. Electrical characteristics

T_A = 0 °C to 85 °C, VCC = AVCC = +5 V, LIN = 1.5 V and LOUT = 0.6 V, if not otherwise specified (1)

Symbol	Parameter	Test condition		Values			Unit
				Min	Typ	Max	
Supply section							
I_{IN}	Operating current (Switching + LDO)	SWEN, LEN, VSEL and NOSKIP connected to AVCC, No load on LOUT output.				2	mA
I_{SW}	Operating current (Switching)	SWEN, VSEL and NOSKIP connected to AVCC, LEN connected to SGND.				1	
I_{SHDN}	Shutdown operating current	SWEN and LEN tied to SGND.				10	µA
UVLO	AVCC under voltage lockout upper threshold			4.1	4.25	4.4	V
	AVCC under voltage lockout upper threshold			3.85	4.0	4.1	
	UVLO hysteresis			70			mV
ON-time (SMPS)							
t_{ON}	On-time duration	VSEL low, NOSKIP low, V_{VSNS} = 2V	VOSC=300 mV	530	630	730	ns
			VOSC=500 mV	320	380	440	
OFF-time (SMPS)							
t_{OFFMIN}	Minimum OFF-time				300	350	ns
Voltage reference							
	Voltage accuracy	4.5 V< V_{IN} < 25 V		1.224	1.237	1.249	V
	Load regulation	-50 µA< I_{VREF} < 50 µA		-4		4	mV
	Undervoltage Lockout Fault Threshold				800		

Table 6. Electrical characteristics (continued)
T_A = 0 °C to 85 °C, VCC = AVCC = +5 V, LIN = 1.5 V and LOUT = 0.6 V, if not otherwise specified (1)

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
SMPS output						
V_{OUT}	SMPS fixed output voltage	VSEL connected to AVCC, NOSKIP tied to SGND, No Load		1.5		V
	Feedback output voltage accuracy		-1.5		1.5	%
Current limit and zero crossing comparator						
I_{CSNS}	CSNS input bias current		90	100	110	µA
	Comparator offset		-6		6	mV
	Positive current limit threshold	V_{PGND} - V_{CSNS}		100		
	Fixed negative current limit threshold			110		
$V_{ZC,OFFS}$	Zero crossing comparator offset		-11	-5	1	
High and low side gate drivers						
	HGATE driver on-resistance	HGATE high state (pull-up)		2.0	3	Ω
		HGATE low state (pull-down)		1.8	2.7	
	LGATE driver on-resistance	LGATE high state (pull-up)		1.4	2.1	
		LGATE low state (pull-down)		0.6	0.9	
UVP/OVP protections and PGOOD signals						
OVP	Over voltage threshold		112	115	118	%
UVP	Under voltage threshold		67	70	73	
PGOOD	SMPS upper threshold		107	110	113	
	SMPS lower threshold		86	90	93	
	LDO upper threshold		107	110	113	
	LDO lower threshold		86	90	93	
$I_{PG,LEAK}$	SPG and LPG Leakage Current	SPG and LPG forced to 5.5 V			1	µA
$V_{PG,LOW}$	SPG and LPG Low Level Voltage	$I_{LPG,SINK}$ = $I_{SPG,SINK}$ = 4 mA		150	250	mV
Soft-start section (SMPS)						
	Soft-start ramp time (4 steps current limit)		2	3	4	ms
	Soft-start current limit step			25		µA

Table 6. Electrical characteristics (continued)
T_A = 0 °C to 85 °C, VCC = AVCC = +5 V, LIN = 1.5 V and LOUT = 0.6 V, if not otherwise specified (1)

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
Soft-end section						
	Switching section discharge resistance		15	25	35	Ω
	LDO section discharge resistance		15	25	35	
LDO section						
V_{LREF}	LDO reference voltage			600		mV
	LDO output accuracy respect to VREF	-1 mA < I_{LDO} < 1 mA	-20		20	
		-1 A < I_{LDO} < 1 A	-25		25	
$I_{LDO,CL}$	LDO sink current limit	V_{LFB} > V_{LREF} , LILIM = 5 V	-3	-2.3	-2	A
		V_{LFB} > V_{LREF}, LILIM = 0 V	-1.6	-1.3	-1	
	LDO source current limit	0.9 • V_{LREF} < V_{LFB} < V_{LREF}, LILIM = 5V	2	2.4	3	
		0.9 • V_{LREF} < V_{LFB} < V_{LREF}, LILIM = 0V	1	1.3	1.6	
		V_{LFB} < 0.9 • V_{LREF}, LILIM = 5 V	1	1.3	1.6	
		V_{LFB} < 0.9 • V_{LREF}, LILIM = 0 V	0.5	0.8	1.1	
$I_{LIN,BIAS}$	LDO input bias current, ON	LEN connected to AVCC, no load		1	10	µA
	LDO input bias current, OFF	LEN = 0 V, no load			1	
$I_{LFB,BIAS}$	LFB input bias current	LEN connected to AVCC V_{LFB} = 0.6 V	-1		1	
$I_{LFB,LEAK}$	LFB leakage current	LEN = 0 V, V_{LFB} = 0.6 V	-1		1	

Table 6. Electrical characteristics (continued)

T_A = 0 °C to 85 °C, VCC = AVCC = +5 V, LIN = 1.5 V and LOUT = 0.6 V, if not otherwise specified (1)

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
Power management section						
$V_{VTHVSEL}$	VSEL pin thresholds	Fixed mode	V_{AVCC} -0.7			V
		Adjustable mode			V_{AVCC} -1.3	
$V_{VTHNOSKIP}$	NOSKIP pin thresholds	Forced-PWM mode	V_{AVCC} -0.8			
		No-audible mode	1.0		V_{AVCC} -1.5	
		Pulse-skip mode			0.5	
V_{VTHLEN}, $V_{VTHSWEN}$	LEN, SWEN turn off level		0.4			
	LEN, SWEN turn on level				1.6	
$V_{VTHLILIM}$	LILIM pin thresholds	±2 A LDO current limit	V_{AVCC} -0.8			
		±1 A LDO current limit			0.5	
$I_{IN,LEAK}$	Logic input leakage current	LEN, SWEN and LILIM = 5 V			10	µA
$I_{IN3,LEAK}$	Multilevel input leakage current	VSEL and NOSKIP = 5 V			10	
$I_{OSC,LEAK}$	VOSC pin leakage current	VOSC = 1 V			1	
Thermal shutdown						
T_{SHDN}	Shutdown temperature (2)			150		°C

1. $T_A = T_J$. All parameters at operating temperature extremes are guaranteed by design and statistical analysis (not production tested)
2. Guaranteed by design. Not production tested.

5 Typical operating characteristics

Figure 3. VOUT efficiency vs load, 1.5 V, SW frequency = 400 kHz

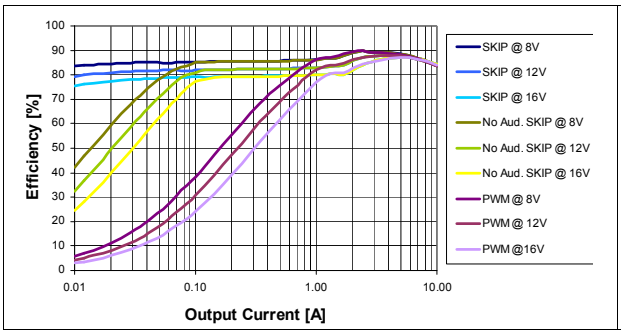


Figure 4. VOUT efficiency vs load, 1.25 V, SW frequency = 400 kHz

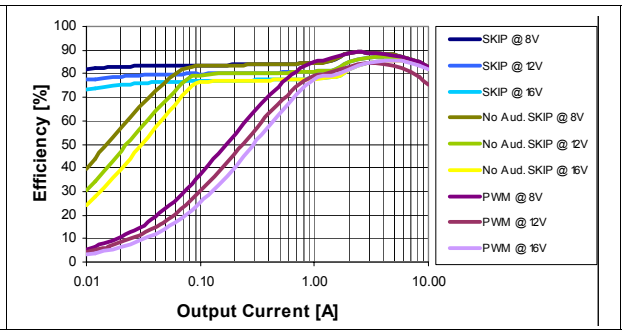


Figure 5. VOUT load regulation, 1.5 V, Vin = 12 V

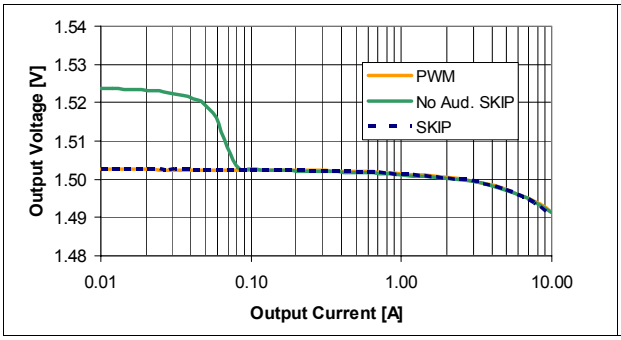


Figure 6. VOUT load regulation, 1.25 V, Vin = 12 V

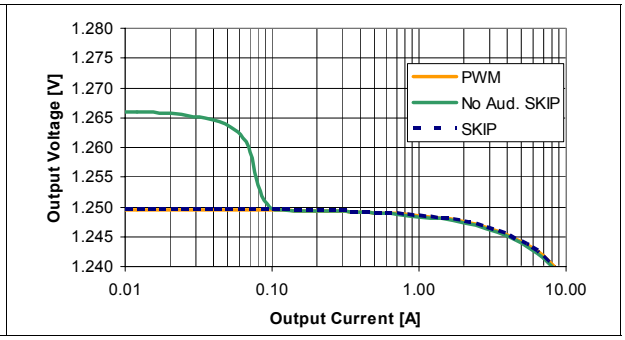


Figure 7. VOUT load regulation, 2.5 V, Vin = 12 V

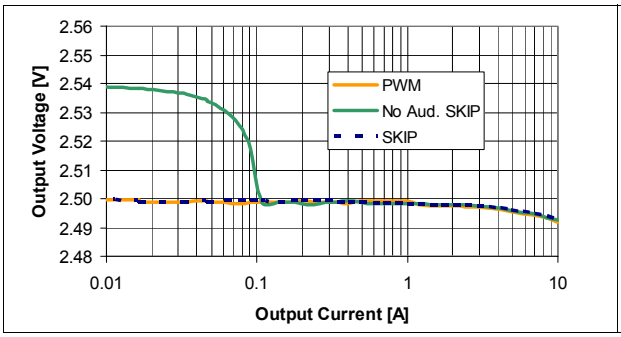


Figure 8. LOUT load regulation, LOUT = 0.9 V, LIN = 1.5 V

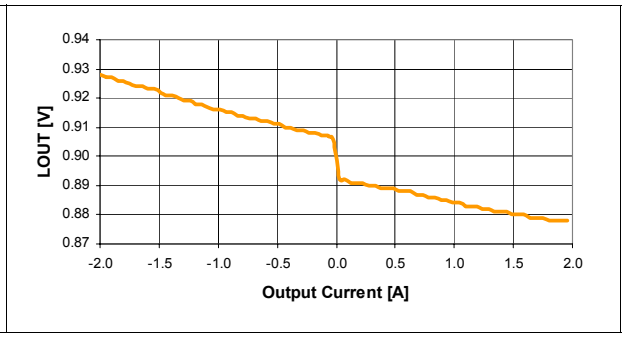


Figure 9. VOUT line regulation, 1.5 V, 0 A

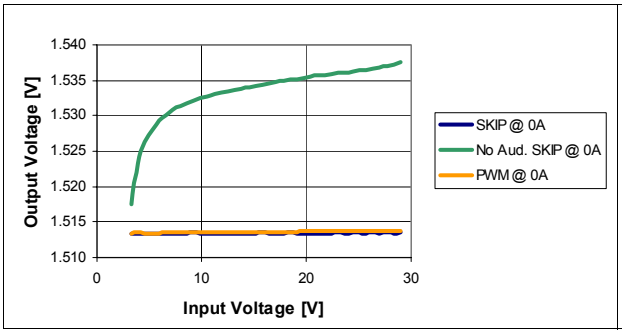


Figure 10. VOUT line regulation, 1.25 V, 0 A

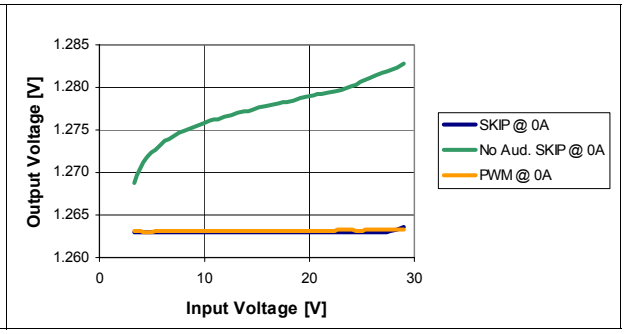


Figure 11. VOUT line regulation, 1.5 V

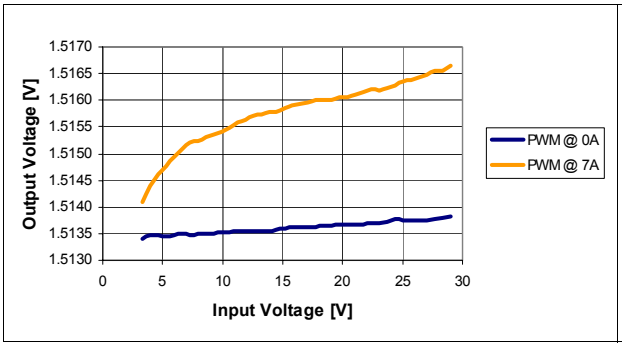


Figure 12. VOUT line regulation, 1.25 V

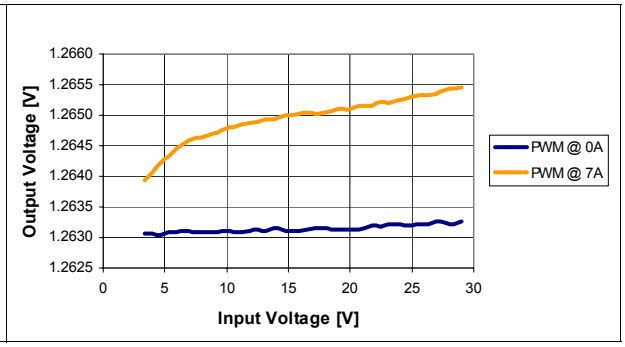


Figure 13. Switching frequency vs input voltage, 1.5 V

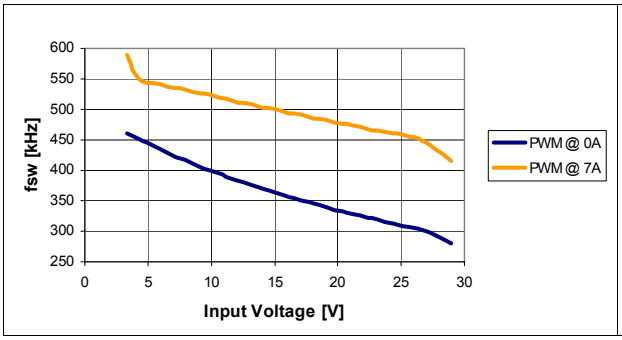


Figure 14. Switching frequency vs input voltage, 1.25 V

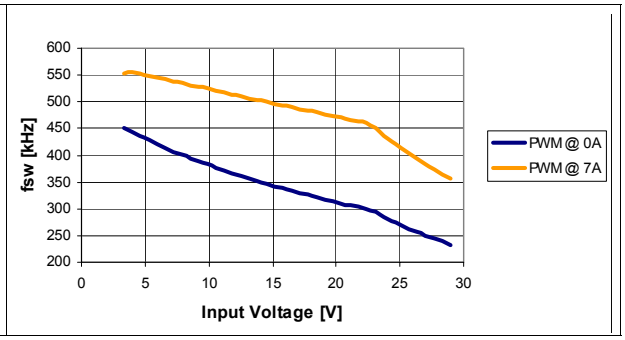


Figure 15. Switching frequency vs load - 1.5 V

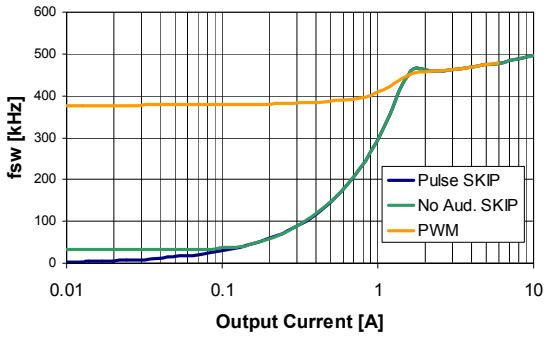


Figure 16. PWM waveforms

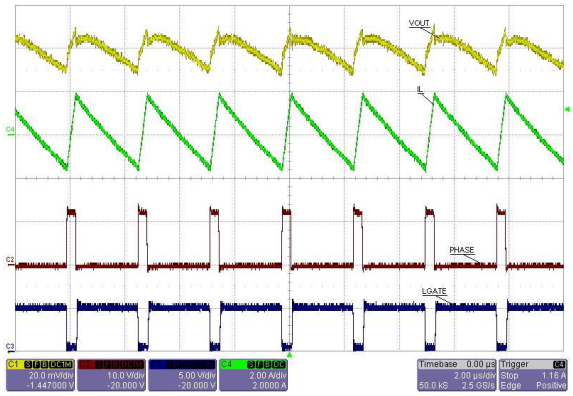


Figure 17. No-audible pulse-skip waveforms

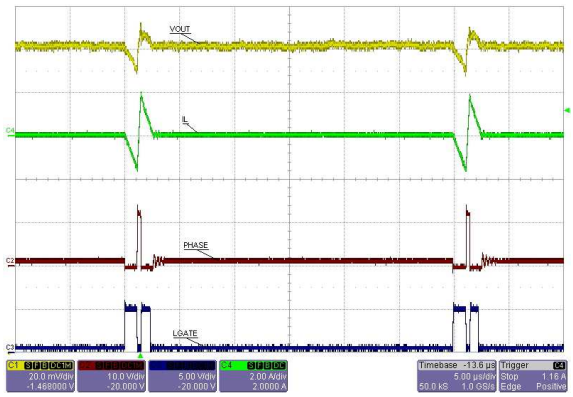


Figure 18. Pulse-skip waveforms

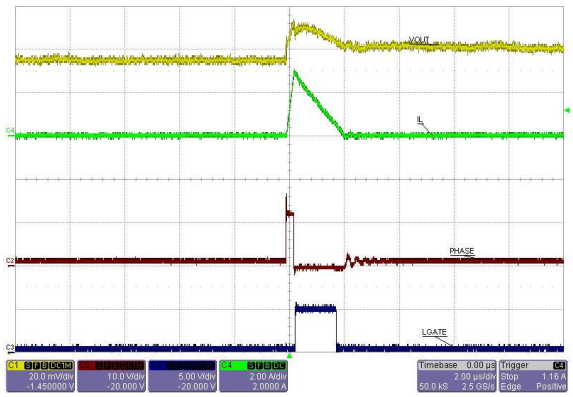


Figure 19. Power-up sequence VCC above UVLO

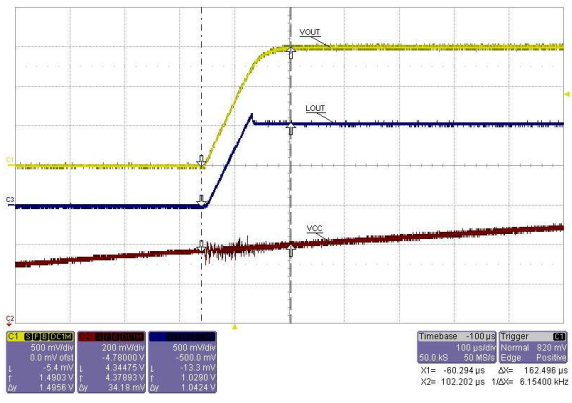


Figure 20. VOUT soft-start, 1.5 V, heavy load

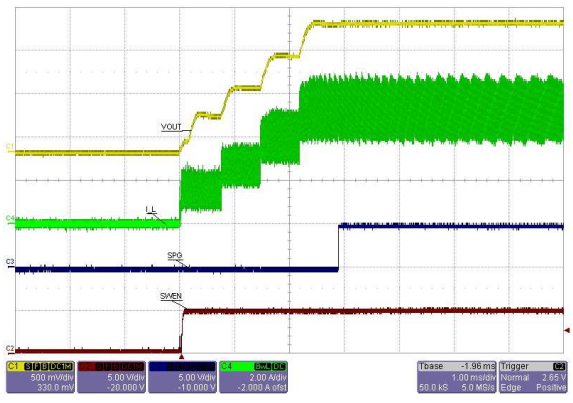


Figure 21. Switching section output soft-end

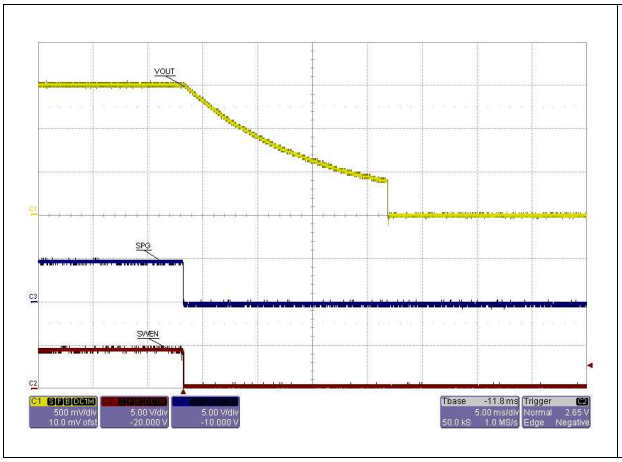


Figure 22. LDO section output soft-end

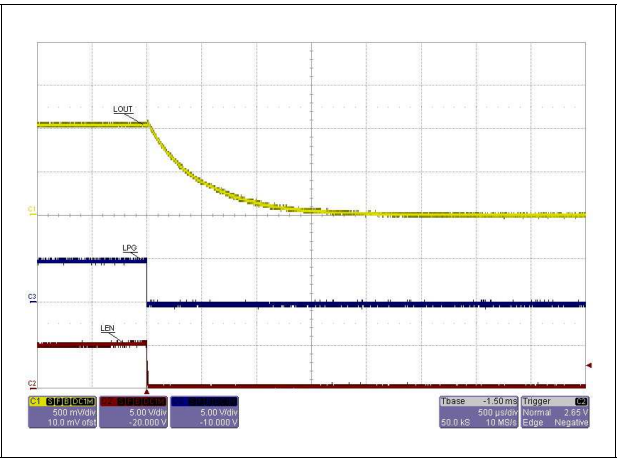


Figure 23. -1.8 A to 1.8 A LOUT load transient, 0.9 V

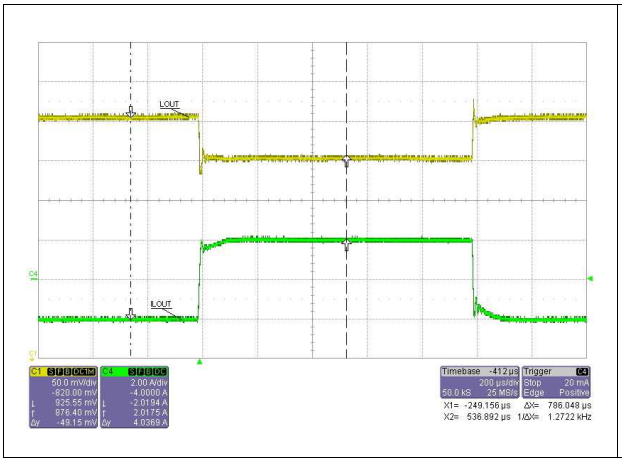


Figure 24. -1 A to 1 A LOUT load transient, 0.9 V

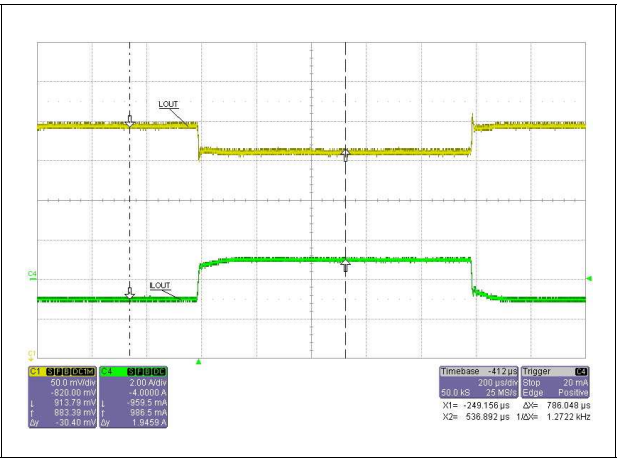


Figure 25. 0 A to 8 A VOUT load transient, PWM

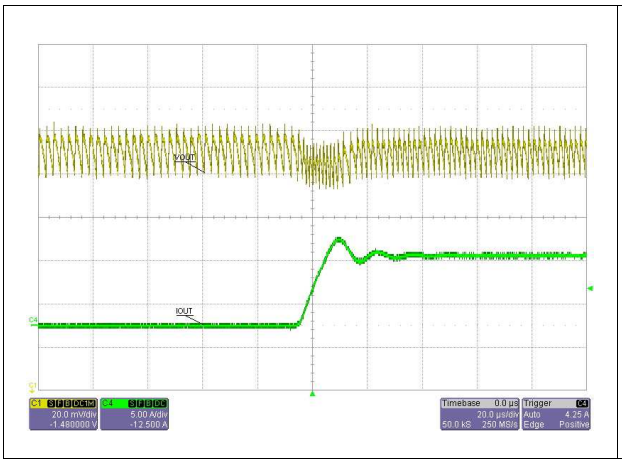


Figure 26. 8 A to 0 A VOUT load transient, PWM

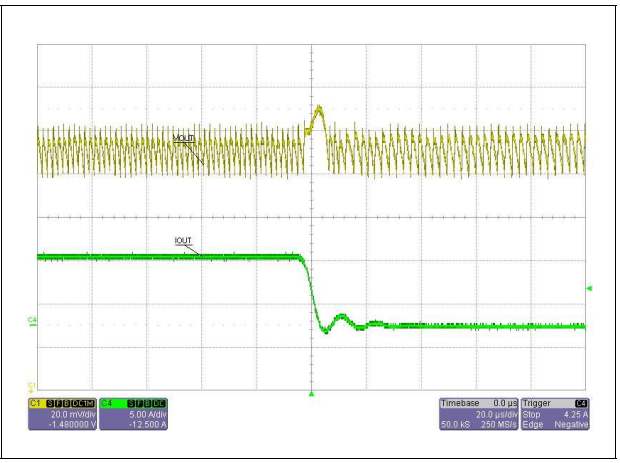


Figure 27. 0 A to 5 A VOUT load transient, Pulse-Skip

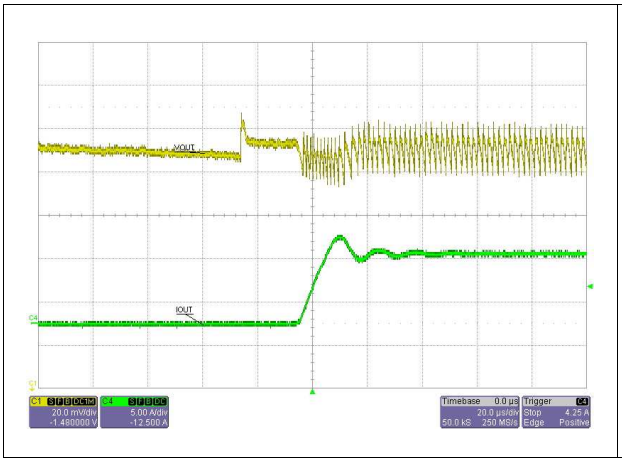


Figure 28. 5 A to 0 A VOUT load transient, Pulse-Skip

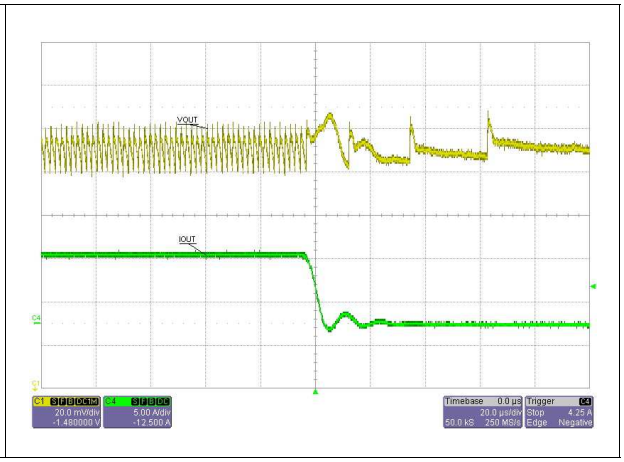


Figure 29. Over-voltage protection, VOUT = 1.5 V

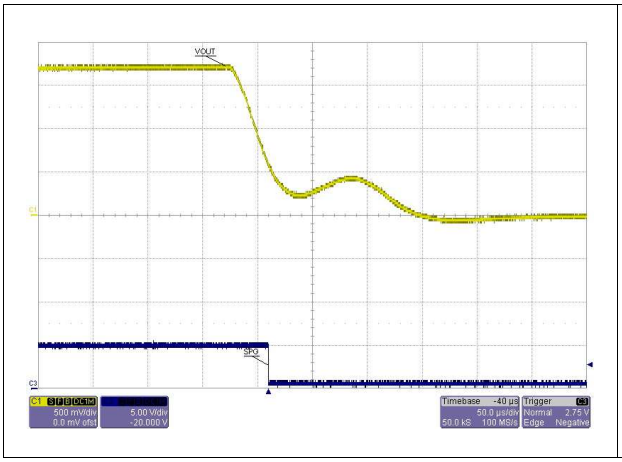
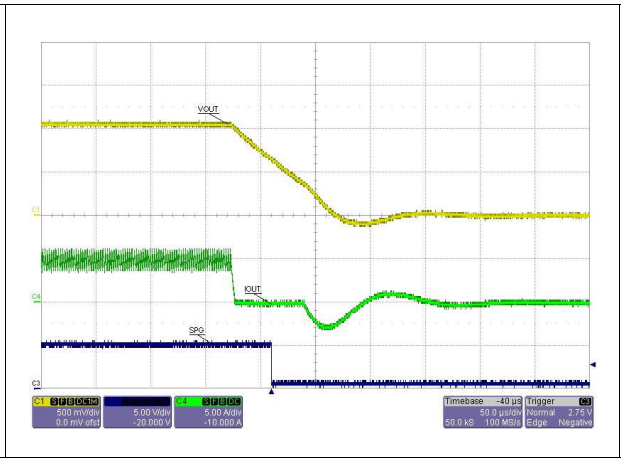


Figure 30. Under-voltage protection, VOUT = 1.5 V



6 Block diagram

Figure 31. Functional and block diagram

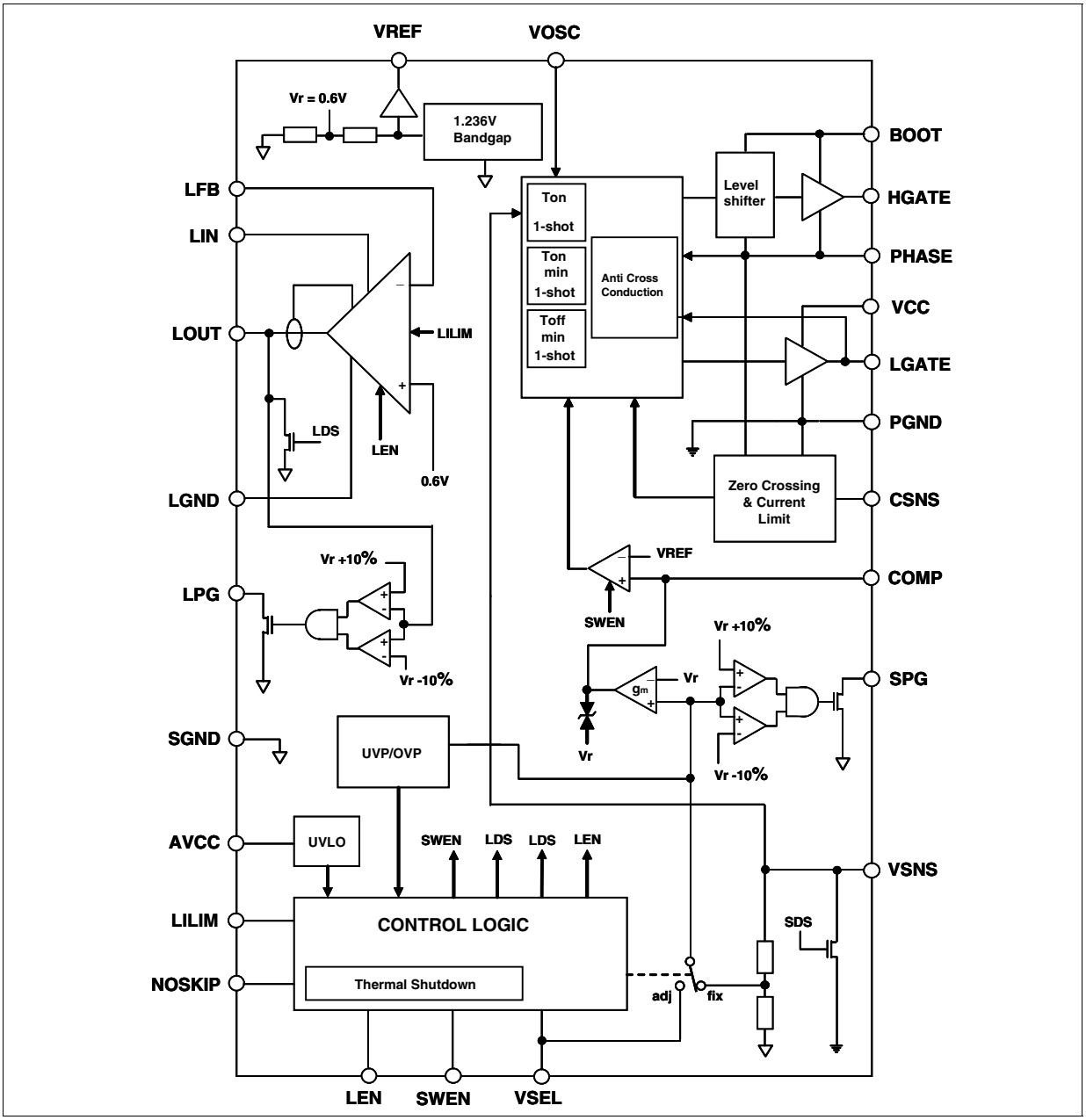


Table 7. Legend

SWEN	Switching controller enable
LEN	LDO regulator enable
LDS	LDO output discharge enable
SDS	Switching output discharge enable
LILIM	LDO regulator current limit

7 Device description

The PM6675S combines a single high efficiency step-down controller and an independent Low Drop-Out (LDO) linear regulator in the same package.

The switching controller section is a high-performance, pseudo-fixed frequency, Constant-On-Time (COT) based regulator specifically designed for handling fast load transient over a wide range of input voltages.

The switching section output can be easily set to a fixed 1.5 V voltage without additional components or adjusted in the 0.6 V to 3.3 V range using an external resistor divider. The Switching Mode Power Supply (SMPS) can handle different modes of operation in order to minimize noise or power consumption, depending on the application needs. Selectable low-consumption and low-noise modes allow the highest efficiency and a 33 kHz minimum switching frequency respectively at light loads.

A lossless current sensing scheme, based on the Low-Side MOSFET turn-on resistance, avoids the need for an external sensing resistor.

The input of the LDO can be either the switching section output or a lower voltage rail in order to reduce the total power dissipation. Linear regulator stability is achieved by filtering its output with a ceramic capacitor (20 µF or greater). The LDO linear regulator can sink and source up to 2 Apk.
Two fixed current limit (±1 A-±2 A) can be chosen.

An active soft-end is independently performed on both the switching and the linear regulators outputs when disabled.

7.1 Switching section - constant on-time PWM controller

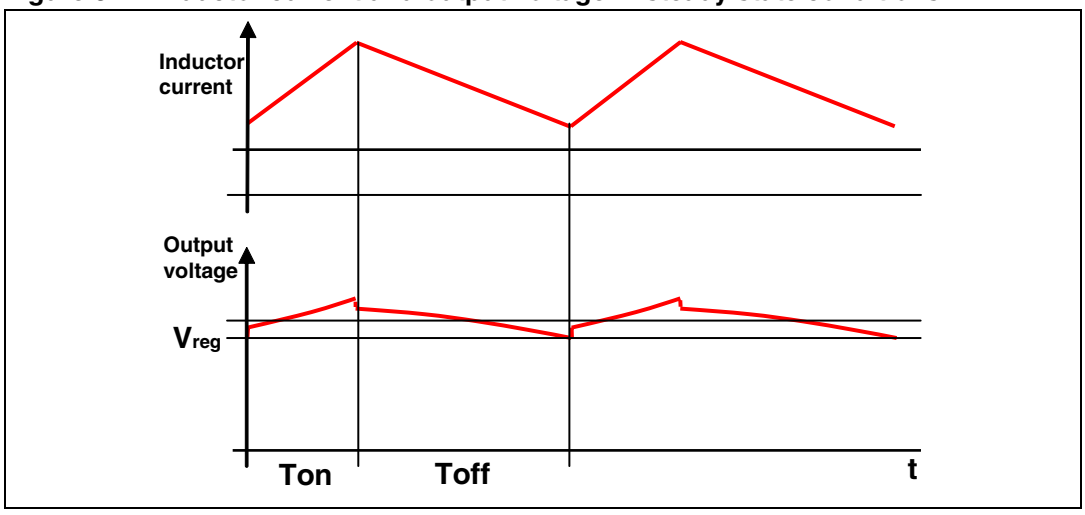
The PM6675S employes a pseudo-fixed frequency, Constant On-Time (COT) controller as the core of the switching section. It is well known that the COT controller uses a relatively simple algorithm and uses the ripple voltage derived across the output capacitor ESR to trigger the On-Time one-shot generator. In this way, the output capacitor ESR acts as a current sense resistor providing the appropriate ramp signal to the PWM comparator. Nearly constant switching frequency is achieved by the system loop in steady-state operating conditions by varying the On-Time duration, avoiding thus the need for a clock generator. The On-Time one shot duration is directly proportional to the output voltage, detected by theVSNS pin, and inversely proportional to the input voltage, detected by the the VOSC pin, as follows:

Equation 1

$$T_{ON} = K_{OSC} \frac{V_{SNS}}{V_{OSC}} + \tau$$

where K_{OSC} is a constant value (130 ns typ.) and τ is the internal propagation delay (40ns typ.). The one-shot generator directly drives the high-side MOSFET at the beginning of each switching cycle allowing the inductor current to increase; after the On-Time has expired, an Off-Time phase, in which the low-side MOSFET is turned on, follows. The Off-Time duration is solely determined by the output voltage: when lower than the set value (i.e. the voltage at VSNS pin is lower than the internal reference V_R = 0.6 V), the synchronous rectifier is turned off and a new cycle begins (*Figure 32*).

Figure 32. Inductor current and output voltage in steady state conditions



The duty-cycle of the buck converter is, in steady-state conditions, given by

Equation 2

$$D = \frac{V_{OUT}}{V_{IN}}$$

The switching frequency is thus calculated as

Equation 3

$$f_{SW} = \frac{D}{T_{ON}} = \frac{\frac{V_{OUT}}{V_{IN}}}{K_{OSC}\frac{V_{SNS}}{V_{OSC}}} = \frac{\alpha_{OSC}}{\alpha_{OUT}} \cdot \frac{1}{K_{OSC}}$$

where

Equation 4a

$$\alpha_{OSC} = \frac{V_{OSC}}{V_{IN}}$$

Equation 4b

$$\alpha_{OUT} = \frac{V_{SNS}}{V_{OUT}}$$

Referring to the typical application schematic (figures on cover page and *Figure 33*), the final expression is then:

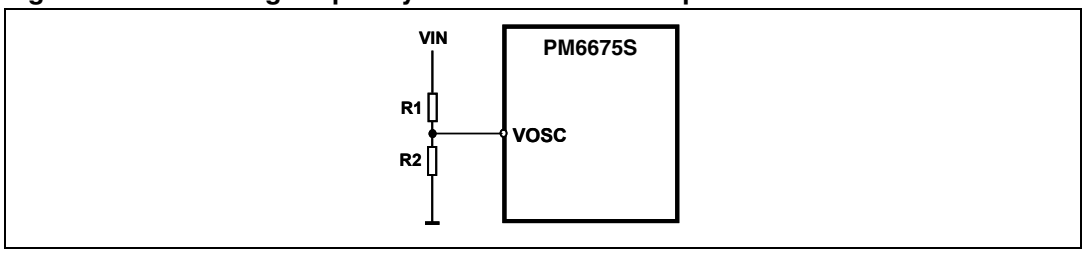
Equation 5

$$f_{SW} = \frac{\alpha_{OSC}}{K_{OSC}} = \frac{R_2}{R_1 + R_2} \cdot \frac{1}{K_{OSC}}$$

Even if the switching frequency is theoretically independent from battery and output voltages, parasitic parameters involved in the power path (like MOSFET on-resistance and inductor DCR) introduce voltage drops responsible for a slight dependence on load current. In addition, the internal delay is due to a small dependence on input voltage.

The PM6675S switching frequency can be set by an external divider connected to the VOSC pin.

Figure 33. Switching frequency selection and VOSC pin



The voltage seen at this pin must be greater than 0.8 V and lower than 2 V in order to ensure the system linearity.

7.1.1 Constant-On-Time architecture

Figure 34 shows the simplified block diagram of the Constant-On-Time controller.

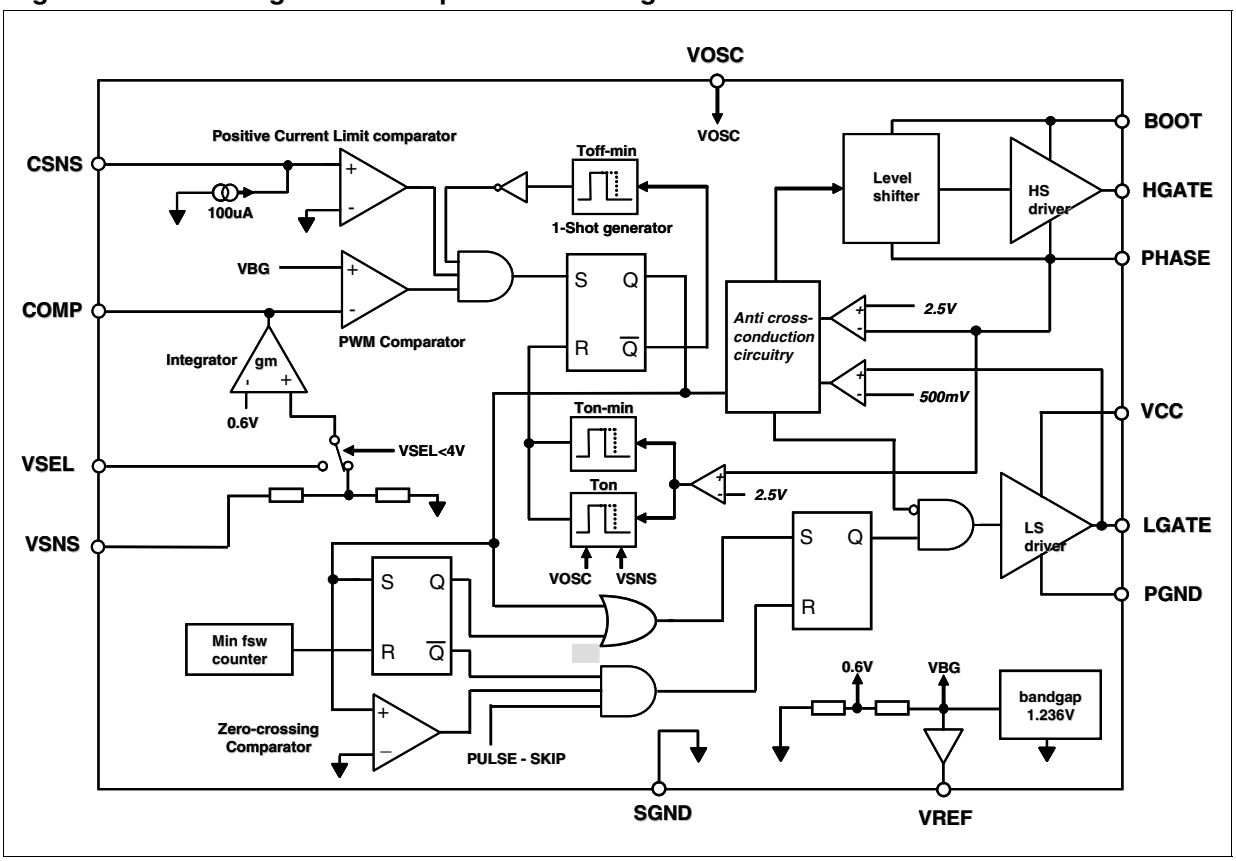
The switching regulator of the PM6675S controls a one-shot generator that turns on the high-side MOSFET when the following conditions are simultaneously satisfied: the PWM comparator is high (i.e. output voltage is lower than Vr = 0.6 V), the synchronous rectifier current is below the current limit threshold and the minimum off-time has expired.

A minimum Off-Time contraint (300ns typ.) is introduced to assure the boot capacitor charge and allow inductor valley current sensing on low-side MOSFET. A minimum On-Time is also introduced to assure the start-up switching sequence.

Once the On-Time has timed out, the high side switch is turned off, while the synchronous rectifier is ignited according to the anti-cross conduction management circuitry.

When the output voltage reaches the valley limit (determined by internal reference Vr = 0.6 V), the low-side MOSFET is turned off according to the anti-cross conduction logic once again, and a new cycle begins.

Figure 34. Switching section simplified block diagram

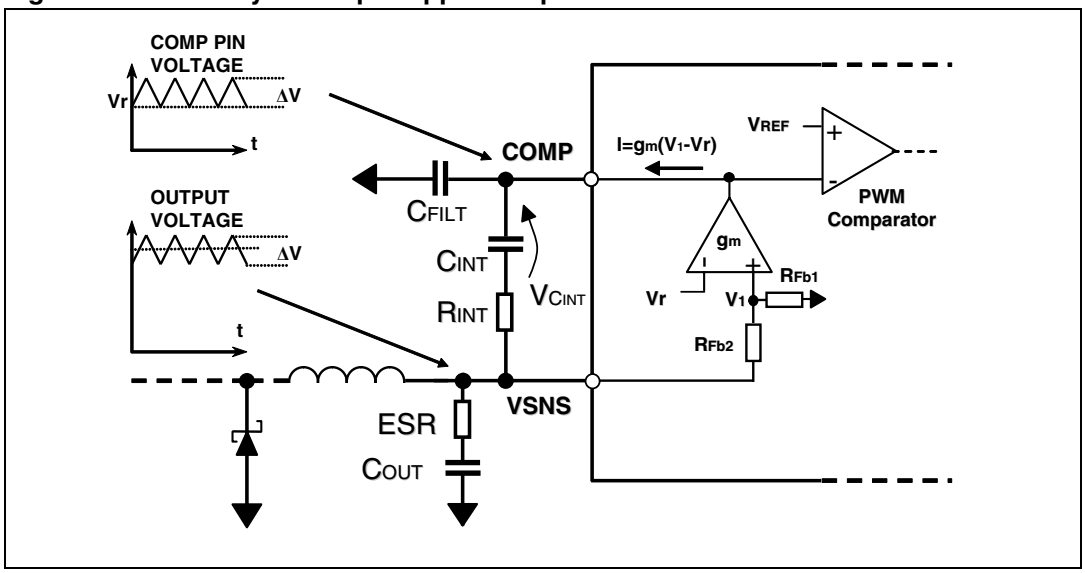


7.1.2 Output ripple compensation and loop stability

The loop is closed connecting the center tap of the output divider (internally, when the fixed output voltage is chosen, or externally, using the VSEL pin in the adjustable output voltage mode). The feedback node is the negative input of the error comparator, while the positive input is internally connected to the reference voltage (Vr = 0.6 V). When the feedback voltage becomes lower than the reference voltage, the PWM comparator goes to high and sets the control logic, turning on the high-side MOSFET. After the On-Time (calculated as previously described), the system releases the high-side MOSFET and turns on the synchronous rectifier.

The voltage drop along ground and supply PCB paths, used to connect the output capacitor to the load, is a source of DC error. Furthermore the system regulates the output voltage valley, not the average, as shown in *Figure 37*. Thus, the voltage ripple on the output capacitor is an additional source of DC error. To compensate this error, an integrative network is introduced in the control loop, by connecting the output voltage to the COMP pin through a capacitor (C_{INT}) as shown in *Figure 35*.

Figure 35. Circuitry for output ripple compensation



The additional capacitor is used to reduce the voltage on the COMP pin when higher than 300 mVpp and is unnecessary for most of applications. The trans conductance amplifier (gm) generates a current, proportional to the DC error, used to charge the C_{INT} capacitor. The voltage across the C_{INT} capacitor feeds the negative input of the PWM comparator, forcing the loop to compensate the total static error. An internal voltage clamp forces the COMP pin voltage range to ±150 mV respect to V_{REF}. This is useful to avoid or smooth output voltage overshoot during a load transient. When the Pulse-Skip Mode is entered, the clamping range is automatically reduced to 60 mV in order to enhance the recovering capability. If the ripple amplitude is larger than 150 mV, an additional capacitor C_{FILT} can be connected between the COMP pin and ground to reduce ripple amplitude, otherwise the integrator will operate out of its linearity range. This capacitor is unnecessary for most of applications and can be omitted.

The design of the external feedback network depends on the output voltage ripple. If the ripple is higher than approximately 20 mV, the correct C_{INT} capacitor is usually enough to keep the loop stable. The stability of the system depends firstly on the output capacitor zero frequency.

The following condition must be satisfied:

Equation 6

$$f_{SW} > k \cdot f_{Zout} = \frac{k}{2\pi \cdot C_{out} \cdot ESR}$$

where k is a fixed design parameter (k > 3). It determinates the minimum integrator capacitor value:

Equation 7

$$C_{INT} > \frac{g_m}{2\pi \cdot \left(\frac{f_{SW}}{k} - f_{Zout}\right)} \cdot \frac{Vr}{Vout}$$

where gm = 50 µs is the integrator trans conductance.

If the ripple on the COMP pin is greater than 150 mV, the auxiliary capacitor C_{FILT} can be added. If q is the desired attenuation factor of the output ripple, C_{FILT} is given by:

Equation 8

$$C_{FILT} = \frac{C_{INT} \cdot (1-q)}{q}$$

In order to reduce the noise on the COMP pin, it is possible to add a resistor R_{INT} that, together with CINT and C_{FILT}, becomes a low pass filter. The cutoff frequency f_{CUT} must be much greater (10 or more times) than the switching frequency:

Equation 9

$$R_{INT} = \frac{1}{2\pi \cdot f_{CUT} \cdot \frac{C_{INT} \cdot C_{FILT}}{C_{INT} + C_{FILT}}}$$

If the ripple is very small (lower than approximately 20mV), a different compensation network, called "Virtual-ESR" Network, is needed. This additional circuit generates a triangular ripple that is added to the output voltage ripple at the input of the integrator. The complete control scheme is shown in *Figure 36*.