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PM6675

High efficiency step-down controller with embedded 2A LDO regulator

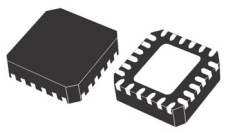
Preliminary Data

Features switching

- Switching section
  - 4.5V to 28V input voltage range
  - 0.6V, ±1% voltage reference
  - Selectable 1.5V fixed output voltage
  - Adjustable 0.6V to 3.3V output voltage
  - 1.237V ±1% reference voltage available
  - Very fast load transient response using constant on-time control loop
  - No R_{SENSE} current sensing using low side MOSFETs' $R_{DS(ON)}$
  - Negative current limit
  - Latched OVP and UVP
  - Soft start internally fixed at 3ms
  - Selectable pulse skipping at light load
  - Selectable No-Audible (33KHz) pulse skip mode
  - Ceramic output capacitors supported
  - Output voltage ripple compensation
  - Output soft-end
- LDO regulator section
  - Adjustable 0.6V to 3.3V output voltage
  - Selectable ±1Apk or ±2Apk current limit
  - Dedicated Power-Good signal
  - Ceramic output capacitors supported
  - Output soft-end

Applications

- Notebook computers
- Graphic cards
- Embedded computers



VFQFPN-24 4x4

Description

The PM6675 device consists of a single high efficiency step-down controller and an independent Low Drop-Out (LDO) linear regulator.

The Constant On-Time (COT) architecture assures fast transient response supporting both electrolytic and ceramic output capacitors. An embedded integrator control loop compensates the DC voltage error due to the output ripple.

A selectable low-consumption mode allows the highest efficiency over a wide range of load conditions. The low-noise mode sets the minimum switching frequency to 33kHz for audio-sensitive applications.

The LDO linear regulator can sink and source up to 2Apk. Two fixed current limits (±1A-±2A) can be chosen.

An active Soft-End is independently performed on both the switching and the linear regulators outputs when disabled.

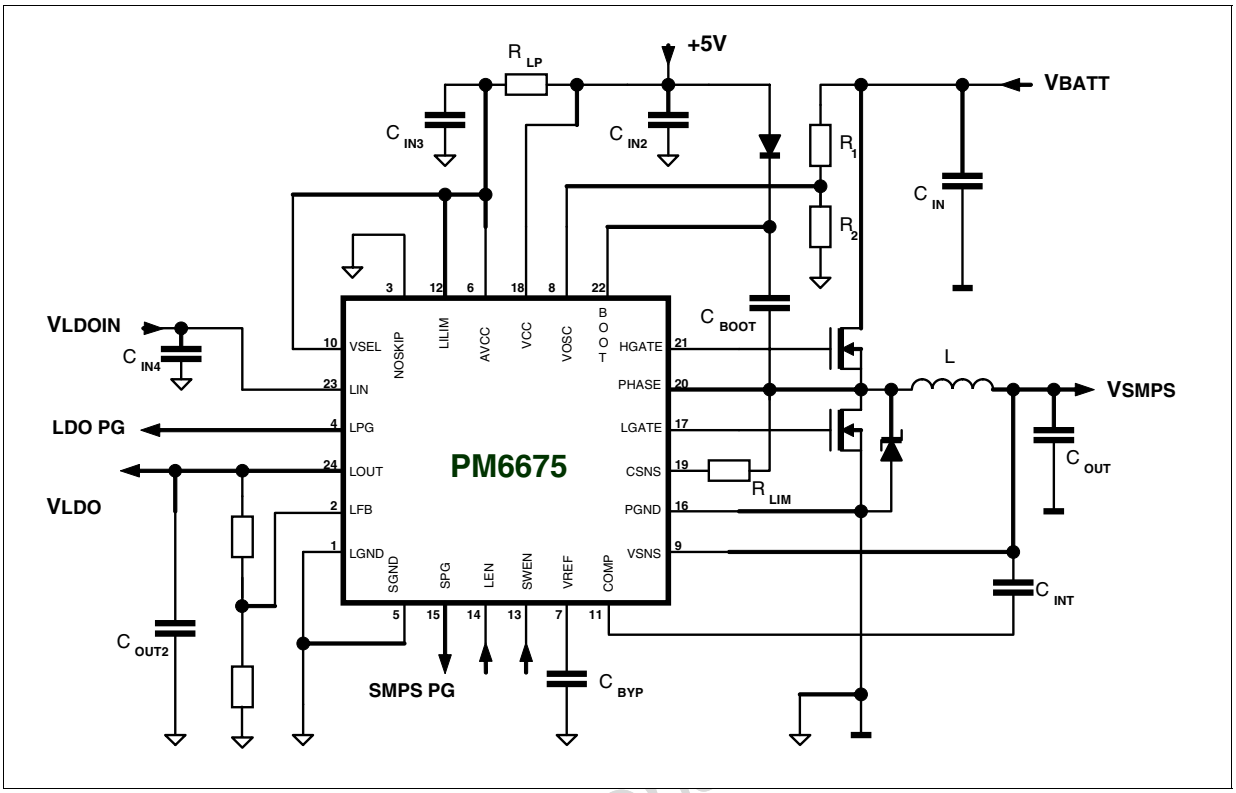
Order codes

Part number	Package	Packaging
PM6675	VFQFPN-24 4x4 (Exposed Pad)	Tube

Contents

1 Typical application circuit

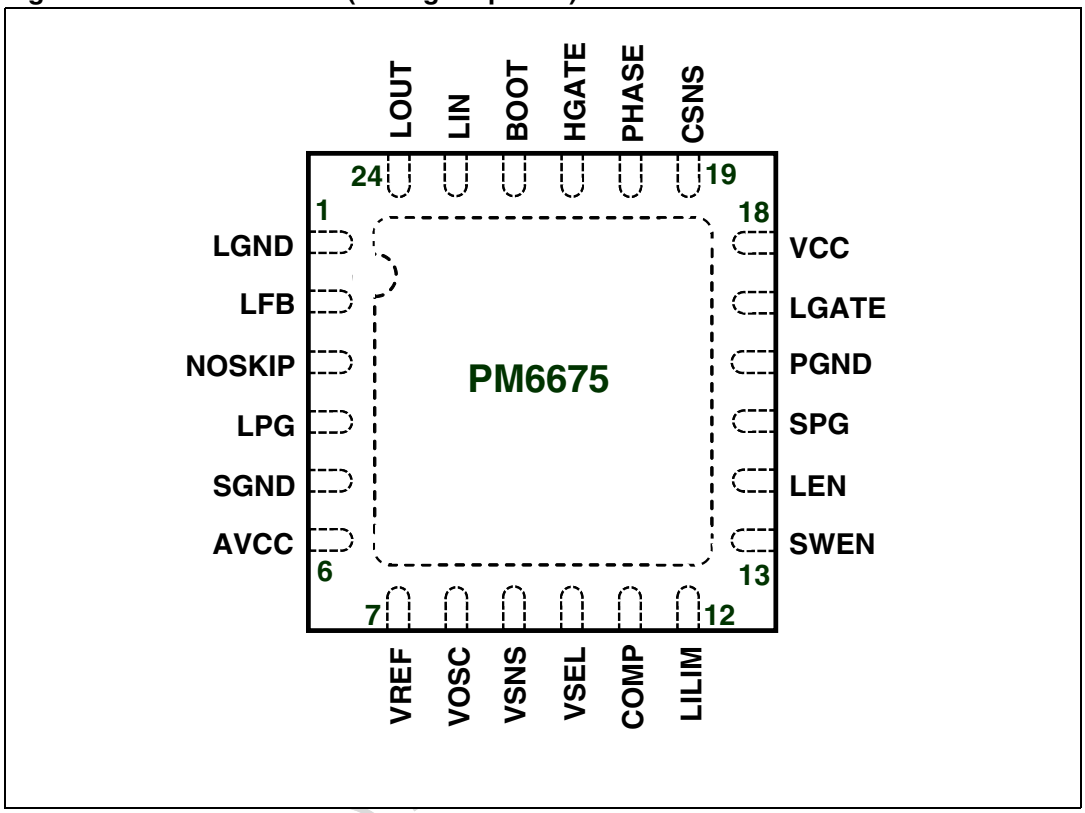
Figure 1. Application circuit



2 Pin settings

2.1 Connections

Figure 2. Pin connection (through top view)



2.2 Pin description

Table 1. Pin functions

N°	Pin	Function
1	LGND	LDO power ground. Connect to the negative terminal of VTT output capacitor.
2	LFB	LDO remote sensing. Connect as close as possible to the load via a low noise PCB trace.
3	NOSKIP	Pulse-Skip/No-Audible Pulse-Skip Modes selector. See *Section 6.1.4: Mode-of-operation selection on page 24*
4	LPG	LDO section Power-Good signal (open drain output). High when LDO output voltage is within ±10% of nominal value.
5	SGND	Ground Reference for analog circuitry, control logic and VTTREF buffer. Connect together with the thermal pad and VTTGND to a low impedance ground plane. See the *Application Note* for details.
6	AVCC	+5V supply for internal logic. Connect to +5V rail through a simple RC filtering network.
7	VREF	High accuracy output voltage reference (1.237V) for multilevel pins setting. It can deliver up to 50µA. Connect a 100nF capacitor between VREF and SGND in order to enhance noise rejection.
8	VOSC	Frequency Selection. Connect to the central tap of a resistor divider to set the desired switching frequency. The pin cannot be left floating. See *Section 6: Device description on page 14* for details.
9	VSNS	Switching section output remote sensing and discharge path during output Soft-End. Connect as close as possible to the load via a low noise PCB trace.
10	VSEL	Fixed output selector and feedback input for the switching controller. If VSEL pin voltage is higher than 4V, the fixed 1.5V output is selected. If VSEL pin voltage is lower than 4V, it is used as negative input of the error amplifier. See *Section 6.1.4: Mode-of-operation selection on page 24* for details.
11	COMP	DC voltage error compensation input pin for the switching section. Refer to *Section 6.1.4: Mode-of-operation selection on page 24* for more details.
12	LILIM	Current limit selector for the LDO. Connect to SGND for ±1A current limit or to +5V for ±2A current limit.
13	SWEN	Switching Controller Enable. When tied to ground, the switching output is turned off and a Soft-End is performed.
14	LEN	Linear Regulator Enable. When tied to ground, the LDO output is turned off and a Soft-End is performed.
15	SPG	Switching Section Power-Good signal (open drain output). High when the switching regulator output voltage is within ±10% of nominal value.
16	PGND	Power ground for the switching section.
17	LGATE	Low-side gate driver output.
18	VCC	+5V low-side gate driver supply. Bypass with a 100nF capacitor to PGND.

Table 1. Pin functions (continued)

N°	Pin	Function
19	CSNS	Current sense input for the switching section. This pin must be connected through a resistor to the drain of the synchronous rectifier ($R_{DS(ON)}$ sensing) to set the current limit threshold.
20	PHASE	Switch node connection and return path for the high side gate driver.
21	HGATE	High-Side Gate Driver Output
22	BOOT	Bootstrap capacitor connection. Input for the supply voltage of the high-side gate driver.
23	LIN	Linear Regulator Input. Bypass to LGND by a 10µF ceramic capacitor for noise rejection enhancement.
24	LOUT	LDO linear regulator output. Bypass with a 20ìF (2 x 10µF MLCC) filter capacitor.

3 Electrical data

3.1 Maximum rating

Table 2. Absolute maximum ratings (1)

Symbol	Parameter	Value	Unit
V_{AVCC}	AVCC to SGND	-0.3 to 6	V
V_{VCC}	VCC to SGND	-0.3 to 6	
	PGND, LGND to SGND	-0.3 to 0.3	
	HGATE and BOOT to PHASE	-0.3 to 6	
	HGATE and BOOT to PGND	-0.3 to 42	
V_{PHASE}	PHASE to SGND	-0.3 to 36	
	LGATE to PGND	-0.3 to V_{CC} +0.3	
	CSNS, SPG, LEN, SWEN, LILIM, COMP, VSEL, VSNS, VOSC, VREF, NOSKIP to SGND	-0.3 to V_{AVCC} + 0.3	
	LPG,VREF, LOUT, LFB to SGND	-0.3 to V_{AVCC} + 0.3	
	LIN, LOUT, LPG, LIN to LGND	-0.3 to V_{AVCC} + 0.3	
	Maximum withstanding Voltage range test condition: CDF-AEC-Q100-002- “Human Body Model” acceptance criteria: “Normal Performance”	±1250	V

1. Free air operating conditions unless otherwise specified. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	42	°C/W
T_{STG}	Storage temperature range	-40 to 150	°C
T_A	Operating ambient temperature range	-40 to 85	°C
T_J	Junction operating temperature range	0 to 125	°C

4 Electrical characteristics

V_{IN} = 12V; T_A = 0°C to 85°C, VCC = AVCC = +5V, LIN = 1.5V and LOUT = 0.9V (if not otherwise specified)

Table 4. Electrical characteristics

Symbol	Parameter	Test condition		Values			Unit
				Min	Typ	Max	
Supply section							
V_{IN}	Input voltage range			4.5		28	V
V_{AVCC}	IC supply voltage			4.5		5.5	
V_{VCC}	IC supply voltage			4.5		5.5	
I_{IN}	Operating current (Switching + LDO)	SWEN, LEN, VSEL and NOSKIP connected to AVCC, No load on LOUT output.				2	mA
I_{SW}	Operating current (Switching)	SWEN, VSEL and NOSKIP connected to AVCC, LEN connected to SGND.				1	
I_{SHDN}	Shutdown operating current	SWEN and LEN tied to SGND.				10	µA
UVLO	AVCC under voltage lockout upper threshold			4.1	4.25	4.4	V
	AVCC under voltage lockout upper threshold			3.9	4.0	4.1	
	UVLO hysteresis			70			mV
ON-time (SMPS)							
t_{ON}	On-time duration	VSELhigh, and NOSKIP low, V_{VSNS} = 2V	VOSC=300mV	550	630	710	ns
			VOSC=500mV	330	380	430	
OFF-time (SMPS)							
t_{OFFMIN}	Minimum OFF-time				300	350	ns
Voltage reference							
	Voltage accuracy	4.5V< V_{IN} < 25V		1.224	1.237	1.249	V
	Load regulation	-50µA< I_{VREF} < 50µA		-4		4	mV
	Undervoltage Lockout Fault Threshold				800		
SMPS output							
V_{OUT}	SMPS fixed output voltage (1)	VSEL connected to AVCC, NOSKIP tied to SGND, No Load			1.5		V
	Output voltage accuracy (1)			-1.5		1.5	%

1. Guaranteed by design. Not production tested

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
Current limit and zero crossing comparator						
I_{CSNS}	CSNS input bias current		90	100	110	µA
	Comparator offset		-5		5	mV
	Positive current limit threshold	V_{PGND} - V_{CSNS}	-115	-100	-85	
	Fixed negative current limit threshold		-130	-110	-90	
$V_{ZC,OFFS}$	Zero crossing comparator offset		-10	-5	0	
High and low side gate drivers						
	HGATE driver on-resistance	HGATE high state (pull-up)		2.0	3	Ω
		HGATE low state (pull-down)		1.8	2.7	
	LGATE driver on-resistance	LGATE high state (pull-up)		1.4	2.1	
		LGATE low state (pull-down)		0.6	0.9	
UVP/OVP protections and PGOOD signals						
OVP	Over voltage threshold		112	115	118	%
UVP	Under voltage threshold		67	70	73	
PGOOD	SMPS upper threshold		107	110	113	
	SMPS lower threshold		87	90	93	
	LDO upper threshold		107	110	113	
	LDO lower threshold		87	90	93	
$I_{PG,LEAK}$	SPG and LPG Leakage Current[1]	SPG and LPG forced to 5.5V			1	µA
$V_{PG,LOW}$	SPG and LPG Low Level Voltage	$I_{LPG,SINK}$ = $I_{SPG,SINK}$ = 4mA		150	250	mV
Soft start section (SMPS)						
	Soft-start ramp time (4 steps current limit)		2	3	4	ms
	Soft-start current limit step			25		µA

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
Soft end section						
	Switching section discharge resistance		15	25	35	Ω
	LDO section discharge resistance		15	25	35	
LDO section						
V_{LREF}	LDO reference voltage		0.594	0.6	0.606	V
V_{DROP}	LDO drop-out voltage	V_{LOUT} = 0.9V, I_{LOUT} = 1A, -10% output drop		0.25		
	LDO Internal high-side MOSFET $R_{DS(ON)}$	I_{LOUT} = 1A, AVCC=5V		0.2	0.23	Ω
$I_{LDO,CL}$	LDO sink current limit	$V_{LFB} > V_{LREF}$, LILIM = 5V	-2	-2.3	-2.8	A
		$V_{LFB} > V_{LREF}$, LILIM = 0V	-1	-1.15	-1.4	
	LDO source current limit	$0.9 \bullet V_{LREF} < V_{LFB} < V_{LREF}$, LILIM = 5V	2.8	2.3	2	
		$0.9 \bullet V_{LREF} < V_{LFB} < V_{LREF}$, LILIM = 0V	1.4	1.15	1	
		$V_{LFB} < 0.9 \bullet V_{LREF}$, LILIM = 5V	1.4	1.15	1	
		$V_{LFB} < 0.9 \bullet V_{LREF}$, LILIM = 0V	0.7	0.55	0.5	
$I_{LIN,BIAS}$	LDO input bias current, ON	LEN connected to AVCC, no load		1	10	µA
	LDO input bias current, OFF	LEN = 0V, no load			1	
$I_{LFB,BIAS}$	LFB input bias current	LEN connected to AVCC V_{LFB} = 0.6V	-1		1	
$I_{LFB,LEAK}$	LFB leakage current	LEN = 0V, V_{LFB} = 0.6V	-1		1	

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
Power management section						
$V_{VTHVSEL}$	VSEL pin thresholds	Fixed mode	V_{AVCC} -0.7			V
		Adjustable mode			V_{AVCC} -1.3	
$V_{VTHNOSKIP}$	NOSKIP pin thresholds[1]	Forced-PWM mode	V_{AVCC} -0.8			
		No-audible mode	1.0		V_{AVCC} -1.5	
		Pulse-skip mode			0.5	
$V_{VTHLILIM}$	LILIM pin thresholds[1]	±2A LDO current limit	V_{AVCC} -0.8			
		±1A LDO current limit			0.5	
$I_{IN,LEAK}$	Logic input leakage current (1)	LEN, SWEN and LILIM = 5V			10	µA
$I_{IN3,LEAK}$	Multilevel input leakage current (1)	VSEL and NOSKIP = 5V			10	
$I_{OSC,LEAK}$	VOSC pin leakage current (1)	VOSC = 1V			1	
Thermal shutdown						
T_{SHDN}	Shutdown temperature[1]			150		°C

1. Guaranteed by design. Not production tested

5 Block diagram

Figure 3. Functional and block diagram

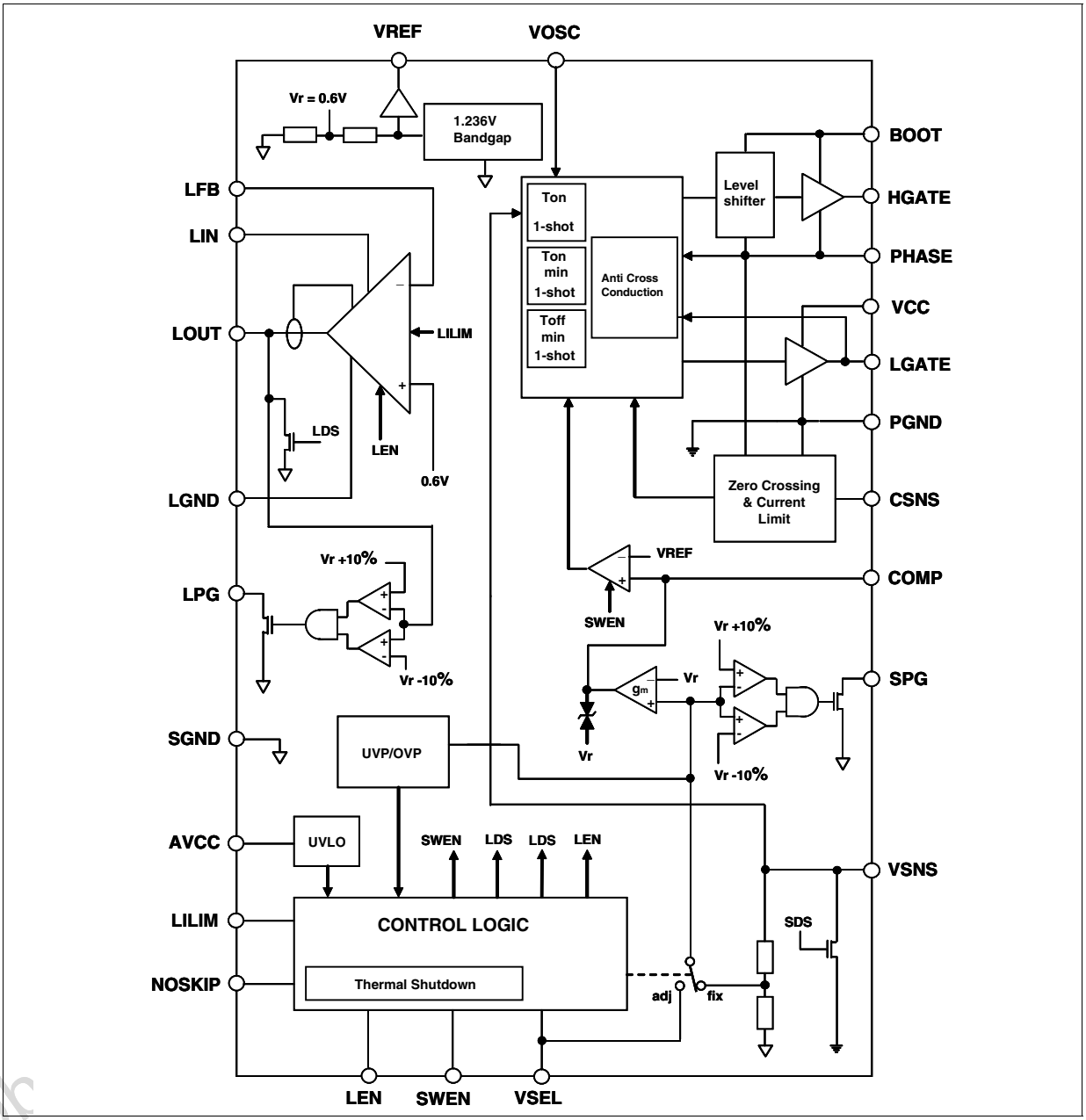


Table 5. Legend

SWEN	Switching controller enable
LEN	LDO regulator enable
LDS	LDO output discharge enable
SDS	Switching output discharge enable
LILIM	LDO regulator current limit

6 Device description

The PM6675 combines a single high efficiency step-down controller and an independent Low Drop-Out (LDO) linear regulator in the same package.

The switching controller section is a high-performance, pseudo-fixed frequency, Constant-On-Time (COT) based regulator specifically designed for handling fast load transient over a wide range of input voltages.

The switching section output can be easily set to a fixed 1.5V voltage without additional components or adjusted in the 0.6V to 3.3V range using an external resistor divider. The Switching Mode Power Supply (SMPS) can handle different modes of operation in order to minimize noise or power consumption, depending on the application needs. Selectable low-consumption and low-noise modes allow the highest efficiency and a 33kHz minimum switching frequency respectively at light loads.

A loss less current sensing scheme, based on the Low-Side MOSFET's turn-on resistance, avoids the need for an external sensing resistor.

The input of the LDO can be either the switching section output or a lower voltage rail in order to reduce the total power dissipation. Linear regulator stability is achieved by filtering its output with a ceramic capacitor (20µF or greater). The LDO linear regulator can sink and source up to 2Apk.
Two fixed current limit (±1A-±2A) can be chosen.

An active Soft-End is independently performed on both the switching and the linear regulators outputs when disabled.

6.1 Switching section - constant on-time PWM controller

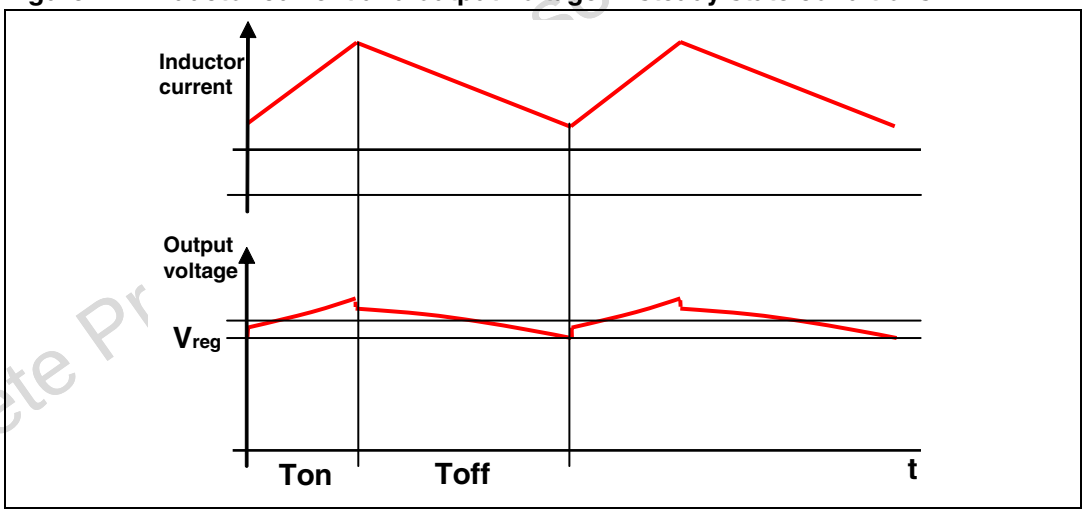
The PM6675 employees a pseudo-fixed frequency, Constant On-Time (COT) controller as the core of the switching section. It is well known that the COT controller uses a relatively simple algorithm and uses the ripple voltage derived across the output capacitor's ESR to trigger the On-Time one-shot generator. In this way, the output capacitor's ESR acts as a current sense resistor providing the appropriate ramp signal to the PWM comparator. Nearly constant switching frequency is achieved by the system's loop in steady-state operating conditions by varying the On-Time duration, avoiding thus the need for a clock generator. The On-Time one shot duration is directly proportional to the output voltage, detected by theVSNS pin, and inversely proportional to the input voltage, detected by the the VOSC pin, as follows:

Equation 1

$$T_{ON} = K_{OSC} \frac{V_{SNS}}{V_{OSC}} + \tau$$

where K_{OSC} is a constant value (130ns typ.) and τ is the internal propagation delay (40ns typ.). The one-shot generator directly drives the high-side MOSFET at the beginning of each switching cycle allowing the inductor current to increase; after the On-Time has expired, an Off-Time phase, in which the low-side MOSFET is turned on, follows. The Off-Time duration is solely determined by the output voltage: when lower than the set value (i.e. the voltage at VSNS pin is lower than the internal reference V_R = 0.6V), the synchronous rectifier is turned off and a new cycle begins (*Figure 4*).

Figure 4. Inductor current and output voltage in steady state conditions



The duty-cycle of the buck converter is, in steady-state conditions, given by

Equation 2

$$D = \frac{V_{OUT}}{V_{IN}}$$

The switching frequency is thus calculated as

Equation 3

$$f_{SW} = \frac{D}{T_{ON}} = \frac{\frac{V_{OUT}}{V_{IN}}}{K_{OSC}\frac{V_{SNS}}{V_{OSC}}} = \frac{\alpha_{OSC}}{\alpha_{OUT}} \cdot \frac{1}{K_{OSC}}$$

where

Equation 4a

$$\alpha_{OSC} = \frac{V_{OSC}}{V_{IN}}$$

Equation 4b

$$\alpha_{OUT} = \frac{V_{SNS}}{V_{OUT}}$$

Referring to the typical application schematic (figures on cover page and *Figure 5*), the final expression is then:

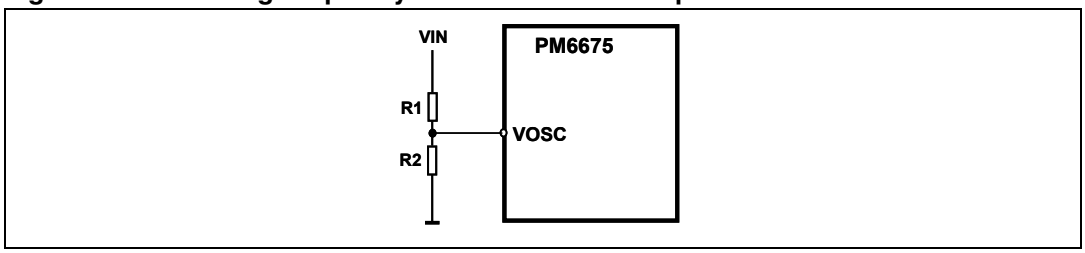
Equation 5

$$f_{SW} = \frac{\alpha_{OSC}}{K_{OSC}} = \frac{R_2}{R_1 + R_2} \cdot \frac{1}{K_{OSC}}$$

Even if the switching frequency is theoretically independent from battery and output voltages, parasitic parameters involved in the power path (like MOSFETs' on-resistance and inductor's DCR) introduce voltage drops responsible for a slight dependence on load current. In addition, the internal delay is due to a small dependence on input voltage.

The PM6675 switching frequency can be set by an external divider connected to the VOSC pin.

Figure 5. Switching frequency selection and VOSC pin



The voltage seen at this pin must be greater than 0.8V and lower than 2V in order to ensure the system's linearity.

6.1.1 Constant-On-Time architecture

Figure 6 shows the simplified block diagram of the Constant-On-Time controller.

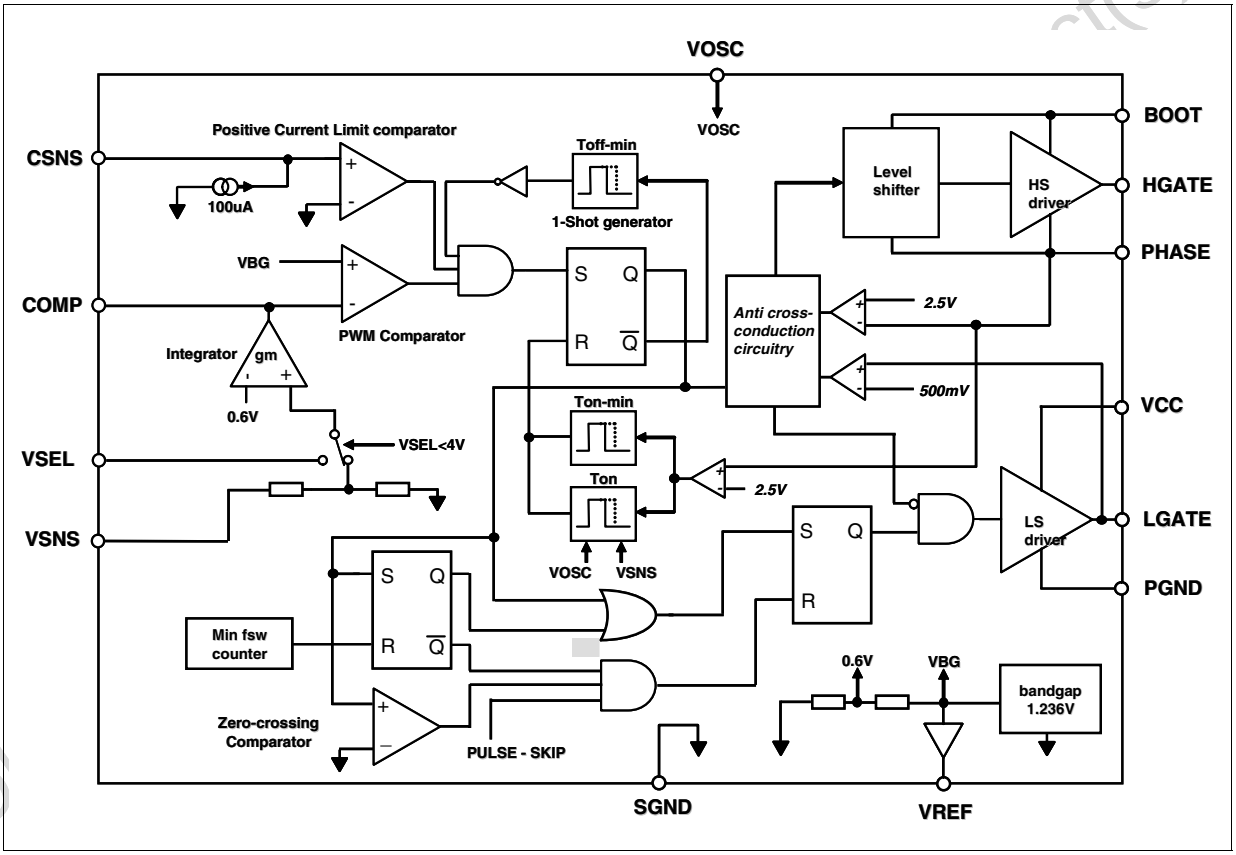
The switching regulator of the PM6675 controls a one-shot generator that initiates the high-side MOSFET when the following conditions are simultaneously satisfied: the PWM comparator is high (i.e. output voltage is lower than Vr = 0.6V), the synchronous rectifier current is below the current limit threshold and the minimum off-time has expired.

A minimum Off-Time contraint (300ns typ.) is introduced to assure the boot capacitor charge and allow inductor valley current sensing on low-side MOSFET. A minimum On-Time is also introduced to assure the start-up switching sequence.

Once the On-Time has timed out, the high side switch is turned off, while the synchronous rectifier is ignited according to the anti-cross conduction management circuitry.

When the output voltage reaches the valley limit (determined by internal reference Vr = 0.6V), the low-side MOSFET is turned off according to the anti-cross conduction logic once again, and a new cycle begins.

Figure 6. Switching section simplified block diagram

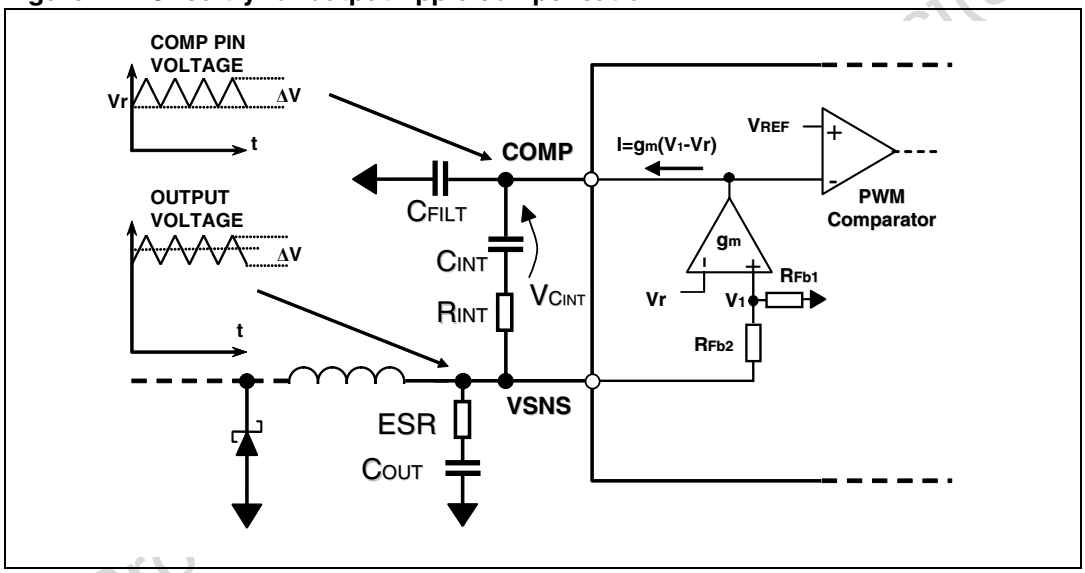


6.1.2 Output ripple compensation and loop stability

The loop is closed connecting the center tap of the output divider (internally, when the fixed output voltage is chosen, or externally, using the VSEL pin in the adjustable output voltage mode). The feedback node is the negative input of the error comparator, while the positive input is internally connected to the reference voltage (Vr = 0.6V). When the feedback voltage becomes lower than the reference voltage, the PWM comparator goes to high and sets the control logic, turning on the high-side MOSFET. After the On-Time (calculated as previously described), the system releases the high-side MOSFET and turns on the synchronous rectifier.

The voltage drop along ground and supply PCB paths, used to connect the output capacitor to the load, is a source of DC error. Furthermore the system regulates the output voltage valley, not the average, as shown in *Figure 9*. Thus, the voltage ripple on the output capacitor is an additional source of DC error. To compensate this error, an integrative network is introduced in the control loop, by connecting the output voltage to the COMP pin through a capacitor (C_{INT}) as shown in *Figure 7*.

Figure 7. Circuitry for output ripple compensation



The additional capacitor is used to reduce the voltage on the COMP pin when higher than 300mVpp and is unnecessary for most of applications. The trans conductance amplifier (gm) generates a current, proportional to the DC error, used to charge the C_{INT} capacitor. The voltage across the C_{INT} capacitor feeds the negative input of the PWM comparator, forcing the loop to compensate the total static error. An internal voltage clamp forces the COMP pin voltage range to ±150mV respect to V_{REF}. This is useful to avoid or smooth output voltage overshoot during a load transient. When the Pulse-Skip Mode is entered, the clamping range is automatically reduced to 60mV in order to enhance the recovering capability. If the ripple amplitude is larger than 150mV, an additional capacitor C_{FILT} can be connected between the COMP pin and ground to reduce ripple amplitude, otherwise the integrator will operate out of its linearity range. This capacitor is unnecessary for most of applications and can be omitted.

The design of the external feedback network depends on the output voltage ripple. If the ripple is higher than approximately 20mV, the correct C_{INT} capacitor is usually enough to keep the loop stable. The stability of the system depends firstly on the output capacitor zero frequency.

The following condition must be satisfied:

Equation 6

$$f_{SW} > k \cdot f_{Zout} = \frac{k}{2\pi \cdot C_{out} \cdot ESR}$$

where k is a fixed design parameter (k > 3). It determinates the minimum integrator capacitor value:

Equation 7

$$C_{INT} > \frac{g_m}{2\pi \cdot \left(\frac{f_{SW}}{k} - f_{Zout} \right)} \cdot \frac{Vr}{Vout}$$

where gm = 50µs is the integrator trans conductance.

If the ripple on the COMP pin is greater than the integrator 150mV, the auxiliary capacitor C_{FILT} can be added. If q is the desired attenuation factor of the output ripple, C_{FILT} is given by:

Equation 8

$$C_{FILT} = \frac{C_{INT} \cdot (1 - q)}{q}$$

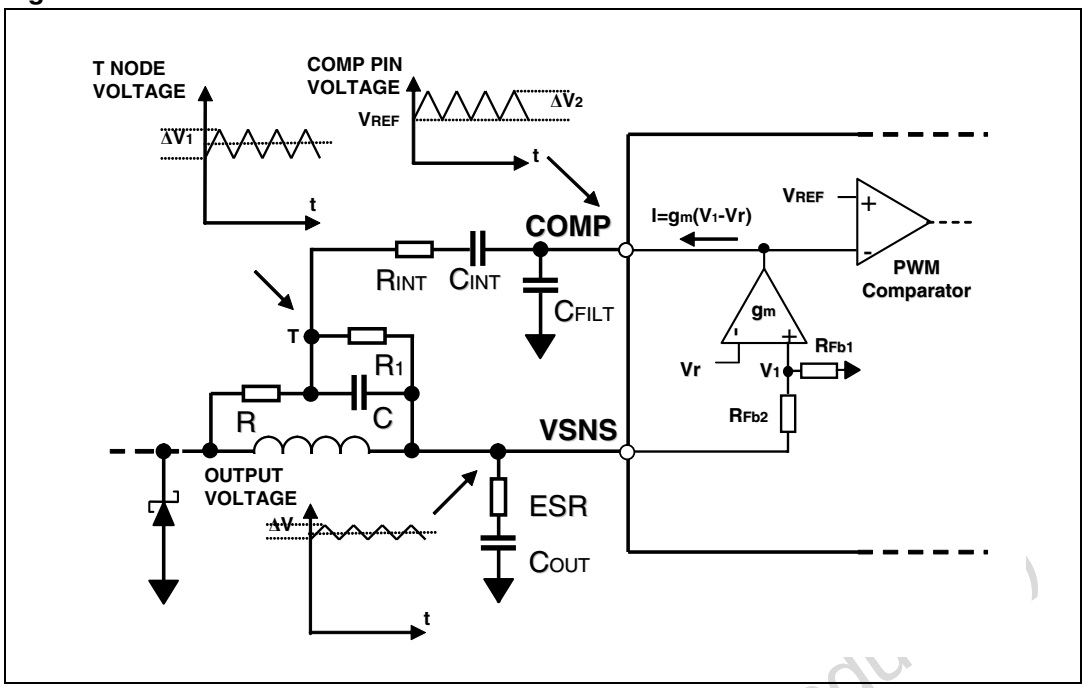
In order to reduce the noise on the COMP pin, it is possible to add a resistor R_{INT} that, together with CINT and C_{FILT}, becomes a low pass filter. The cutoff frequency f_{CUT} must be much greater (10 or more times) than the switching frequency:

Equation 9

$$R_{INT} = \frac{1}{2\pi \cdot f_{CUT} \cdot \frac{C_{INT} \cdot C_{FILT}}{C_{INT} + C_{FILT}}}$$

If the ripple is very small (lower than approximately 20mV), a different compensation network, called "Virtual-ESR" Network, is needed. This additional circuit generates a triangular ripple that is added to the output voltage ripple at the input of the integrator. The complete control scheme is shown in *Figure 8*.

Figure 8. "Virtual-ESR" network



The ripple on the COMP pin is the sum of the output voltage ripple and the triangular ripple generated by the Virtual-ESR Network. In fact the Virtual-ESR Network behaves like a another equivalent series resistor R_{VESR}.

A good trade-off is to design the network in order to achieve an R_{VESR} given by:

Equation 10

$$R_{VESR} = \frac{V_{RIPPLE}}{\Delta I_L} - ESR$$

where ΔI_L is the inductor current ripple and V_{RIPPLE} is the total ripple at the T node, chosen greater than approximately 20mV.

The new closed-loop gain depends on C_{INT}. In order to ensure stability it must be verified that:

Equation 11

$$C_{INT} > \frac{g_m}{2\pi \cdot f_Z} \cdot \frac{Vr}{Vout}$$

where:

Equation 12

$$f_Z = \frac{1}{2\pi \cdot C_{out} \cdot R_{TOT}}$$

and:

Equation 13

$$R_{TOT} = ESR + R_{VESR}$$

Moreover, the C_{INT} capacitor must meet the following condition:

Equation 14

$$f_{SW} > k \cdot f_Z = \frac{k}{2\pi \cdot C_{out} \cdot R_{TOT}}$$

where R_{TOT} is the sum of the ESR of the output capacitor and the equivalent ESR given by the Virtual-ESR Network (R_{VESR}). The k parameter must be greater than unity (k > 3) and determines the minimum integrator capacitor value C_{INT}:

Equation 15

$$C_{INT} > \frac{g_m}{2\pi \cdot \left(\frac{f_{SW}}{k} - f_Z\right)} \cdot \frac{Vr}{Vout}$$

The capacitor of the Virtual-ESR Network, C, is chosen as follow

Equation 16

$$C > 5 \cdot C_{INT}$$

and R is calculated to provide the desired triangular ripple voltage:

Equation 17

$$R = \frac{L}{R_{VESR} \cdot C}$$

Finally the R1 resistor is calculated according to expression 18:

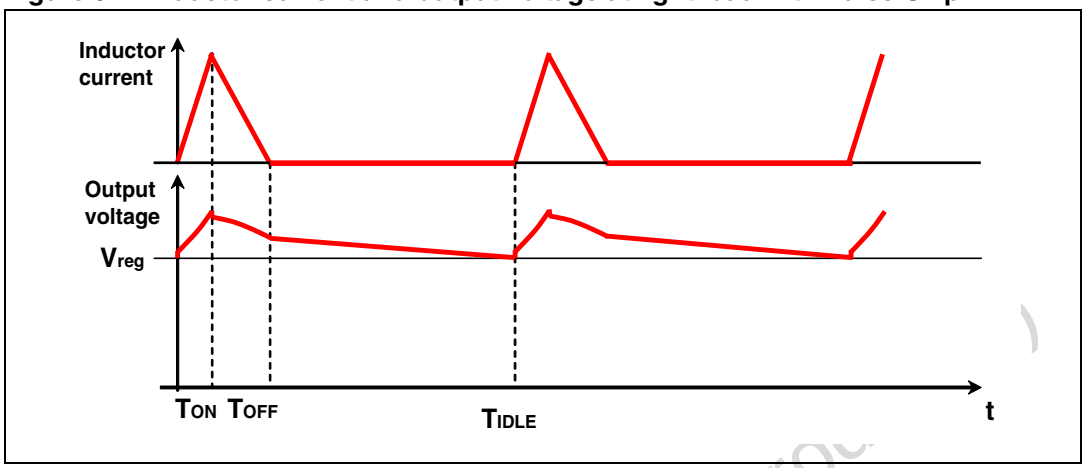
Equation 18

$$R1 = \frac{R \cdot \left(\frac{1}{\pi \cdot f_Z \cdot C}\right)}{R - \frac{1}{\pi \cdot f_Z \cdot C}}$$

6.1.3 Pulse-Skip and No-Audible Pulse-Skip Modes

High efficiency at light load conditions is achieved by PM6675 entering the Pulse-Skip Mode (if enabled). When one of the two fixed output voltages is set, Pulse-Skip power saving is a default feature. At light load conditions the zero-crossing comparator truncates the low-side switch on-time as soon as the inductor current becomes negative; in this way the comparator determines the On-Time duration instead of the output ripple (see *Figure 9*).

Figure 9. Inductor current and output voltage at light load with Pulse-Skip



As a consequence, the output capacitor is left floating and its discharge depends solely on the current drained from the load. When the output ripple on the pin COMP falls under the reference, a new shot is triggered and the next cycle begins. The Pulse-Skip mode is naturally obtained enabling the zero-crossing comparator and automatically takes part in the C.O.T. algorithm when the inductor current is about half the ripple current amount, i.e. migrating from continuous conduction mode (C.C.M.) to discontinuous conduction mode (D.C.M.).

The output current threshold related to the transition between PWM Mode and Pulse-Skip Mode can be approximately calculated as:

Equation 19

$$I_{LOAD}(PWM2Skip) = \frac{V_{IN} - V_{OUT}}{2 \cdot L} \cdot T_{ON}$$

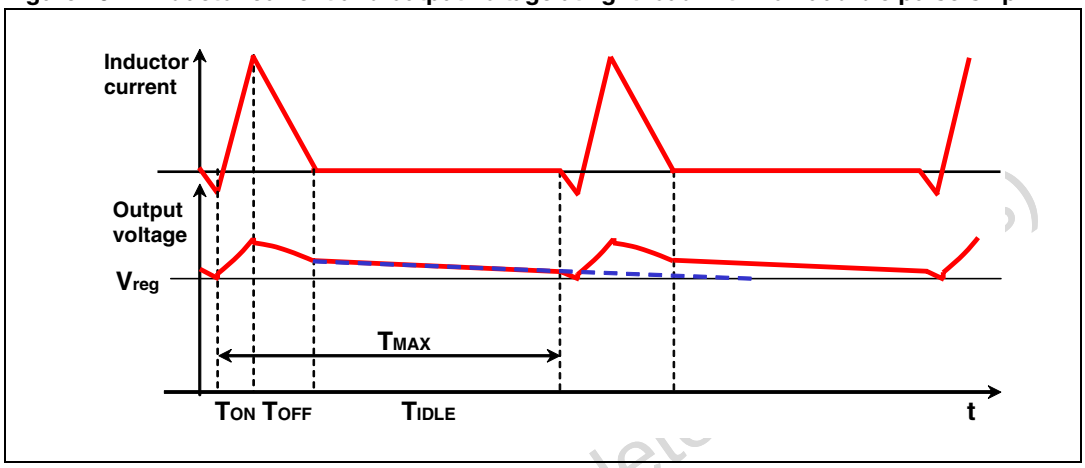
At higher loads, the inductor current never crosses the zero and the device works in pure PWM mode with a switching frequency around the nominal value.

A physiological consequence of Pulse-Skip Mode is a more noisy and asynchronous (than normal conditions) output, mainly due to very low load. If the Pulse-Skip is not compatible with the application, the PM6675, when set in adjustable mode-of-operation, allows the user to choose between forced-PWM and No-Audible Pulse-Skip alternative modes (see *Section 6.1.4: Mode-of-operation selection on page 24* for details).

No-Audible Pulse-Skip Mode

Some audio-noise sensitive applications cannot accept the switching frequency to enter the audible range as it is possible in Pulse-Skip mode with very light loads. For this reason, the PM6675 implements an additional feature to maintain a minimum switching frequency of 33kHz despite a slight efficiency loss. At very light load conditions, if any switching cycle has taken place within 30µs (typ.) since the last one (because of the output voltage is still higher than the reference), a No-Audible Pulse-Skip cycle begins. The low-side MOSFET is turned on and the output is driven to fall until the reference point has been crossed. Then, the high-side switch is turned on for a T_{ON} period and, once it has expired, the synchronous rectifier is enabled until the inductor current reaches the zero-crossing threshold (see *Figure 10*).

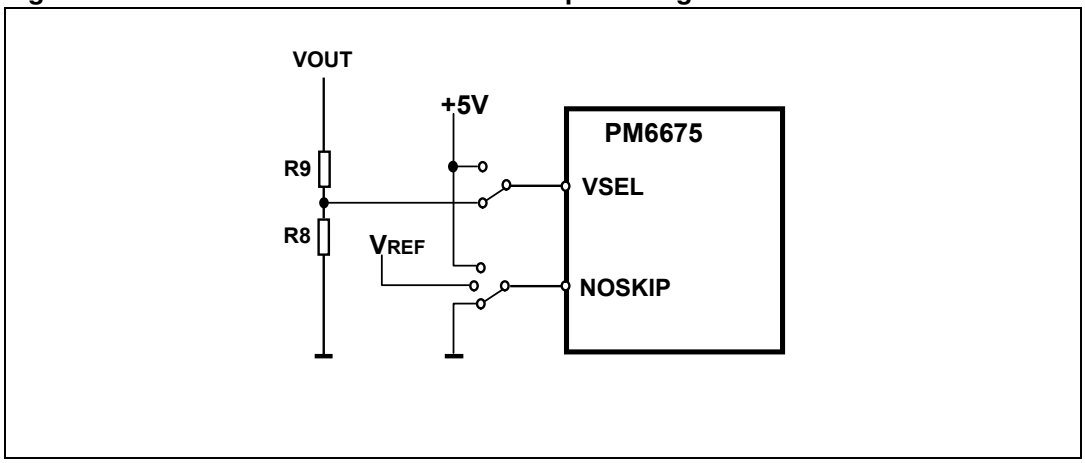
Figure 10. Inductor current and output voltage at light load with non-audible pulse-skip



For frequencies higher than 33kHz (due to heavier loads) the device works in the same way as in Pulse-Skip mode. It is important to notice that in both Pulse-Skip and No-Audible Pulse-Skip modes, the switching frequency changes not only with the load but also with the input voltage.

6.1.4 Mode-of-operation selection

Figure 11. VSEL and NOSKIP multifunction pin configurations



The PM6675 has been designed to satisfy the widest range of applications. The device is provided with some multilevel pins which allow the user to choose the appropriate configuration. The VSEL pin is used to firstly decide between fixed preset or adjustable (user defined) output voltages.

When the VSEL pin is connected to +5V, the PM6675 sets the switching section output voltage to 1.5V without the need of an external divider.

Applications requiring different output voltages can be managed by PM6675 simply setting the adjustable mode. Consider that if the VSEL pin voltage is higher than 4V, the fixed output mode is selected. When connecting an external divider to the VSEL pin, it is used as negative input of the error amplifier and the output voltage is given by expression (20).

Equation 20

$$VOUT_{ADJ} = 0.6 \cdot \frac{R8 + R9}{R8}$$

The output voltage can be set in the range from 0.6V to 3.3V.

The NOSKIP is the power saving algorithm selector: if tied to +5V, the forced-PWM (fixed frequency) control is performed. If grounded or connected to VREF pin (1.237V reference voltage), the Pulse-Skip or Non-Audible Pulse-Skip Modes are respectively selected.

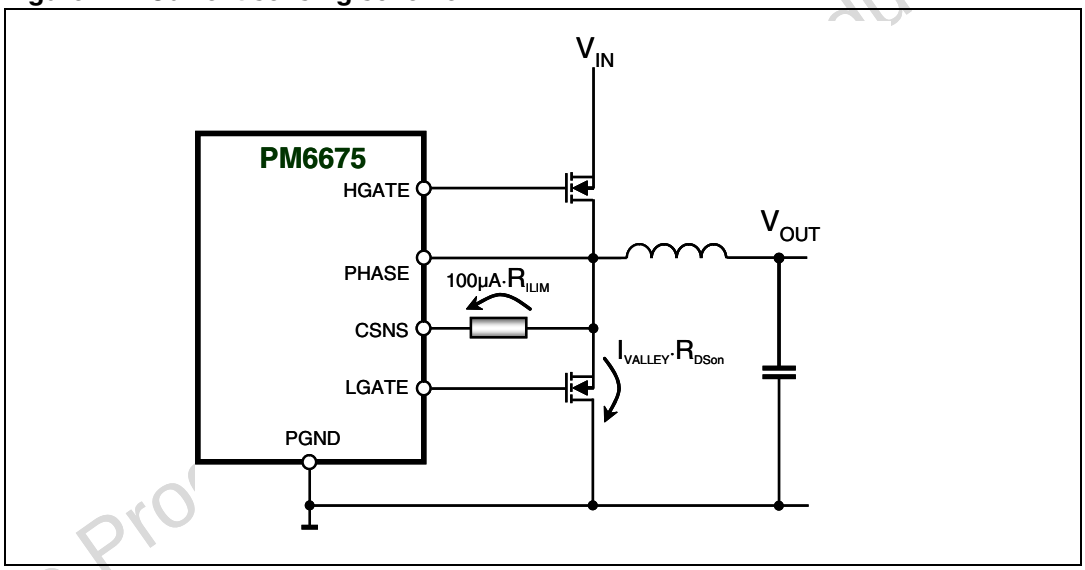
Table 6. Mode-of-operation settings summary

VSEL	NOSKIP	VOUT	Operating mode
V_{VSEL} > 4.3V	V_{NOSKIP} > 4.2V	1.5V	Forced-PWM
	1V <V_{NOSKIP} < 3.5V		Non-audible pulse-skip
	< 0.5V		Pulse-skip
V_{VSEL} < 3.7V	V_{NOSKIP} > 4.2V	ADJ	Forced-PWM
	1V <V_{NOSKIP} < 3.5V		Non-audible pulse-skip
	V_{NOSKIP} < 0.5V		Pulse-skip

6.1.5 Current sensing and current limit

The PM6675 switching controller uses a valley current sensing algorithm to properly handle the current limit protection and the inductor current zero-crossing information. The current is detected during the conduction time of the low-side MOSFET. The current sensing element is the on-resistance of the low-side switch. The sensing scheme is visible in *Figure 12*.

Figure 12. Current sensing scheme



An internal 100µA current source is connected to C_{SNS} pin that is also the non-inverting input of the positive current limit comparator. When the voltage drop developed across the sensing parameter equals the voltage drop across the programming resistor R_{ILIM}, the controller skips subsequent cycles until the overcurrent condition is detected or the output UV protection latches off the device (see *Section 6.1.11: Switching section OV and UV protections on page 28*).

Referring to *Figure 12*, the $R_{DS(on)}$ sensing technique allows high efficiency performance without the need for an external sensing resistor. The on-resistance of the MOSFET is affected by temperature drift and nominal value spread of the parameter itself; this must be considered during the R_{ILIM} setting resistor design.