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PM6680

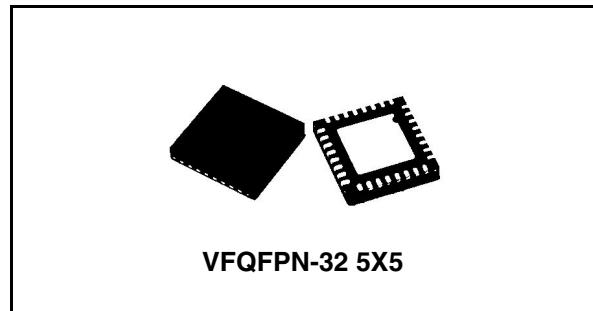
No Rsense dual step-down controller with adjustable voltages for notebook system power

Features

- 6 V to 28 V input voltage range
- Adjustable output voltages
- 5 V always voltage available deliver 100 mA peak current
- 1.237 V \pm 1% reference voltage available
- Lossless current sensing using low side MOSFETs $R_{DS(on)}$
- Negative current limit
- Soft-start internally fixed at 2ms
- Soft output discharge
- Latched OVP and UVP
- Selectable pulse skipping at light loads
- Selectable minimum frequency (33 kHz) in pulse skip mode
- 4 mW maximum quiescent power
- Independent power good signals
- Output voltage ripple compensation

Applications

- Notebook computers
- Tablet PC or slates
- Mobile system power supply
- 3-4 cells Li+ battery powered devices



Description

PM6680 is a dual step-down controller specifically designed to provide extremely high efficiency conversion, with lossless current sensing technique. The constant on-time architecture assures fast load transient response and the embedded voltage feed-forward provides nearly constant switching frequency operation. An embedded integrator control loop compensates the DC voltage error due to the output ripple. Pulse skipping technique increases efficiency at very light load. Moreover a minimum switching frequency of 33kHz is selectable to avoid audio noise issues. The PM6680 provides a selectable switching frequency, allowing three different values of switching frequencies for the two switching sections. The output voltages OUT1 and OUT2 can be adjusted from 0.9 V to 5.5 V and from 0.9 V to 3.3 V respectively.

Table 1. Device summary

Order codes	Package	Packaging
PM6680	VFQFPN-32 5mm x 5mm (Exposed pad)	Tray
PM6680TR		Tape and reel

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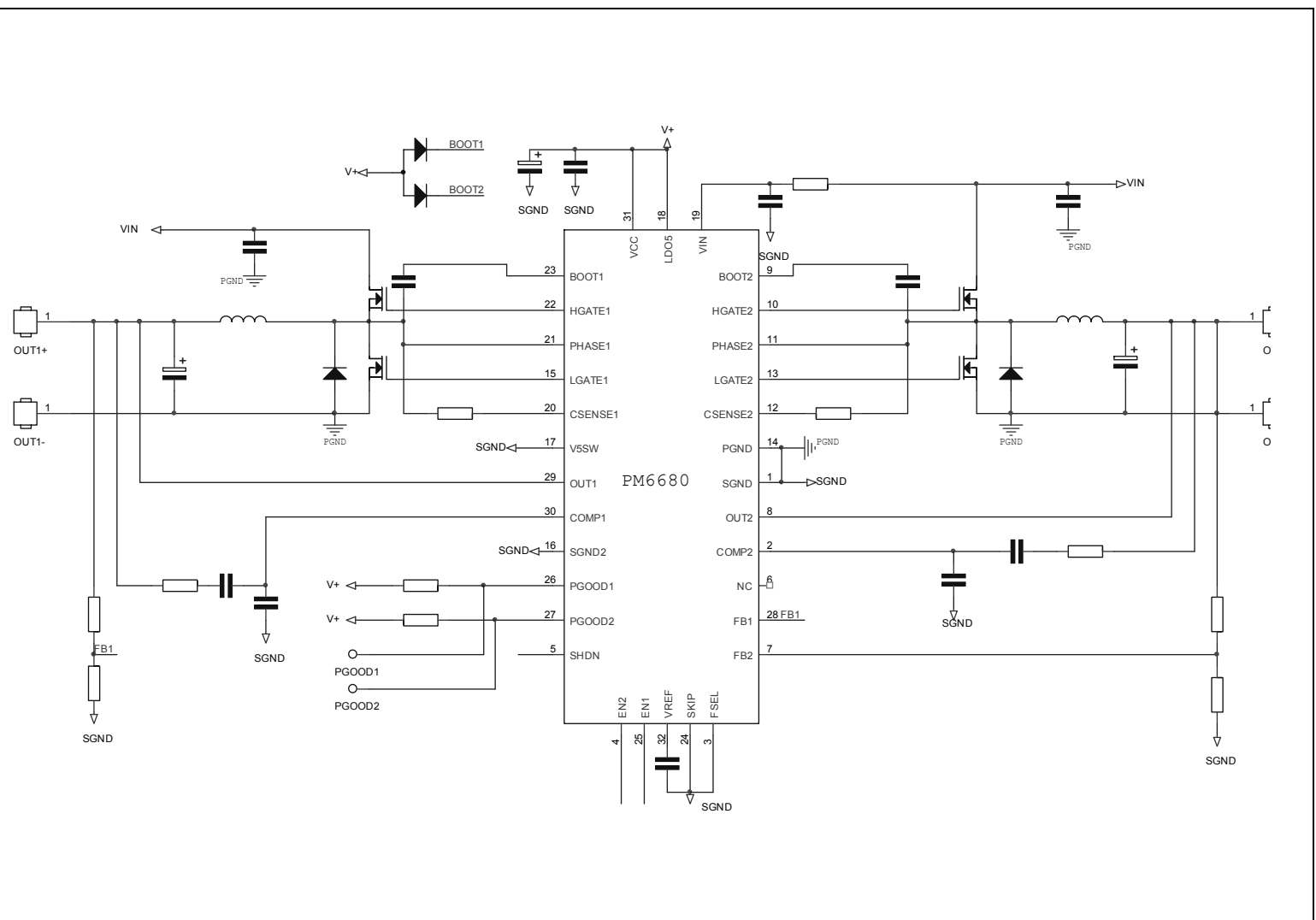
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1 Simplified application schematic

Figure 1. Simplified application schematic



2 Electrical data

2.1 Maximum rating

Table 2. Absolute maximum ratings

Parameter		Value	Unit
V5SW, LDO5 to PGND		-0.3 to 6	V
VIN to PGND		-0.3 to 36	V
HGATE _x and BOOT _x , to PHASE _x		-0.3 to 6	V
PHASE _x to PGND		-0.6 ⁽¹⁾ to 36	V
CSENSE _x , to PGND		-0.6 to 42	V
CSENSE _x to BOOT _x		-6 to 0.3	V
LGATE _x to PGND		-0.3 ⁽²⁾ to LDO5 +0.3	V
FB _x , COMP _x , SKIP, , FSEL,VREF to SGND1,SGND2		-0.3 to V _{cc} +0.3	V
PGND to SGND1,SGND2		-0.3 to 0.3	V
SHDN,PGOOD _x , OUT _x , VCC, EN _x to SGND1,SGND2		-0.3 to 6	V
Power dissipation at T _A = 25°C		2.8	W
Maximum withstanding voltage range test condition: CDF-AEC-Q100-002- "Human Body Model" acceptance criteria: "Normal Performance"	VIN	±1000	V
	Other pins	±2000	

1. PHASE to PGND up to -2.5 V for t<10 ns

2. LGATE_x to PGND up to -1 V for t<40 ns

2.2 Thermal data

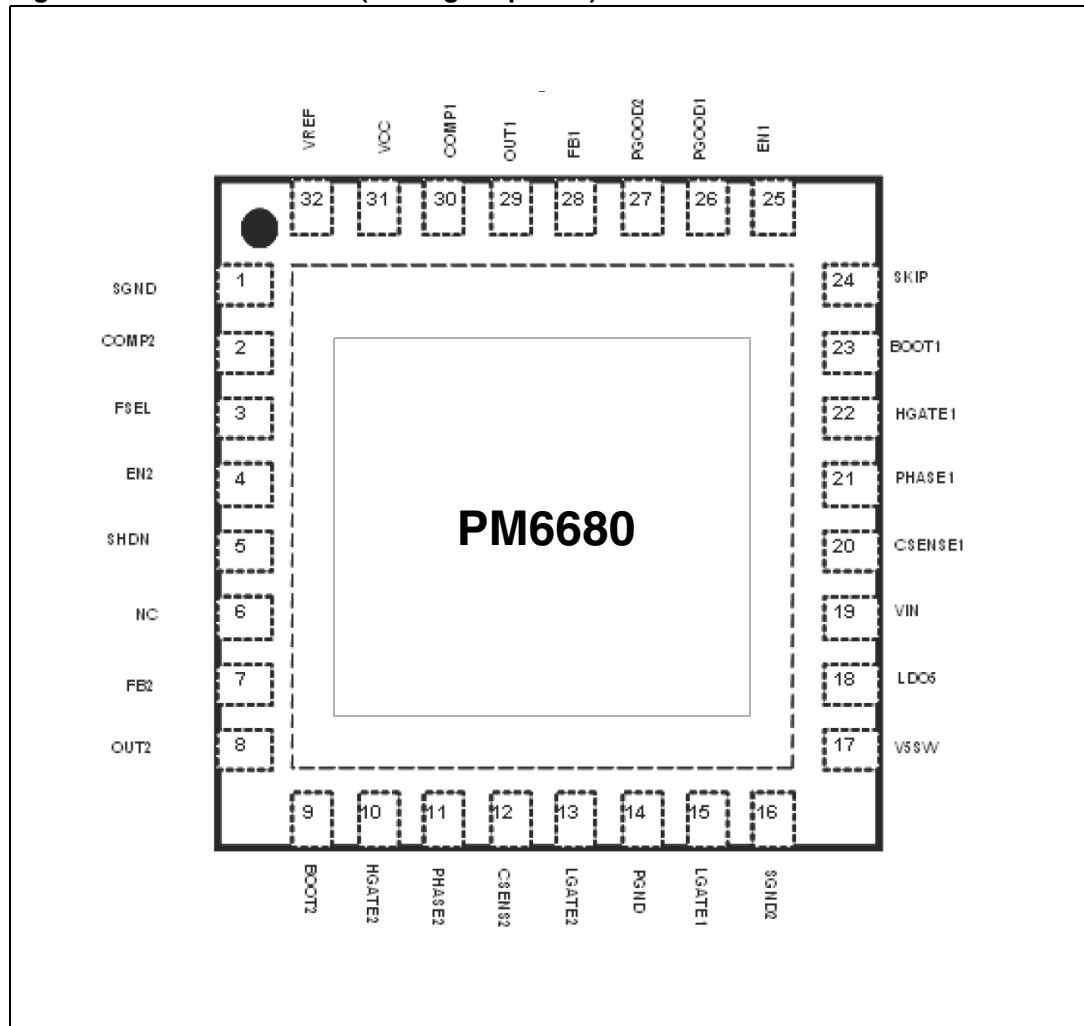
Table 3. Thermal data

Symbol	Parameter	Value	Unit
R _{thJA}	Thermal resistance junction to ambient	35	°C/W
T _{STG}	Storage temperature range	-50 to 150	°C
T _J	Junction operating temperature range	-40 to 125	°C
T _A	Operating ambient temperature range	-40 to 85	°C

3 Pin settings

3.1 Connections

Figure 2. Pin connection (Through top view)



3.2 Functions

Table 4. Pin functions

N°	Pin	Function
1	SGND1	Signal ground. Reference for internal logic circuitry. It must be connected to the signal ground plan of the power supply. The signal ground plan and the power ground plan must be connected together in one point near the PGND pin.
2	COMP2	DC voltage error compensation pin for the switching section 2
3	FSEL	Frequency selection pin. It provides a selectable switching frequency, allowing three different values of switching frequencies for the switching sections.
4	EN2	Enable input for the switching section 2. <ul style="list-style-type: none"> • The section 2 is enabled applying a voltage greater than 2.4 V to this pin. • The section 2 is disabled applying a voltage lower than 0.8 V. When the section is disabled the High Side gate driver goes low and Low Side gate driver goes high. If both EN1 and EN2 pins are low and SHDN pin is high the device enters in standby mode.
5	SHDN	Shutdown control input. <ul style="list-style-type: none"> • The device switch off if the SHDN voltage is lower than the device off threshold (Shutdown mode) • The device switch on if the SHDN voltage is greater than the device on threshold. The SHDN pin can be connected to the battery through a voltage divider to program an undervoltage lockout. In shutdown mode, the gate drivers of the two switching sections are in high impedance (high-Z).
6	NC	Not connected.
7	FB2	Feedback input for the switching section 2 This pin is connected to a resistive voltage-divider from OUT2 to PGND to adjust the output voltage from 0.9 V to 3.3 V.
8	OUT2	Output voltage sense for the switching section 2.This pin must be directly connected to the output voltage of the switching section.
9	BOOT2	Bootstrap capacitor connection for the switching section 2. It supplies the high-side gate driver.
10	HGATE2	High-side gate driver output for section 2. This is the floating gate driver output.
11	PHASE2	Switch node connection and return path for the high side driver for the section 2.It is also used as negative current sense input.
12	CSENSE2	Positive current sense input for the switching section 2. This pin must be connected through a resistor to the drain of the synchronous rectifier (R_{DSON} sensing) to obtain a positive current limit threshold for the power supply controller.
13	LGATE2	Low-side gate driver output for the section 2.
14	PGND	Power ground. This pin must be connected to the power ground plan of the power supply.
15	LGATE1	Low-side gate driver output for the section 1.

Table 4. Pin functions (continued)

N°	Pin	Function
16	SGND2	Signal ground for analog circuitry. It must be connected to the signal ground plan of the power supply.
17	V5SW	Internal 5 V regulator bypass connection. <ul style="list-style-type: none"> • If V5SW is connected to OUT5 (or to an external 5 V supply) and V5SW is greater than 4.9 V, the LDO5 regulator shuts down and the LDO5 pin is directly connected to OUT5 through a 3 Ω (max) switch. • If V5SW is connected to GND, the LDO5 linear regulator is always on.
18	LDO5	5 V internal regulator output. It can provide up to 100mA peak current. LDO5 pin supplies embedded low side gate drivers and an external load.
19	VIN	Device supply voltage input and battery voltage sense. A bypass filter (4 Ω and 4.7 μF) between the battery and this pin is recommended.
20	CSENSE1	Positive current sense input for the switching section 1. This pin must be connected through a resistor to the drain of the synchronous rectifier ($R_{DS(on)}$ sensing) to obtain a positive current limit threshold for the power supply controller.
21	PHASE1	Switch node connection and return path for the high side driver for the section 1. It is also used as negative current sense input.
22	HGATE1	High-side gate driver output for section 1. This is the floating gate driver output.
23	BOOT1	Bootstrap capacitor connection for the switching section 1. It supplies the high-side gate driver.
24	SKIP	Pulse skipping mode control input. <ul style="list-style-type: none"> • If the pin is connected to LDO5 the PWM mode is enabled. • If the pin is connected to GND, the pulse skip mode is enabled. • If the pin is connected to VREF the pulse skip mode is enabled but the switching frequency is kept higher than 33 kHz (No-audible pulse skip mode).
25	EN1	Enable input for the switching section 1. <ul style="list-style-type: none"> • The section 1 is enabled applying a voltage greater than 2.4 V to this pin. • The section 1 is disabled applying a voltage lower than 0.8 V. When the section is disabled the High Side gate driver goes low and Low Side gate driver goes high.
26	PGOOD1	Power Good output signal for the section 1. This pin is an open drain output and when the output of the switching section 1 is out of +/- 10 % of its nominal value. It is pulled down.
27	PGOOD2	Power Good output signal for the section 2. This pin is an open drain output and when the output of the switching section 2 is out of +/- 10 % of its nominal value. It is pulled down.
28	FB1	Feedback input for the switching section 1. This pin is connected to a resistive voltage-divider from OUT1 to PGND to adjust the output voltage from 0.9 V to 5.5 V.

Table 4. Pin functions (continued)

N°	Pin	Function
29	OUT1	Output voltage sense for the switching section 1. This pin must be directly connected to the output voltage of the switching section.
30	COMP1	DC voltage error compensation pin for the switching section 1.
31	VCC	Device Supply Voltage pin. It supplies all the internal analog circuitry except the gate drivers (see LDO5). Connect this pin to LDO5.
32	VREF	Internal 1.237 V high accuracy voltage reference. It can deliver 50 uA. Bypass to SGND with a 100 nF capacitor to reduce noise.

4 Electrical characteristics

Table 5. Electrical characteristics
 $V_{IN} = 12\text{ V}$, $T_A = 0\text{ °C}$ to 85 °C , unless otherwise specified ⁽¹⁾

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Supply section						
V _{IN}	Input voltage range	V _{out} = V _{ref} , LDO5 in regulation	5.5		28	V
V _{CC}	IC supply voltage		4.5		5.5	V
V _{V5SW}	Turn-on voltage threshold			4.8	4.9	V
	Turn-off voltage threshold		4.6	4.75		V
	Hysteresis		20	50		mV
V _{V5SW}	Maximum operating range				5.5	V
R _{dson}	LDO5 internal bootstrap switch resistance	V _{5SW} > 4.9		1.8	3	Ω
	OUTx,OUTx discharge-mode on-resistance			18	25	Ω
	OUTx,OUTx discharge-mode synchronous rectifier Turn-on level		0.2	0.36	0.6	V
P _{in}	Operating power consumption	FBx > V _{REF} , V _{ref} in regulation, V _{5WS} to 5 V			4	mW
I _{sh}	Operating current sunk by V _{IN}	SHDN connected to GND,		14	18	μA
I _{sb}	Operating current sunk by V _{IN}	ENx to GND, V _{5SW} to GND		190	250	μA
Shutdown section						
V _{SHDN}	Device on threshold		1.2	1.5	1.7	V
	Device off threshold		0.8	0.85	0.9	V
Soft start section						
	Soft start ramp time		2		3.5	ms
Current limit and zero crossing comparator						
I _{CSENSE}	Input bias current limit		90	100	110	μA
	Comparator offset	V _{CSENSE} -V _{PGND}	-6		6	mV
	Zero crossing comparator offset	V _{PGND} - V _{PHASE}	-1		11	mV
	Fixed negative current limit threshold	V _{PGND} - V _{PHASE}		-120		mV

Table 5. Electrical characteristics (continued)
 $V_{IN} = 12\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$, unless otherwise specified ⁽¹⁾

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	
On time pulse width							
Ton	On time duration	FSEL to GND	OUT1=1.5 V	550	650	750	ns
			OUT2=1.05 V	230	270	315	
		FSEL to VREF	OUT1=1.5 V	375	445	515	
			OUT2=1.05 V	175	210	245	
		FSEL to LDO5	OUT1=1.5 V	285	340	395	
			OUT2=1.05 V	125	150	175	
OFF time							
T _{OFFMIN}	Minimum off time			350	500	ns	
Voltage reference							
V _{REF}	Voltage accuracy	4 V < V _{LDO5} < 5.5 V	1.224	1.236	1.249	V	
	Load regulation	-100 μA < I _{REF} < 100 μA	-4		4	mV	
	Undervoltage lockout fault threshold	Falling edge of REF			0.95	mV	
Integrator							
FB	Voltage accuracy		-909	900	909	mV	
FB	Input bias current			0.1		μA	
COMP	Over voltage clamp	Normal mode		250		mV	
		Pulse skip mode		60			
	Under voltage clamp			-150			
Line regulation							
		Both SMPS, 6 V < V _{in} < 28 V ⁽²⁾		0.004		%/V	
LDO5 linear regulator							
V _{LDO5}	LDO5 linear output voltage	6 V < V _{IN} < 28 V , 0 < I _{LDO5} < 50 mA	4.9	5.0	5.1	V	
	LDO5 line regulation	6 V < V _{IN} < 28 V , I _{LDO5} = 20 mA ,			0.004	%/V	
I _{LDO5}	LDO5 Current limit	V _{LDO5} > UVLO	270	330	400	mA	
ULVO	Under Voltage Lockout of LDO5		3.94	4	4.13	V	

Table 5. Electrical characteristics (continued)
 $V_{IN} = 12\text{ V}$, $T_A = 0\text{ °C}$ to 85 °C , unless otherwise specified ⁽¹⁾

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
High and low gate drivers						
	HGATE driver on-resistance	HGATEx high state (pullup)		2.0	3	Ω
		HGATEx low state (pulldown)		1.6	2.7	Ω
	LGATE driver on-resistance	LGATEx high state (pullup)		1.4	2.1	Ω
		LGATEx low state (pulldown)		0.8	1.2	Ω
PGOOD pins UVP/OVP protections						
OVP	Over voltage threshold	Both SMPS sections with respect to VREF.	112	116	120	%
UVP	Under voltage threshold		65	68	71	%
PGOOD1,2	Upper threshold (VFB-VREF)		107	110	113	%
	Lower threshold (VFB-VREF)		88	91	94	%
$I_{PGOOD1,2}$	PGOOD leakage current	$V_{PGOOD1,2}$ forced to 5.5 V			1	μA
$V_{PGOOD1,2}$	Output low voltage	ISink = 4 mA		150	250	mV
Thermal shutdown						
T_{SDN}	Shutdown temperature			150		$^{\circ}\text{C}$
Power management pins						
EN1,2	SMPS disabled level				0.8	V
	SMPS enabled level		2.4			
FSEL	Frequency selection range	Low level ⁽³⁾			0.5	V
		Middle level ⁽³⁾	1.0		$V_{LDO5}-1.5$	
		High level ⁽³⁾	$V_{LDO5}-0.8$			
SKIP	Pulse skip mode	⁽³⁾			0.5	V
	Ultrasonic mode	⁽³⁾	1.0		$V_{LDO5}-1.5$	
	PWM mode	⁽³⁾	$V_{LDO5}-0.8$			
	Input leakage current	$V_{EN1,2} = 0$ to 5 V			1	μA
		$V_{SKIP} = 0$ to 5 V			1	
		$V_{SHDN} = 0$ to 5 V			1	
		$V_{FSEL} = 0$ to 5 V			1	

- $T_A = T_J$. All parameters at operating temperature extremes are guaranteed by design and statistical analysis (not production tested).
- by design
- by demoboard test

5 Typical operating characteristics

FSEL = GND (200/300 kHz), SKIP = GND (skip mode), V5SW = V5SW = EXT5V (external 5 V power supply connected), input voltage VIN = 12 V, SHDN, EN1 and EN2 high, OUT1 = 1.5 V, OUT2 = 1.05 V, no load unless specified)

Figure 3. 1.5 V output efficiency vs load current

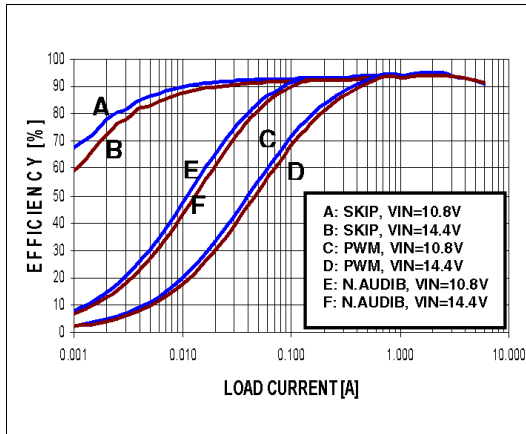


Figure 4. 1.05 V output efficiency vs load current

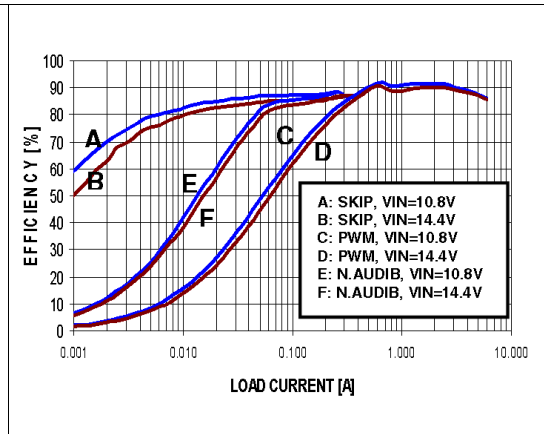


Figure 5. PWM no load input battery vs input voltage

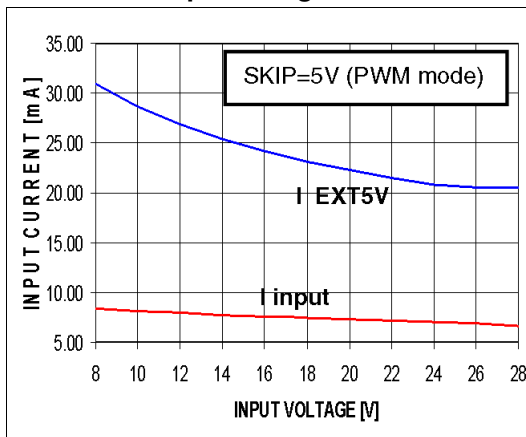


Figure 6. Skip no load battery current

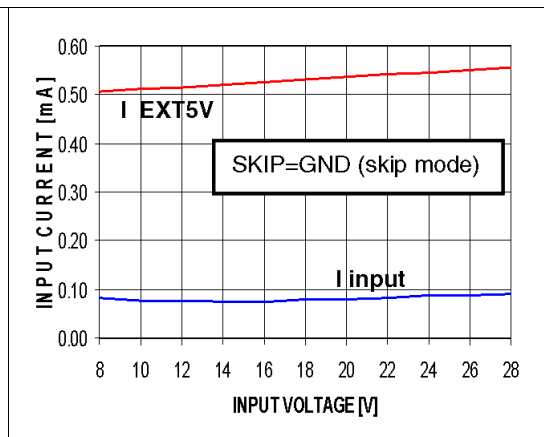


Figure 7. No-audible skip no load battery current vs input voltage

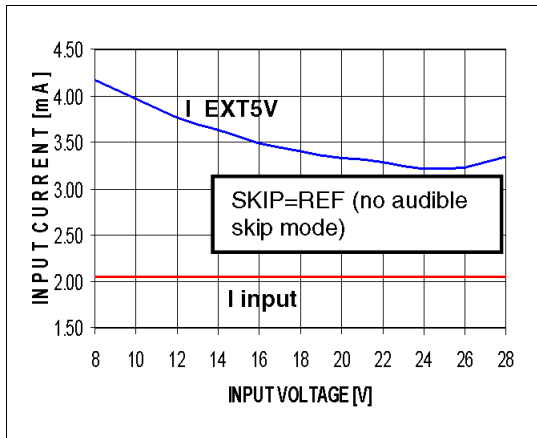


Figure 8. Stand-by mode input battery current vs input voltage

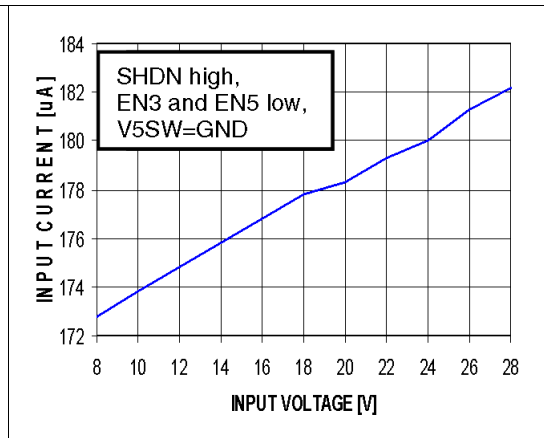


Figure 9. Shutdown mode input battery current vs input voltage

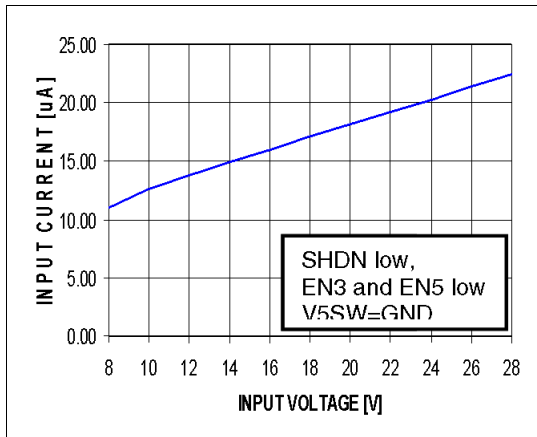


Figure 10. 1.5 V switching frequency vs load current

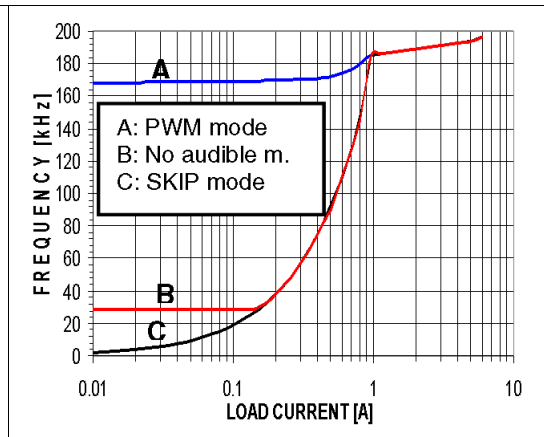


Figure 11. 1.05 V switching frequency vs load current

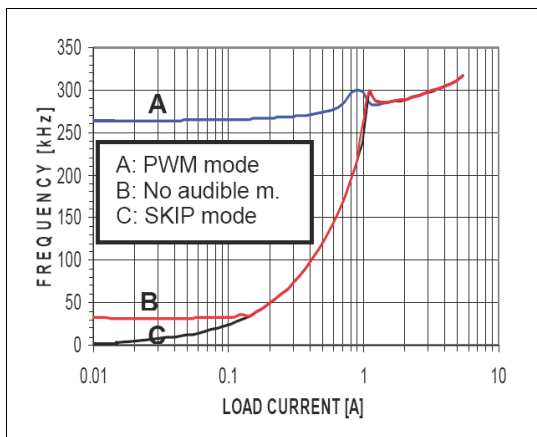


Figure 12. LDO5 vs output current load current

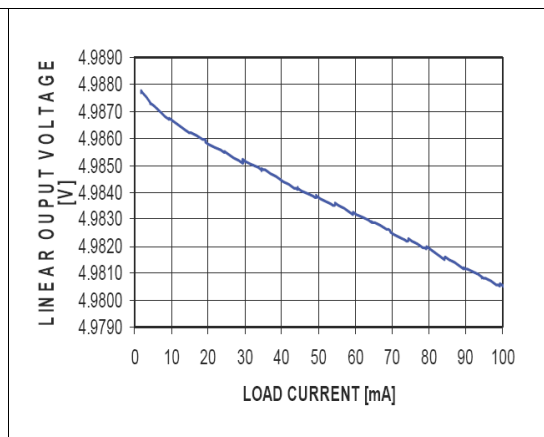


Figure 13. 1.5 V voltage regulation vs load current

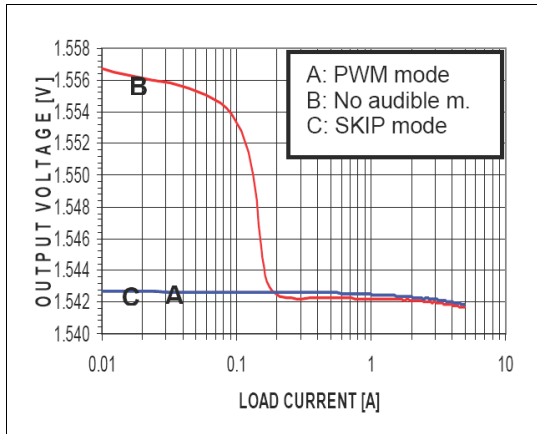


Figure 14. 1.05 V voltage regulation vs load current

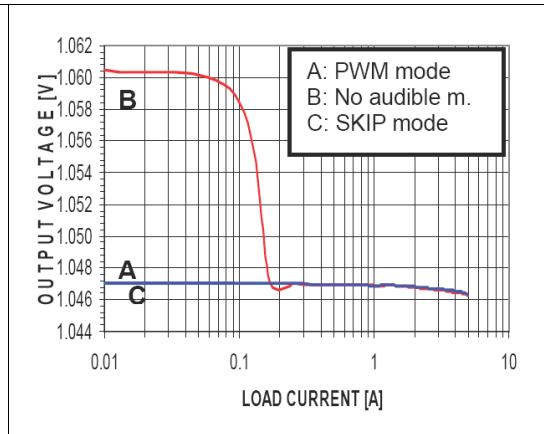


Figure 15. Voltage reference vs load current

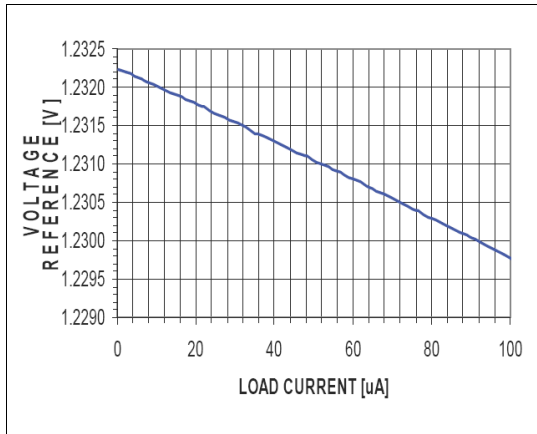


Figure 16. OUT1, OUT2 and LDO5 power-up

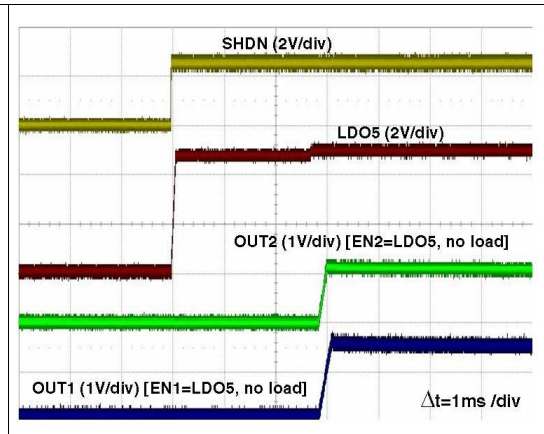


Figure 17. 1.5 V load transient

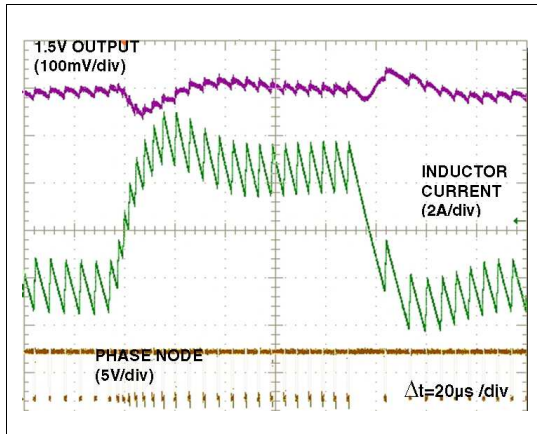


Figure 18. 1.05 V load transient

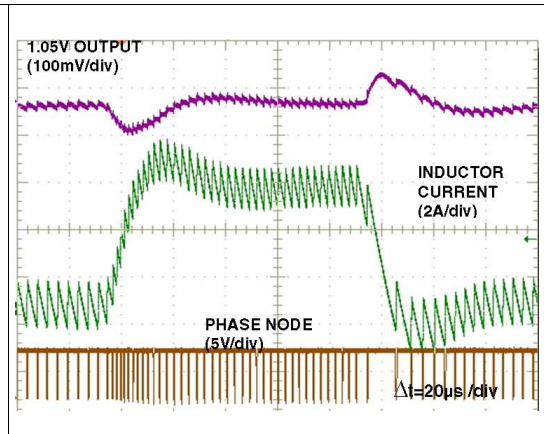


Figure 19. 1.5 V soft start (0.25Ω load)

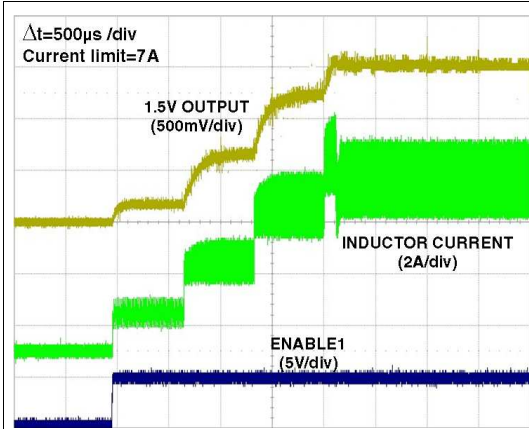


Figure 20. 1.05 V soft start (0.175Ω load)

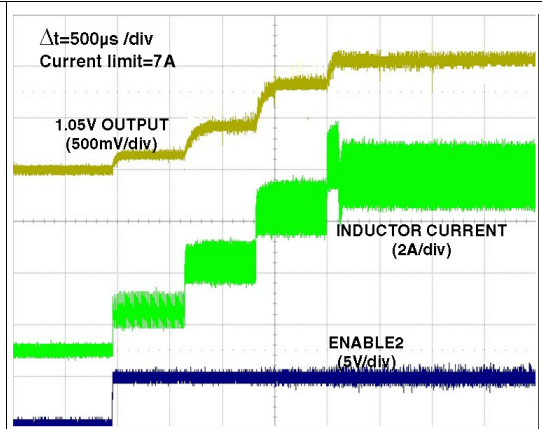


Figure 21. 1.5 V soft end (No load)

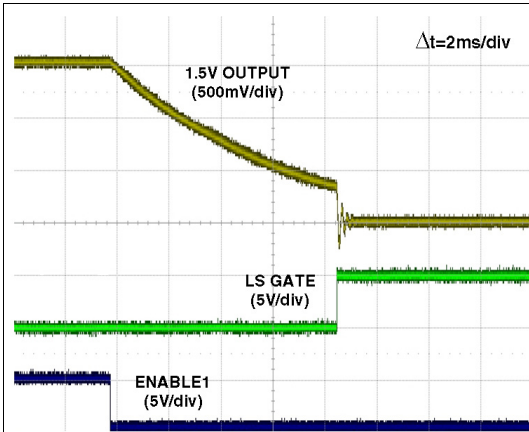


Figure 22. 1.05 V soft end (No load)

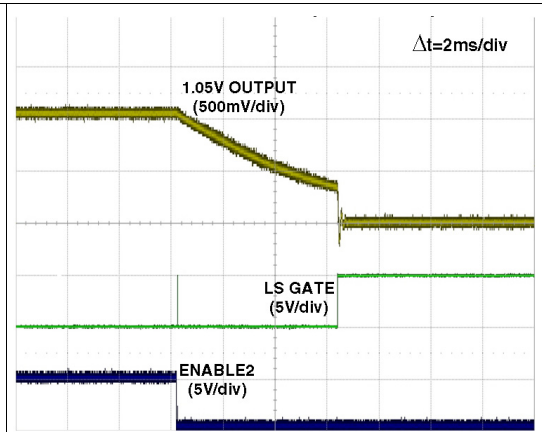


Figure 23. 1.5 V soft end (1Ω Load)

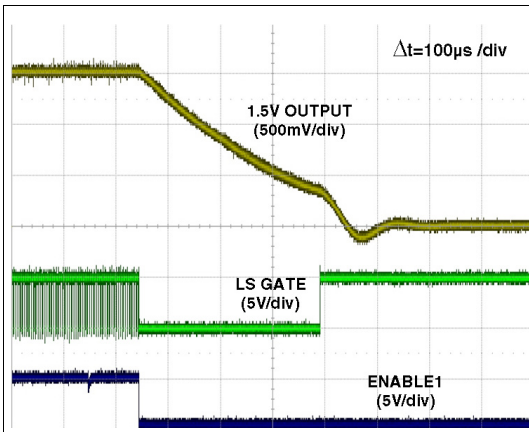


Figure 24. 1.05 V soft end (1Ω Load)

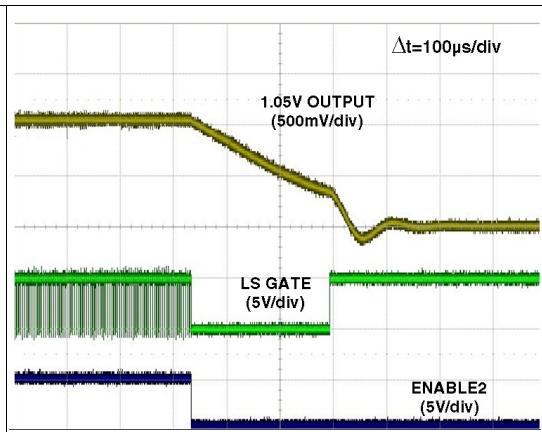
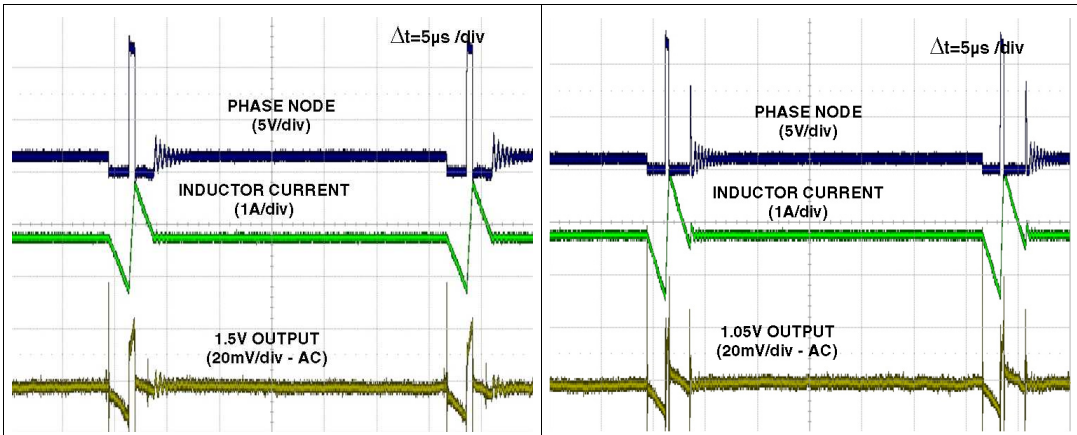


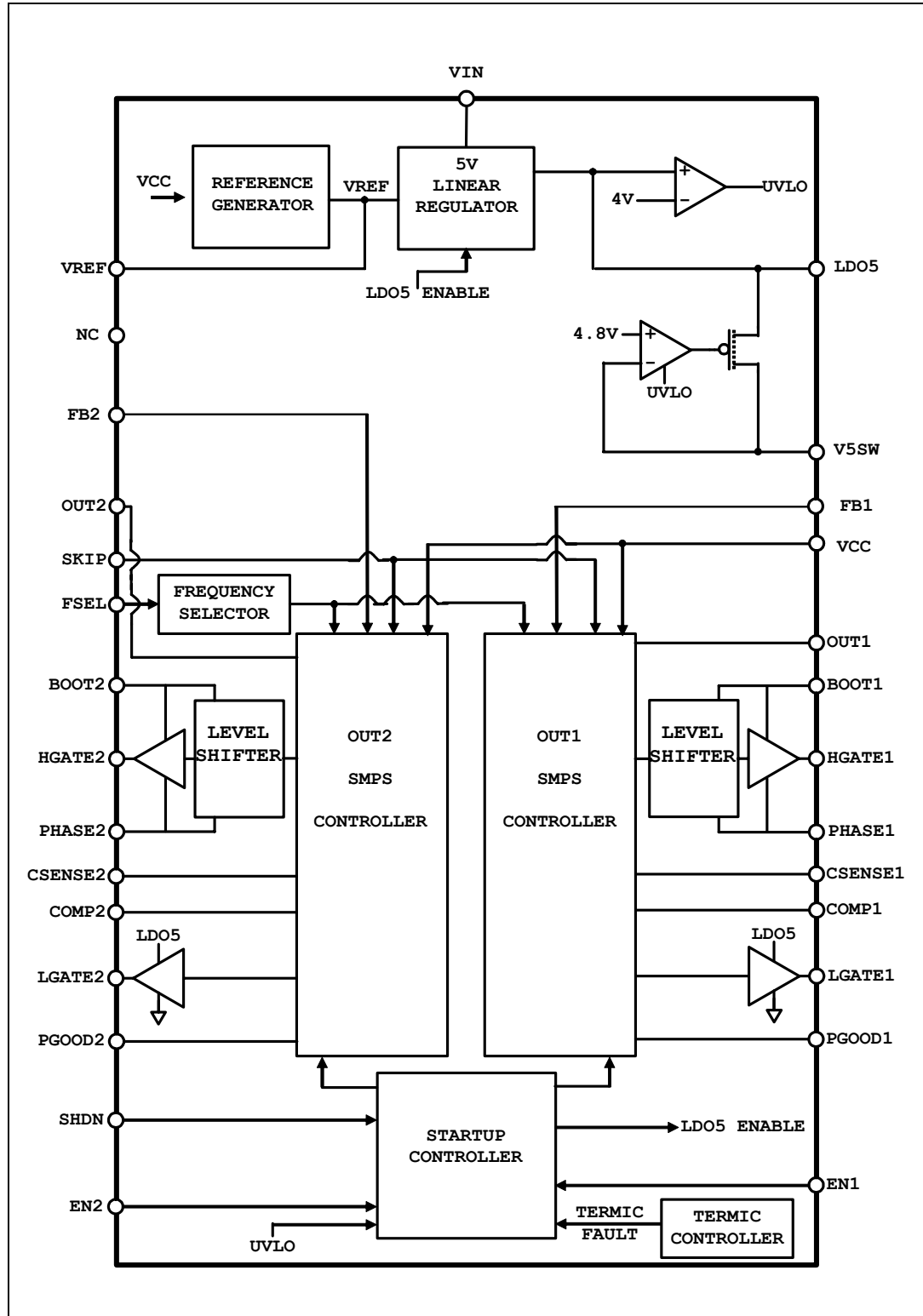
Figure 25. 1.5 V no-audible skip mode

Figure 26. 1.05 V no-audible skip mode



6 Block diagram

Figure 27. Functional block diagram



7 Device description

The PM6680 is a dual step-down controller dedicated to provide logic voltages for notebook computers.

It is based on a Constant On Time control architecture. This type of control offers a very fast load transient response with a minimum external component count. A typical application circuit is shown in [Figure 27](#).

The PM6680 regulates two adjustable output voltages: OUT1 and OUT2. The switching frequency of the two sections can be adjusted to 200/300 kHz, 300/400 kHz or 400/500 kHz respectively. In order to maximize the efficiency at light load condition, a pulse skipping mode can be selected.

The PM6680 includes also a 5 V linear regulator (LDO5) that can power the switching drivers. If the output OUT1 regulates 5 V, in order to maximize the efficiency in higher consumption status, the linear regulator can be turned off and their outputs can be supplied directly from the switching outputs. The PM6680 provides protection versus overvoltage, undervoltage and over temperature as well as power good signals for monitoring purposes. An external 1.237 V reference is available.

7.1 Constant On time PWM control

If the SKIP pin is tied to 5 V, the device works in PWM mode. Each power section has an independent on time control. The PM6680 employs a pseudo-fixed switching frequency, Constant On Time (COT) controller as core of the switched mode section. Each power section has an independent COT control.

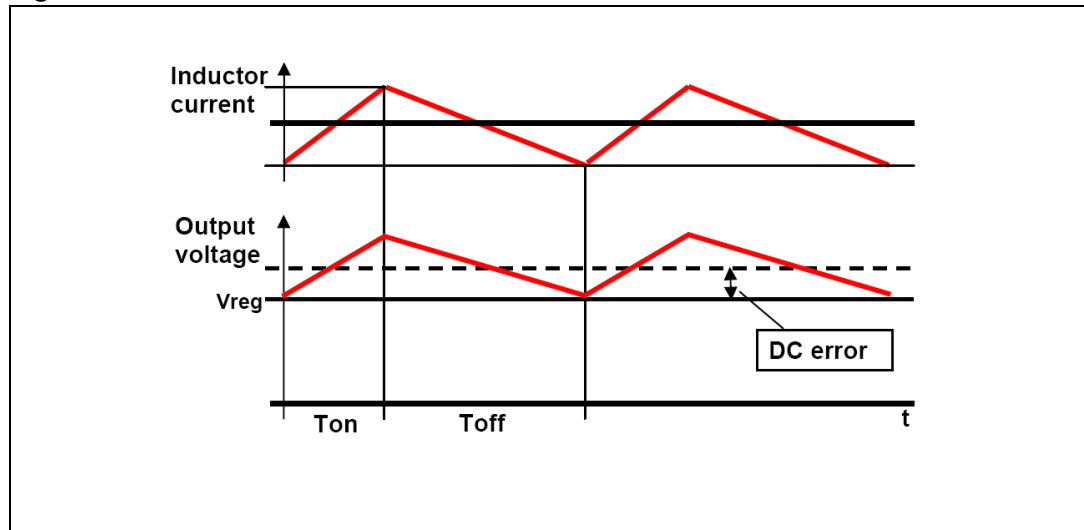
The COT controller is based on a relatively simple algorithm and uses the ripple voltage due to the output capacitor's ESR to trigger the fixed on-time one-shot generator. In this way, the output capacitor's ESR acts as a current sense resistor providing the appropriate ramp signal to the PWM comparator. On-time one-shot duration is directly proportional to the output voltage, sensed at the OUT1/OUT2 pins, and inversely proportional to the input voltage, sensed at the VIN pin, as follows:

Equation 1

$$T_{ON} = K \cdot \frac{V_{OUT}}{V_{IN}}$$

This leads to a nearly constant switching frequency, regardless of input and output voltages. When the output voltage goes lower than the regulated voltage V_{reg} , the on-time one shot generator directly drives the high side MOSFET for a fixed on time allowing the inductor current to increase; after the on time, an off time phase, in which the low side MOSFET is turned on, follows. [Figure 28](#) shows the inductor current and the output voltage waveforms in PWM mode.

Figure 28. Constant ON time PWM control



The duty cycle of the buck converter in steady state is:

Equation 2

$$D = \frac{V_{OUT}}{V_{IN}}$$

The PWM control works at a nearly fixed frequency f_{SW} :

Equation 3

$$f_{SW} = \frac{\frac{V_{OUT}}{V_{IN}}}{K_{on} \times \frac{V_{OUT}}{V_{IN}}} = 1/K_{on}$$

As mentioned the steady state switching frequency is theoretically independent from battery voltage and from output voltage.

Actually the frequency depends on parasitic voltage drops that are present during the charging path (high side switch resistance, inductor resistance (DCR)) and discharging path (low side switch resistance, DCR).

As a result the switching frequency increases as a function of the load current.

Standard switching frequency values can be selected for both sections by pin FSEL as shown in the following table:

Table 6. FSEL pin selection: typical switching frequency

	Fsw@OUT1 = 1.5 V (kHz)	Fsw@OUT2 = 1.05 V (kHz)
FSEL = GND	200	325
FSEL = VREF	290	425
FSEL = LDO5	390	590

7.2 Constant on time architecture

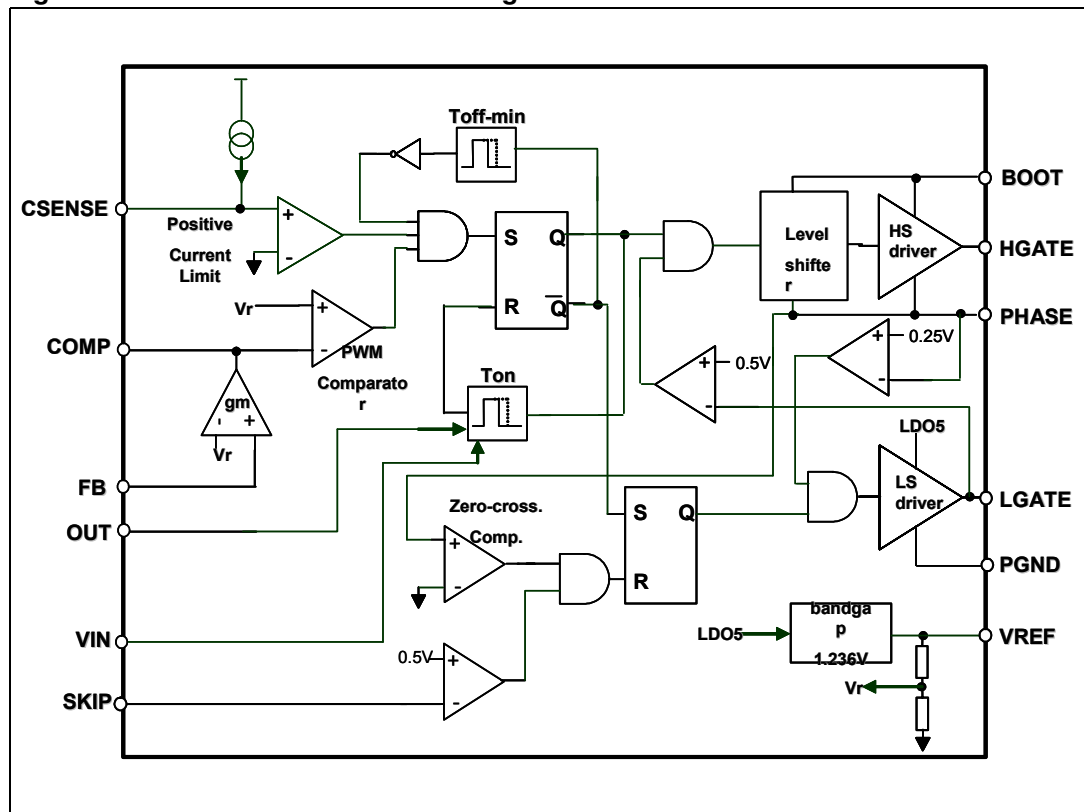
Figure 29 shows the simplified block diagram of a Constant On Time controller. A minimum off-time constrain (300 ns typ.) is introduced to allow inductor valley current sensing on synchronous switch. A minimum on-time (70 ns) is also introduced to assure the start-up switching sequence.

PM6680 has a one-shot generator for each power section that turns on the high side MOSFET when the following conditions are satisfied simultaneously: the PWM comparator is high, the synchronous rectifier current is below the current limit threshold, and the minimum off-time has timed out.

Once the on-time has timed out, the high side switch is turned off, while the synchronous switch is turned on according to the anti-cross conduction circuitry management.

When the negative input voltage at the PWM comparator (Figure 29), which is a scaled-down replica of the output voltage (see the external R1/R2 divider in Figure 29), reaches the valley limit (determined by internal reference $V_r = 0.9\text{ V}$), the low-side MOSFET is turned off according to the anti-cross conduction logic once again, and a new cycle begins.

Figure 29. Constant on-time block diagram

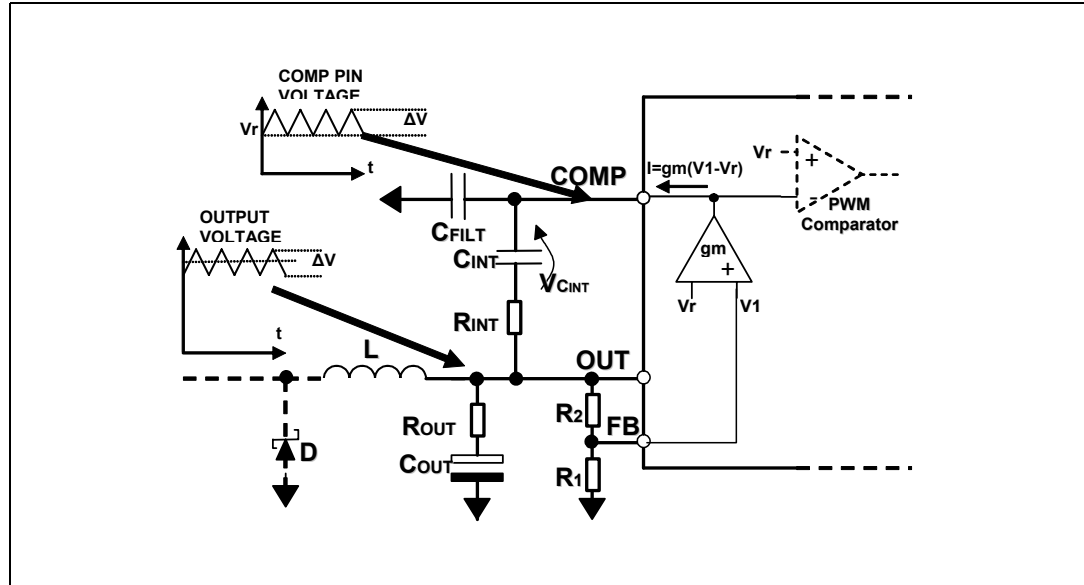


7.3 Output ripple compensation and loop stability

In a classic Constant On Time control, the system regulates the valley value of the output voltage and not the average value, as shown in [Figure 28](#). In this condition, the output voltage ripple is source of a DC static error.

To compensate this error, an integrator network can be introduced in the control loop, by connecting the output voltage to the COMP1/COMP2 (for the OUT1 and OUT2 sections respectively) pin through a capacitor C_{INT} as in [Figure 30](#).

Figure 30. Circuitry for output ripple compensation



The integrator amplifier generates a current, proportional to the DC errors between the FB voltage and V_r , which decreases the output voltage in order to compensate the total static error, including the voltage drop on PCB traces. In addition, C_{INT} provides an AC path for the output ripple. In steady state, the voltage on COMP1/COMP2 pin is the sum of the reference voltage V_r and the output ripple (see [Figure 30](#)). In fact when the voltage on the COMP pin reaches V_r , a fixed T_{on} begins and the output increases.

For example, we consider $V_{out} = 5\text{ V}$ with an output ripple of $\Delta V = 50\text{ mV}$. Considering $C_{INT} \gg C_{FILT}$, the C_{INT} DC voltage drop $V_{C_{INT}}$ is about $5\text{ V} - V_r + 25\text{ mV} = 4.125\text{ V}$. C_{INT} assures an AC path for the output voltage ripple. Then the COMP pin ripple is a replica of the output ripple, with a DC value of $V_r + 25\text{ mV} = 925\text{ mV}$.

For more details about the output ripple compensation network, see the [Section 7.13.6: Closing the integrator loop on page 37](#) in the Design guidelines.

In steady state the FB pin voltage is about V_r and the regulated output voltage depends on the external divider:

Equation 4

$$OUT = V_r \times \left(1 + \frac{R_2}{R_1}\right)$$

7.4 Pulse skip mode

If the SKIP pin is tied to ground, the device works in skip mode.

At light loads a zero-crossing comparator truncates the low-side switch on-time when the inductor current becomes negative. In this condition the section works in discontinuous conduction mode. The threshold between continuous and discontinuous conduction mode is:

Equation 5

$$I_{LOAD(SKIP)} = \frac{V_{IN} - V_{OUT}}{2 \times L} \times T_{ON}$$

For higher loads the inductor current doesn't cross the zero and the device works in the same way as in PWM mode and the frequency is fixed to the nominal value.

Figure 31. PWM and pulse skip mode inductor current

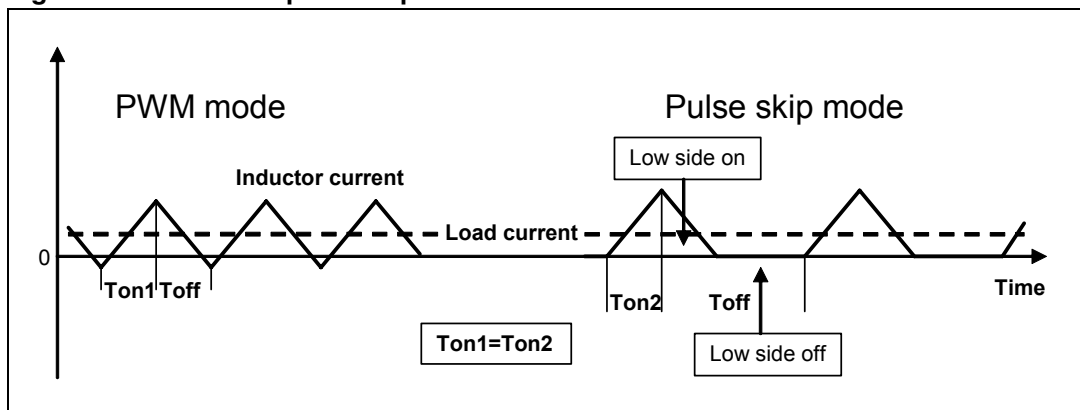


Figure 31 shows inductor current waveforms in PWM and SKIP mode. In order to keep average inductor current equal to load current, in SKIP mode some switching cycles are skipped. When the output ripple reaches the regulated voltage V_{reg} , a new cycle begins. The off cycle duration and the switching frequency depend on the load condition.

As a result of the control technique, losses are reduced at light loads, improving the system efficiency.

7.5 No-audible skip mode

If SKIP pin is tied to V_{REF} , a no-audible skip mode with a minimum switching frequency of 33 kHz is enabled. At light load condition, if there is not a new switching cycle within a 30 μ s (typ.) period, a no-audible skip mode cycle begins.