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PM6681A

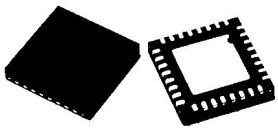
Dual synchronous step-down controller with adjustable LDO

Features

- 6 V to 36 V input voltage range
- Adjustable output voltages
- 0.9 - 3.3 V LDO adjustable delivers 100 mA peak current
- 5 V LDO delivers 100 mA peak current
- 1.237 V ±1 % reference voltage available
- No R_{SENSE} current sensing using low side MOSFETs' $R_{DS(on)}$
- Negative current limit
- Soft-start internally fixed at 2 ms
- Soft output discharge
- Latched UVP
- Not-latched OVP
- Selectable pulse skipping at light loads
- Selectable minimum frequency (33 kHz) in pulse skip mode
- 5 mW maximum quiescent power
- Independent Power Good signals
- Output voltage ripple compensation

Applications

- Embedded computer system
- FPGA system power
- Industrial applications on 24 V
- High performance and high density DC-DC modules
- Notebook computer



VFQFPN-32 (5 mm x 5 mm)

Description

PM6681A is a dual step-down controller specifically designed to provide extremely high efficiency conversion, with lossless current sensing technique. The constant on-time architecture assures fast load transient response and the embedded voltage feed-forward provides nearly constant switching frequency operation. An embedded integrator control loop compensates the DC voltage error due to the output ripple. Pulse skipping technique increases efficiency at very light load. Moreover a minimum switching frequency of 33 kHz is selectable to avoid audio noise issues. The PM6681A provides a selectable switching frequency, allowing three different values of switching frequencies for the two switching sections. The output voltages OUT1 and OUT2 can be adjusted from 0.9 V to 5 V and from 0.9 V to 3.3 V respectively. The device provides also 2 LDOs, 5 V fixed and 0.9 V - 3.3 V adjustable.

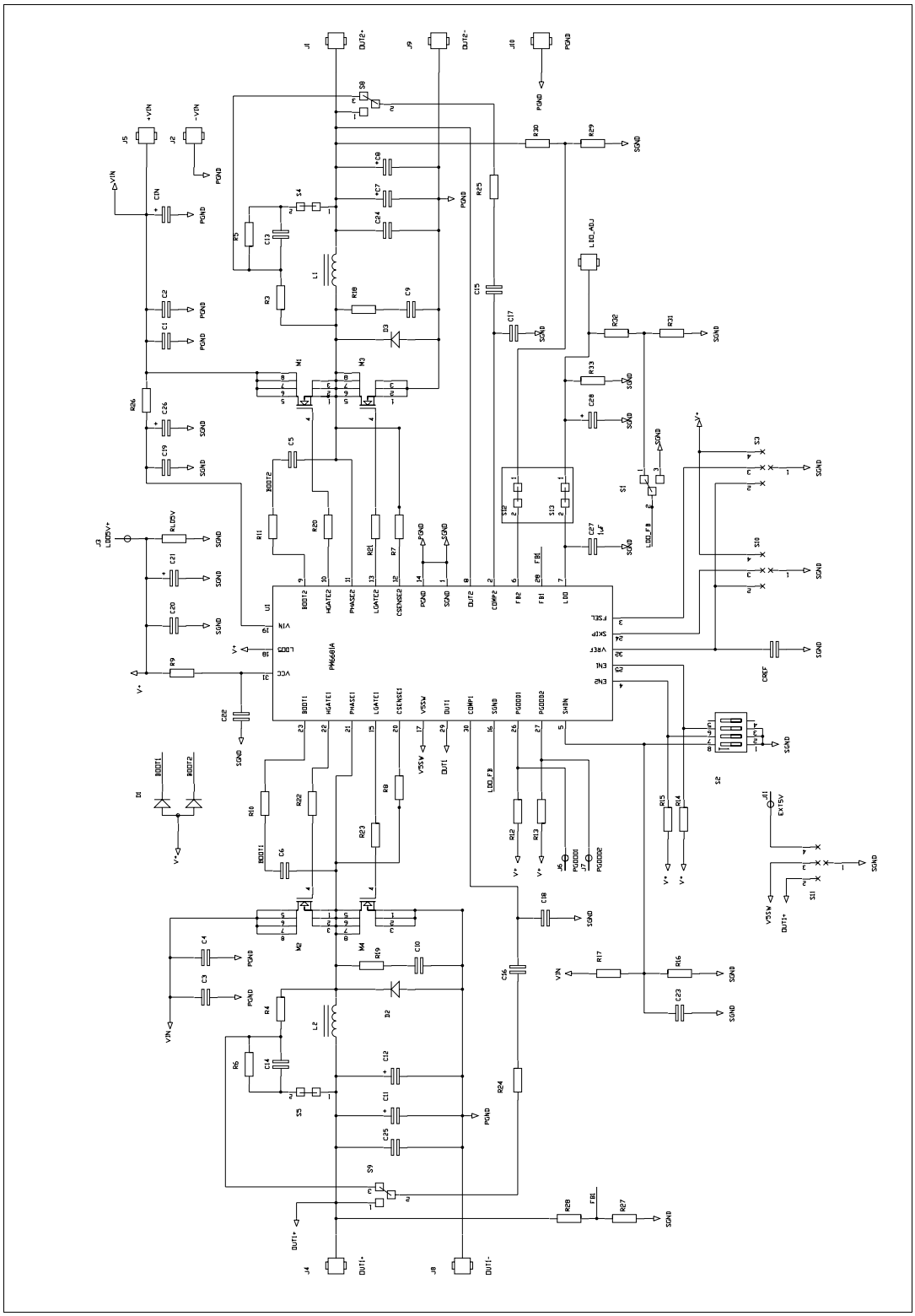
Table 1. Order codes

Order codes	Package	Packaging
PM6681A	VFQFPN-32 (5 mm x 5 mm) exposed pad	Tray
PM6681ATR		Tape and reel

Contents

1 Simplified application schematic

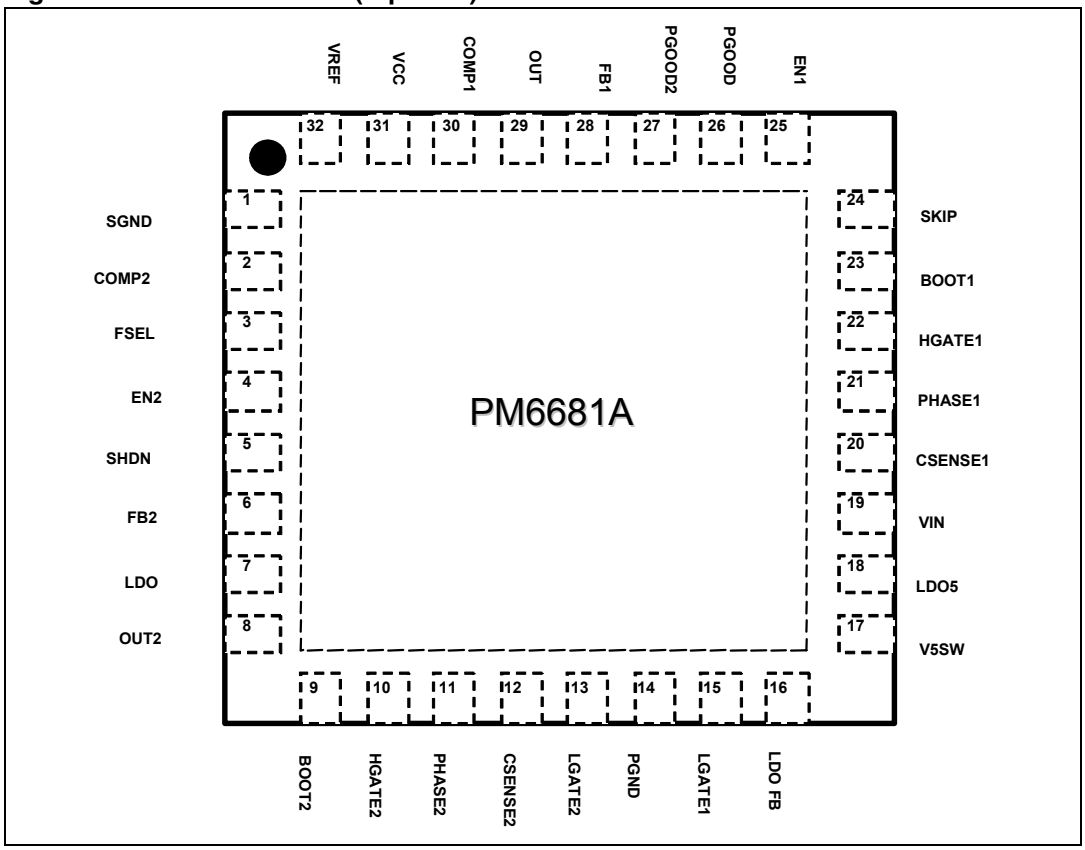
Figure 1. Application schematic



2 Pin settings

2.1 Connections

Figure 2. Pin connection (top view)



2.2 Functions

Table 2. Pin functions

N°	Pin	Function
1	SGND	Signal ground. Reference for internal logic circuitry. It must be connected to the signal ground plan of the power supply. The signal ground plan and the power ground plan must be connected together in one point near the PGND pin.
2	COMP2	DC voltage error compensation pin for the switching section 2
3	FSEL	Frequency selection pin. It provides a selectable switching frequency, allowing three different values of switching frequencies for the switching sections.

Table 2. Pin functions (continued)

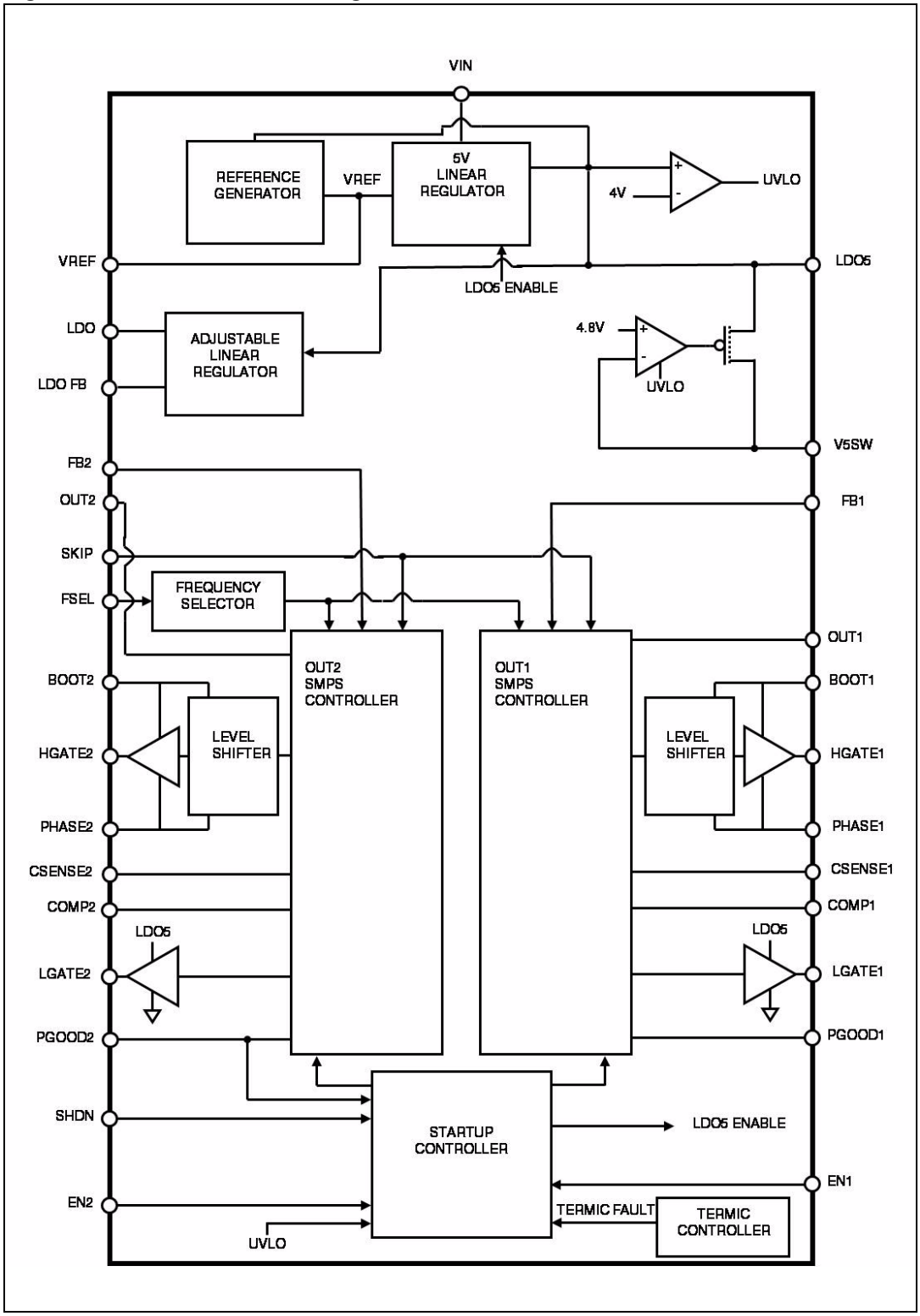
N°	Pin	Function
4	EN2	Enable input for the switching section 2. – The section 2 is enabled applying a voltage greater than 2.4 V to this pin. – The section 2 is disabled applying a voltage lower than 0.8 V. When the section is disabled the high side gate driver goes low and Low Side gate driver goes high. If both EN1 and EN2 pins are low and SHDN pin is high the device enters in standby mode.
5	SHDN	Shutdown control input. – The device switch off if the SHDN voltage is lower than the device off threshold (shutdown mode) – The device switch on if the SHDN voltage is greater than the device on threshold. The SHDN pin can be connected to the battery through a voltage divider to program an undervoltage lockout. In shutdown mode, the gate drivers of the two switching sections are in high impedance (high-Z).
6	FB2	Feedback input for the switching section 2 This pin is connected to a resistive voltage-divider from OUT2 to PGND to adjust the output voltage from 0.9 V to 3.3 V.
7	LDO	Adjustable internal regulator output. It can be set from 0.9 V to 3.3 V. LDO pin can provide a 100 mA peak current.
8	OUT2	Output voltage sense for the switching section 2. This pin must be directly connected to the output voltage of the switching section.
9	BOOT2	Bootstrap capacitor connection for the switching section 2. It supplies the high-side gate driver.
10	HGATE2	High-side gate driver output for section 2. This is the floating gate driver output.
11	PHASE2	Switch node connection and return path for the high side driver for the section 2. It is also used as negative current sense input.
12	CSENSE2	Positive current sense input for the switching section 2. This pin must be connected through a resistor to the drain of the synchronous rectifier ($R_{DS(on)}$ sensing) to obtain a positive current limit threshold for the power supply controller.
13	LGATE2	Low-side gate driver output for the section 2.
14	PGND	Power ground. This pin must be connected to the power ground plan of the power supply.
15	LGATE1	Low-side gate driver output for the section 1.
16	LDO FB	Feedback input for the adjustable internal linear regulator. This pin is connected to a resistive voltage-divider from LDO to SGND to adjust the output voltage from 0.9 V to 3.3 V.
17	V5SW	Internal 5 V regulator bypass connection. – If V5SW is connected to OUT5 (or to an external 5 V supply) and V5SW is greater than 4.9 V, the LDO5 regulator shuts down and the LDO5 pin is directly connected to OUT5 through a 3 W (max) switch. If V5SW is connected to GND, the LDO5 linear regulator is always on if the device is not in shutdown mode.

Table 2. Pin functions (continued)

N°	Pin	Function
18	LDO5	5 V internal regulator output. It can provide up to 100 mA peak current. LDO5 pin supplies embedded low side gate drivers and an external load.
19	VIN	Device supply voltage input and battery voltage sense. A bypass filter (4 W and 4.7 µF) between the battery and this pin is recommended.
20	CSENSE1	Positive current sense input for the switching section 1. This pin must be connected through a resistor to the drain of the synchronous rectifier ($R_{DS(on)}$ sensing) to obtain a positive current limit threshold for the power supply controller.
21	PHASE1	Switch node connection and return path for the high side driver for the section 1. It is also used as negative current sense input.
22	HGATE1	High-side gate driver output for section 1. This is the floating gate driver output.
23	BOOT1	Bootstrap capacitor connection for the switching section 1. It supplies the high-side gate driver.
24	SKIP	Pulse skipping mode control input. – If the pin is connected to LDO5 the PWM mode is enabled. – If the pin is connected to GND, the pulse skip mode is enabled. – If the pin is connected to VREF the pulse skip mode is enabled but the switching frequency is kept higher than 33 kHz (No-audible pulse skip mode).
25	EN1	Enable input for the switching section 1. – The section 1 is enabled applying a voltage greater than 2.4 V to this pin. – The section 1 is disabled applying a voltage lower than 0.8 V. when the section is disabled the high side gate driver goes low and low side gate driver goes high.
26	PGOOD1	Power Good output signal for the section 1. This pin is an open drain output and when the output of the switching section 1 is out of +/- 10 % of its nominal value.It is pulled down.
27	PGOOD2	Power Good output signal for the section 2. This pin is an open drain output and when the output of the switching section 2 is out of +/- 10 % of its nominal value.It is pulled down.
28	FB1	Feedback input for the switching section 1. This pin is connected to a resistive voltage-divider from OUT1 to PGND to adjust the output voltage from 0.9 V to 5.5 V.
29	OUT1	Output voltage sense for the switching section 1.This pin must be directly connected to the output voltage of the switching section.
30	COMP1	DC voltage error compensation pin for the switching section 1.
31	VCC	Device supply voltage pin. It supplies all the internal analog circuitry except the gate drivers (see LDO5). Connect this pin to LDO5.
32	VREF	Internal 1.237 V high accuracy voltage reference. It can deliver 50 µA. Bypass to SGND with a 100 nF capacitor to reduce noise.

3 Functional block diagram

Figure 3. Functional block diagram



4 Maximum ratings

Table 3. Absolute maximum ratings

Parameter		Value	Unit
V5SW, LDO5 to PGND		-0.3 to 6	V
VIN to PGND		-0.3 to 36	V
HGATEx and BOOTx, to PHASEx		-0.3 to 6	V
PHASEx to PGND		-0.6 (1) to36	V
CSENSEx, to PGND		-0.6 to 42	V
CSENSEx to BOOTx		-6 to 0.3	V
LGATEx to PGND		-0.3 (2) to LDO5 +0.3	V
FBx, COMPx, SKIP, FSEL,VREF to SGND, LDO FB		-0.3 to Vcc+0.3	V
PGND to SGND		-0.3 to 0.3	V
SHDN, PGOODx, OUTx, VCC, ENx to SGND		-0.3 to 6	V
Power dissipation at T_A = 25 °C		2.8	W
Maximum withstanding voltage range test condition: CDF-AEC-Q100-002- “human body model” acceptance criteria: “normal performance”	VIN	±1000	V
	Other pins	±2000	

1. PHASE to PGND up to -2.5 V for t < 10 ns
2. LGATEx to PGND up to -1 V for t < 40 ns

Table 4. Thermal data

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature range	-50 to 150	°C
R_{thJA}	Thermal resistance junction to ambient	35	°C/W
T_J	Junction operating temperature range	-40 to 125	°C
T_A	Operating ambient temperature range	-40 to 85	°C

Table 5. Recommended operating conditions

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
VIN	Input voltage range	LDO5 in regulation	5.5		36	V
VCC	IC supply voltage		4.5		5.5	V
V_{V5SW}	V_{V5SW} maximum operating range				5.5	V

5 Electrical characteristics

Table 6. Electrical characteristics (V_{IN} = 24 V; T_J = 25 °C, unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Supply section						
V_{V5SW}	Turn-on voltage threshold			4.8	4.9	V
	Turn-off voltage threshold		4.6	4.75		V
	Hysteresis		20	50		mV
$R_{DS(on)}$	LDO5 internal bootstrap switch resistance	V5SW > 4.9 V		1.8	3	Ω
	OUTx, OUTx discharge-mode On-resistance			18	25	Ω
	OUTx, OUTx discharge-mode Synchronous rectifier turn-on level		0.2	0.35	0.6	V
Pin	Operating power consumption	FBx > VREF, Vref in regulation, V5WS to 5 V			4	mW
Ish	Operating current sunk by V_{IN}	SHDN connected to GND		20	30	µA
Isb	Operating current sunk by V_{IN}	ENx to GND, V5SW to GND		250	380	µA
Shutdown section						
V_{SHDN}	Device on threshold		1.2	1.5	1.7	V
	Device off threshold		0.8	0.85	0.9	V
soft-start section						
	soft-start ramp time		2		3.5	ms
Current limit and zero crossing comparator						
I_{CSENSE}	Input bias current limit (1)		90	100	110	µA
	Comparator offset	V_{CSENSE} - V_{PGND}	-6		6	mV
	Zero crossing comparator offset	V_{PGND} - V_{PHASE}	-1		11	mV
	Fixed negative current limit threshold	V_{PGND} - V_{PHASE}		-120		mV

Table 6. Electrical characteristics (V_{IN} = 24 V; T_J = 25 °C, unless otherwise specified) (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
On time pulse width						
Ton	On time duration_ @VIN = 24 V	FSEL to GND OUT1 = 3.3 V OUT2 = 1.8 V	575	680	785	ns
			195	230	265	
		FSEL to VREF OUT1 = 3.3 V OUT2 = 1.8 V	390	460	530	
			145	175	205	
		FSEL to LDO5 OUT1 = 3.3 V OUT2 =1.8 V	285	340	395	
			110	135	160	
OFF time						
T_{OFFMIN}	Minimum off time @VIN = 24 V			350	500	ns
Voltage reference						
V_{REF}	Voltage accuracy	4 V < V_{LDO5} < 5.5 V	1.224	1.236	1.249	V
	Load regulation	-100 µA< I_{REF} < 100 µA	-4		4	mV
	Undervoltage lockout fault threshold	Falling edge of REF			0.95	mV
Integrator						
FB	Voltage accuracy		+891		+909	mV
FB	Input bias current	(1)		0.1		µA
COMP	Over voltage clamp	Normal mode		250		mV
COMP	Under voltage clamp			-150		
Line regulation						
		Both SMPS, 6 V < Vin < 36 V (1)			1	%
LDO5 linear regulator						
V_{LDO5}	LDO5 linear output voltage	6 V < VIN < 36 V, 0 < I_{LDO5} < 50 mA	4.9	5.0	5.1	V
	LDO5 line regulation	6 V < VIN < 36 V, I_{LDO5} = 20 mA ,			0.004	%/V
I_{LDO5}	LDO5 current limit	V_{LDO5} > UVLO	270	330	400	mA
ULVO	Under voltage lockout of LDO5		3.94	4	4.13	V
LDO linear regulator						
V_{LDO}	LDO linear output voltage	4.5 V< V5SW < 5.5 V 0.5 mA < I_{LDO} < 50 mA LDO FB connected to LDO	0.887	0.905	0.923	V

Table 6. Electrical characteristics (V_{IN} = 24 V; T_J = 25 °C, unless otherwise specified) (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{LDO}	LDO current limit		170	220	270	mA
$I_{LDO\ FB}$	Input bias current	(1)		0.1		µA
High and low gate drivers						
	HGATE driver on-resistance	HGATEx high state (pull-up)		2.0	3	Ω
		HGATEx low state (pull-down)		1.6	2.7	
	LGATE driver on-resistance	LGATEx high state (pull-up)		1.4	2.1	
		LGATEx low state (pull-down)		0.8	1.2	
PGOOD pins UVP/OVP protections						
OVP	Over voltage threshold	Both SMPS sections with respect to VREF, OUT1 = 5 V, OUT2 = 3.3 V	112	116	120	%
UVP	Under voltage threshold		65	68	71	%
PGOOD1,2	Upper threshold (VFB-VREF)		107	110	113	%
	Lower threshold (VFB-VREF)		88	91	94	%
$I_{PGOOD1,2}$	PGOOD leakage current	$V_{PGOOD1,2}$ forced to 5.5 V			1	uA
$V_{PGOOD1,2}$	output low voltage	I_{Sink} = 4 mA		150	250	mV
Power management pins						
EN1,2	SMPS disabled level	(1)			0.8	V
	SMPS enabled level	(1)	2.4			
FSEL	Frequency selection range	Low level (1)			0.5	V
		Middle level (1)	1.0		V_{LDO5} - 1.5	
		High level (1)	V_{LDO5} - 0.8			
SKIP	Pulse skip mode	(1)			0.5	V
	Ultrasonic mode	(1)	1.0		V_{LDO5} - 1.5	
	PWM mode	(1)	V_{LDO5} - 0.8			
	Input leakage current	$V_{EN1,2}$ = 0 to 5 V			1	µA
		V_{SKIP} = 0 to 5 V			1	
		V_{SHDN} = 0 to 5 V			1	
		V_{FSEL} = 0 to 5 V			1	

1. by design

6 Typical operating characteristics

(FSEL = GND (200/300 kHz), SKIP = GND (skip mode), V5SW = EXT5 V (external 5 V power supply connected), input voltage VIN = 24 V, SHDN, EN1 and EN2 high, OUT1 = 3.3 V, OUT2 = 1.8 V, no load, LDO = 3.3 V, (LDO_FB divider = 5.6 k and 15 k) unless specified)

Figure 4. Efficiency vs current load

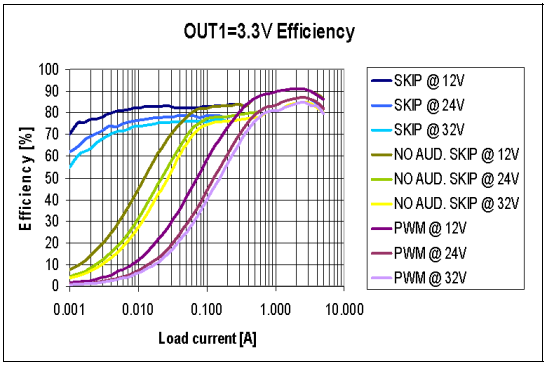


Figure 5. Efficiency vs current load

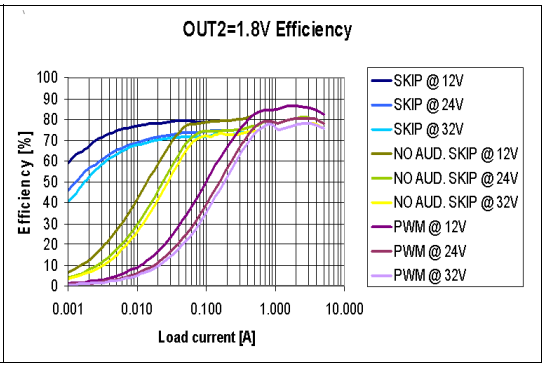


Figure 6. PWM no load battery current vs input voltage

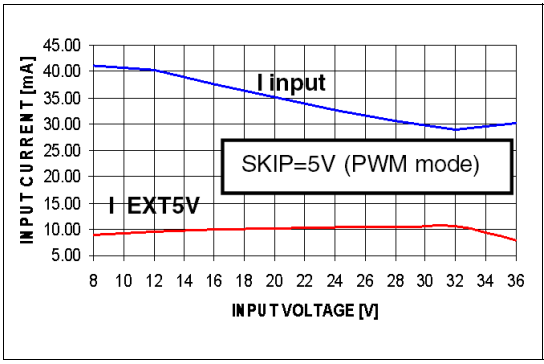


Figure 7. No-audible skip no load battery current vs input voltage

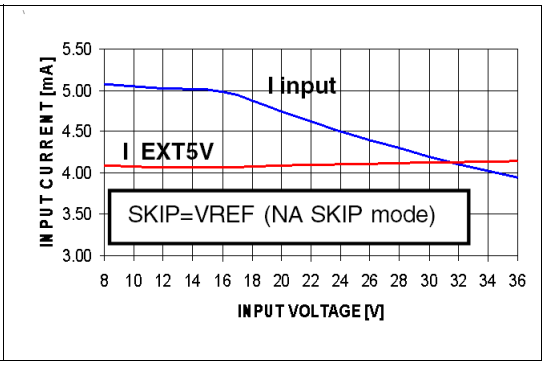


Figure 8. Skip no load battery current vs input voltage

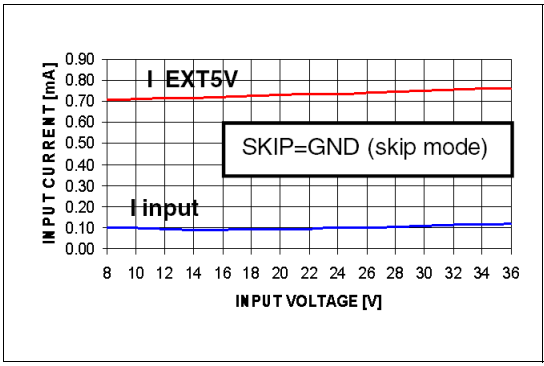


Figure 9. Shutdown mode input battery current vs input voltage

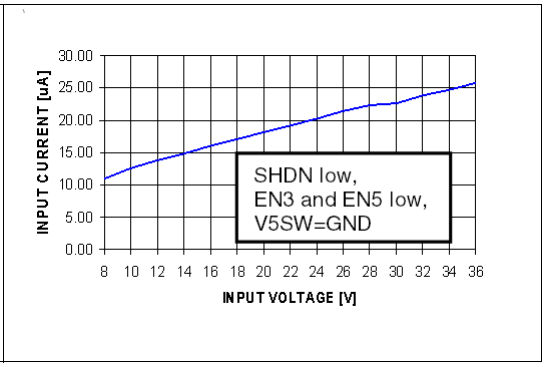


Figure 10. Standby mode input battery current vs input voltage

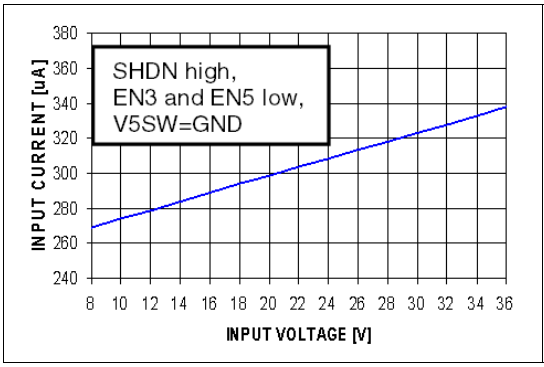


Figure 11. Voltage reference vs load current

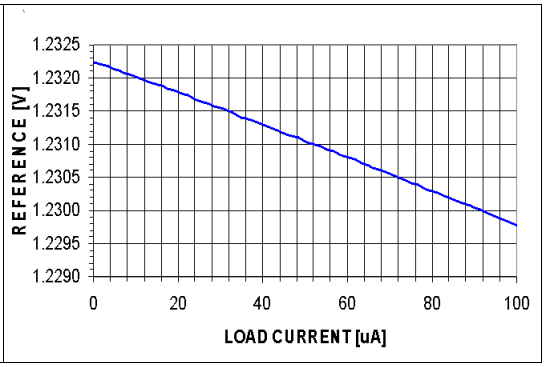


Figure 12. OUT1 = 3.3 V switching frequency

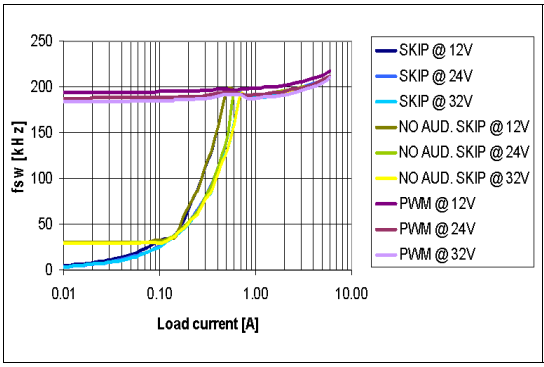


Figure 13. OUT2 = 1.8 V switching frequency

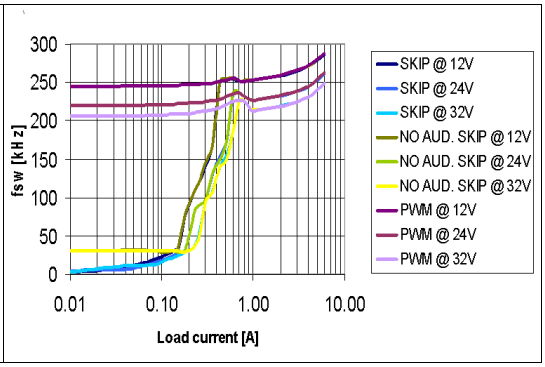


Figure 14. OUT1 = 3.3 V load regulation

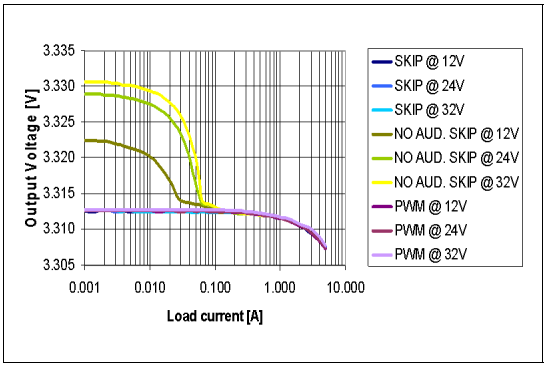


Figure 15. OUT2 = 1.8 V load regulation

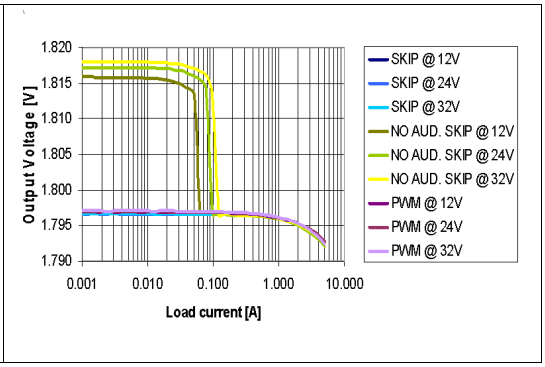


Figure 16. LDO5 vs output current

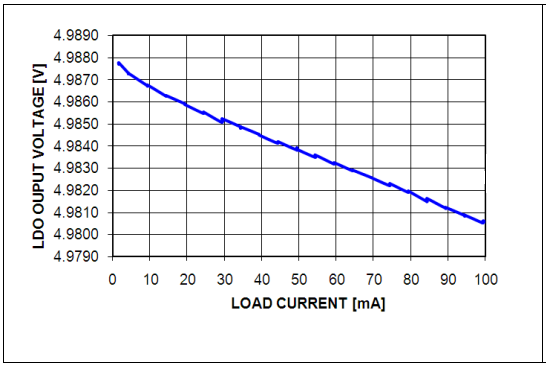


Figure 17. LDO vs output current

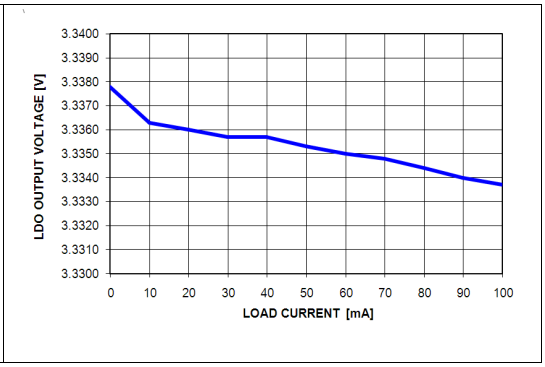


Figure 18. SHDN, OUT1, LDO and LDO5 power-up

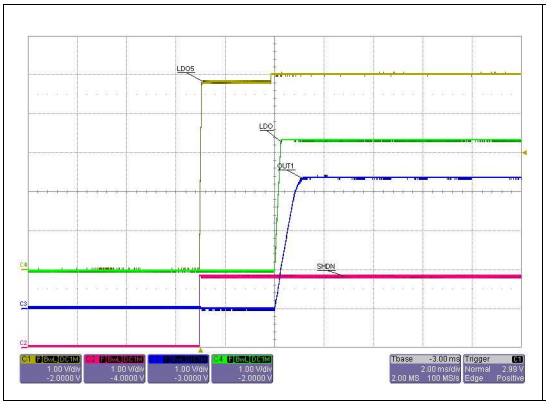


Figure 19. OUT1, OUT2, LDO and LDO5 power-up

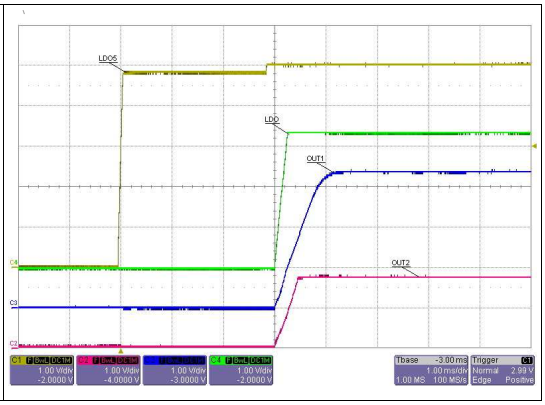


Figure 20. OUT1 = 3.3 V load transient 0 to 2 A

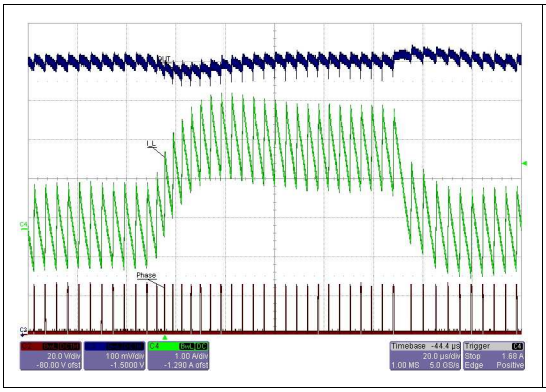


Figure 21. OUT2 = 1.8 V load transient 0 to 2 A

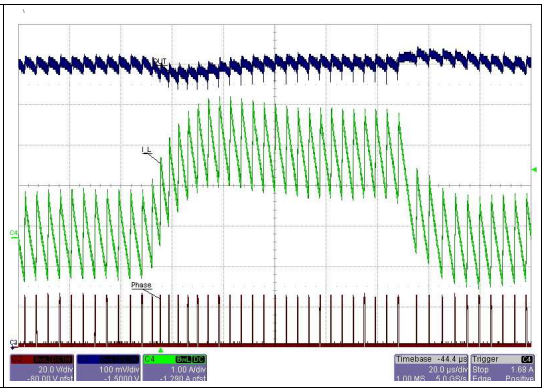


Figure 22. 3.3 V soft-start (1 Ω load)

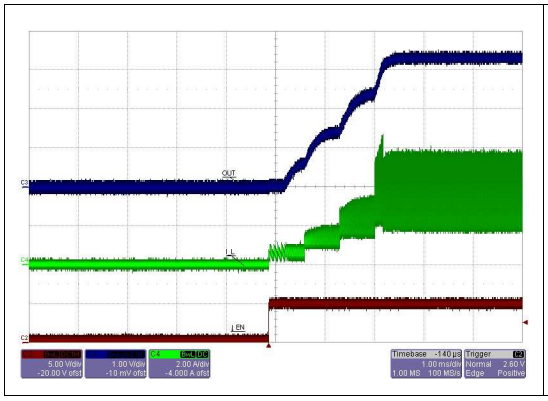


Figure 23. 1.8 V soft-start (0.6 Ω load)

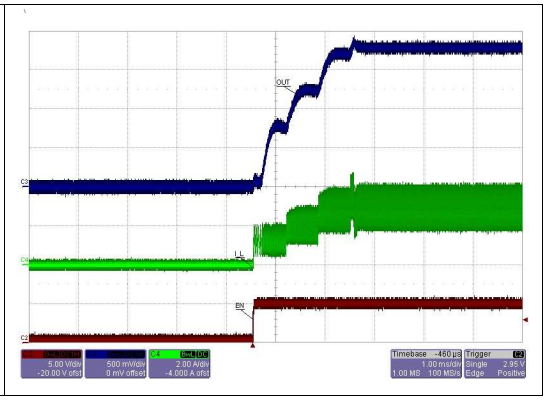


Figure 24. OUT1 = 3.3 V soft-end (no load)

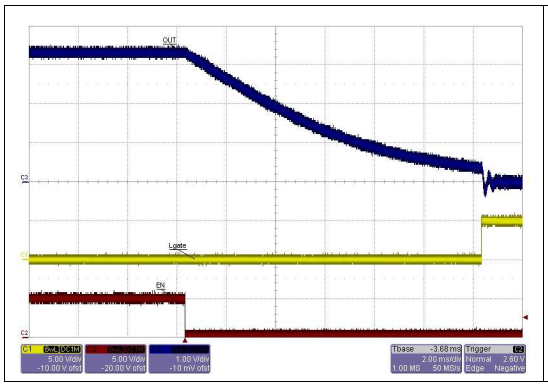


Figure 25. OUT2 = 1.8 V soft-end (no load)

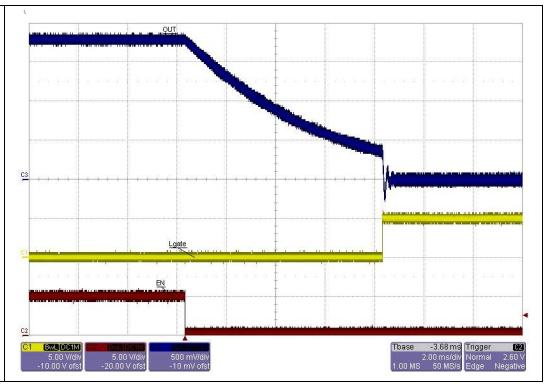


Figure 26. OUT1 = 3.3 V soft-end (0.8 Ω load)

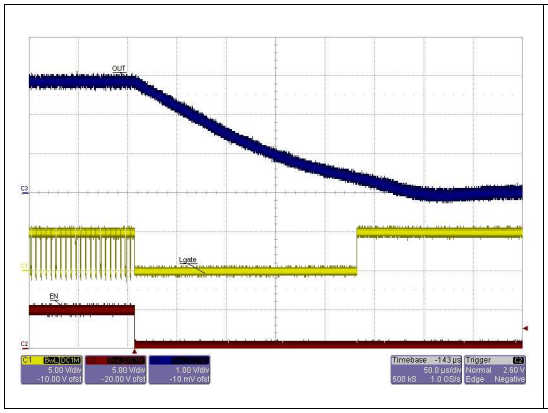


Figure 27. OUT2 = 1.8 V soft-end (0.6 Ω load)

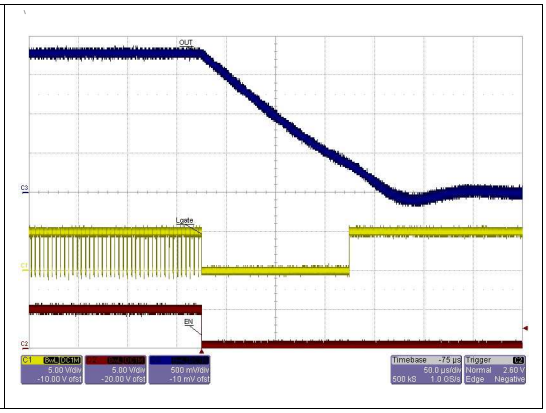


Figure 28. 3.3 V no-audible skip mode

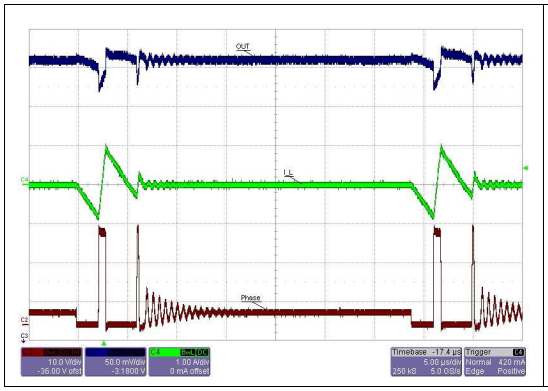
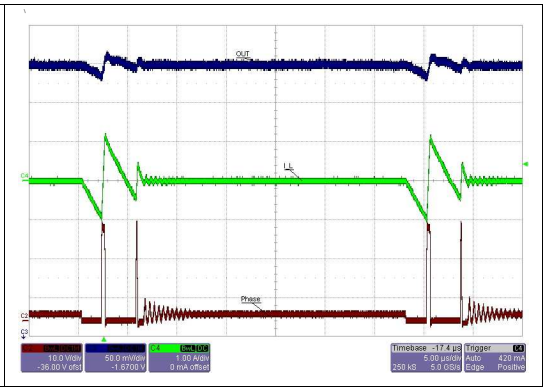


Figure 29. 1.8 V no-audible skip mode



7 Device description

The PM6681A is a dual step-down controller dedicated to provide logic voltages for industrial automation application and notebook computer.

It is based on a constant on time control architecture. This type of control offers a very fast load transient response with a minimum external component count. A typical application circuit is shown in *Figure 1*. The PM6681A regulates two adjustable output voltages: OUT1 and OUT2. The switching frequency of the two sections can be adjusted to three different values. In order to maximize the efficiency at light load condition, a pulse skipping mode can be selected. The PM6681A includes also a 5 V linear regulator (LDO5) that can power the switching drivers. If the output OUT1 regulates 5 V, in order to maximize the efficiency in higher consumption status, the linear regulator can be turned off and their outputs can be supplied directly from the switching outputs. Moreover, the PM6681A includes also a linear regulator with an output voltage adjustable from 0.9 V to 3.3 V. It can provide 100 mA of peak current. The PM6681A provides protection versus overvoltage, undervoltage and overtemperature as well as Power Good signals for monitoring purposes.

An external 1.237 V reference is available.

7.1 Constant on time PWM control

If the SKIP pin is tied to 5 V, the device works in PWM mode. Each power section has an independent on time control.The PM6681A employees a pseudo-fixed switching frequency, constant on time (COT) controller as core of the switched mode section. Each power section has an independent COT control.

The COT controller is based on a relatively simple algorithm and uses the ripple voltage due to the output capacitor's ESR to trigger the fixed on-time one-shot generator. In this way, the output capacitor's ESR acts as a current sense resistor providing the appropriate ramp signal to the PWM comparator. On-time one-shot duration is directly proportional to the output voltage, sensed at the OUT1/OUT2 pins, and inversely proportional to the input voltage, sensed at the VIN pin, as follows:

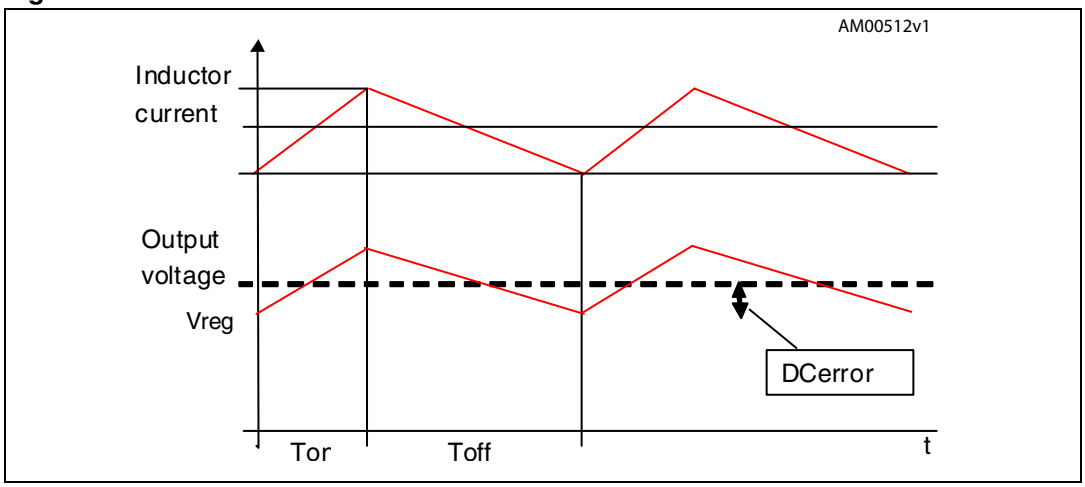
Equation 1

$$T_{on} = K \times \frac{Vout}{Vin}$$

This leads to a nearly constant switching frequency, regardless of input and output voltages.

When the output voltage goes lower than the regulated voltage Vreg, the on-time one shot generator directly drives the high side MOSFET for a fixed on time allowing the inductor current to increase; after the on time, an off time phase, in which the low side MOSFET is turned on, follows. *Figure 30* shows the inductor current and the output voltage waveforms in PWM mode.

Figure 30. Constant on time PWM control



The duty cycle of the buck converter in steady state is:

Equation 2

$$D = \frac{Vout}{Vin}$$

The PWM control works at a nearly fixed frequency f_{SW}:

Equation 3

$$f_{sw} = \frac{D}{T_{on}} = \frac{\frac{Vout}{Vin}}{K_{on} \times \frac{Vout}{Vin}} = 1/K_{on}$$

As mentioned the steady state switching frequency is theoretically independent from battery voltage and from output voltage.

Actually the frequency depends on parasitic voltage drops that are present during the charging path (high side switch resistance, inductor resistance (DCR) and discharging path (low side switch resistance, DCR).

As a result the switching frequency increases as a function of the load current.

Standard switching frequency values can be selected for both sections by connecting pin FSEL to SGND, VREF or LDO5 pin. The following table shows the typical switching frequencies that can be obtained as a function of the programmed output voltage. The measures are referred to switching sections with 2 A load, 12 V input voltage and working in continuous conduction mode.

Table 7. FSEL pin selection: typical switching frequency

	Fsw @ OUT1 = 1.5 V (kHz)	Fsw @ OUT2 = 1.05 V (kHz)
FSEL = GND	200	325
FSEL = VREF	290	425
FSEL = LDO5	390	590

7.2 Constant on time architecture

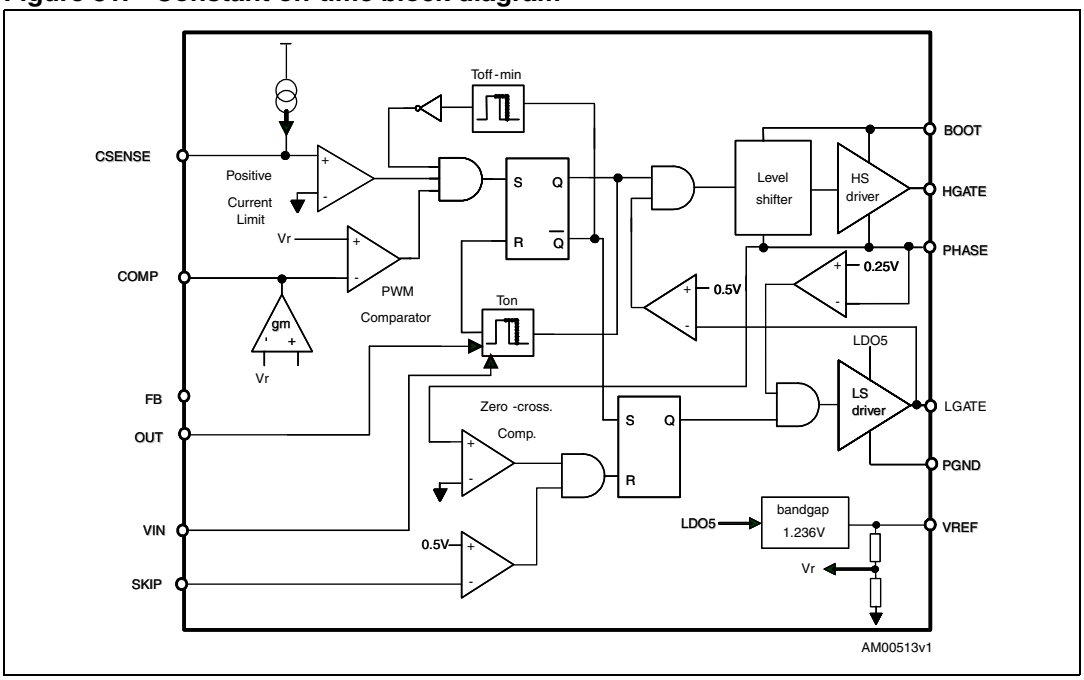
Figure 31 shows the simplified block diagram of a constant on time controller. A minimum off-time constrain (350 ns typ.) is introduced to allow inductor valley current sensing on synchronous switch. A minimum on-time (130 ns) is also introduced to assure the start-up switching sequence.

PM6681A has a one-shot generator for each power section that turns on the high side MOSFET when the following conditions are satisfied simultaneously: the PWM comparator is high, the synchronous rectifier current is below the current limit threshold, and the minimum off-time has timed out.

Once the on-time has timed out, the high side switch is turned off, while the synchronous switch is turned on according to the anti-cross conduction circuitry management.

When the negative input voltage at the PWM comparator (*Figure 31*), which is a scaled-down replica of the output voltage (see the external R1/R2 divider in *Figure 32*), reaches the valley limit (determined by internal reference Vr = 0.9 V), the low-side MOSFET is turned off according to the anti-cross conduction logic once again, and a new cycle begins.

Figure 31. Constant on-time block diagram

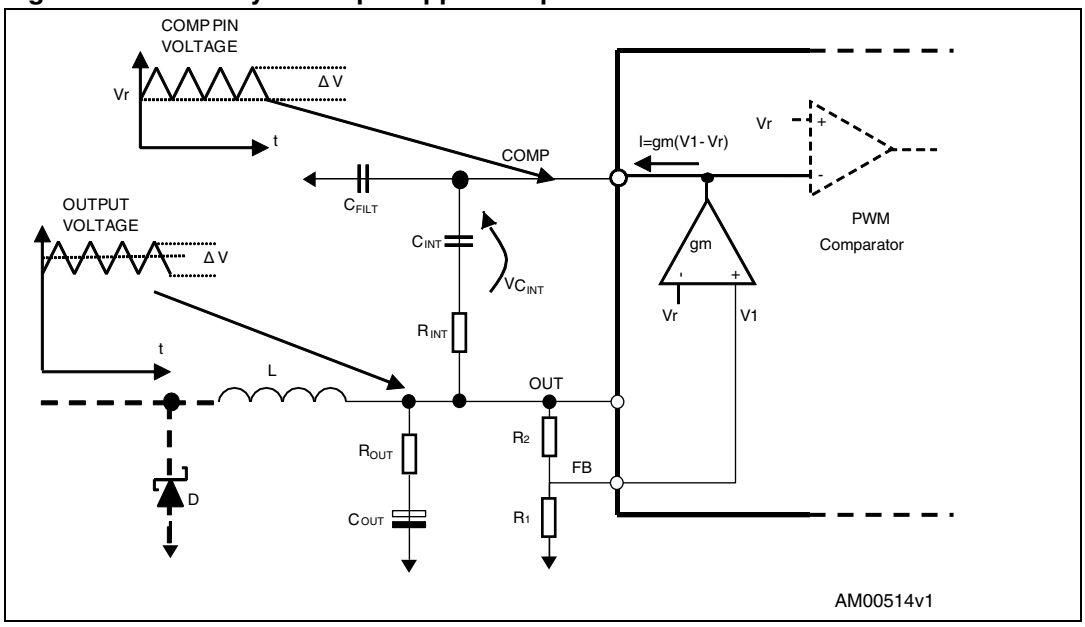


7.3 Output ripple compensation and loop stability

In a classic constant on time control, the system regulates the valley value of the output voltage and not the average value, as shown in *Figure 30*. In this condition, the output voltage ripple is source of a DC static error.

To compensate this error, an integrator network can be introduced in the control loop, by connecting the output voltage to the COMP1/COMP2 (for the OUT1 and OUT2 sections respectively) pin through a capacitor CINT as in *Figure 32*.

Figure 32. Circuitry for output ripple compensation



The integrator amplifier generates a current, proportional to the DC errors between the FB voltage and Vr, which decreases the output voltage in order to compensate the total static error, including the voltage drop on PCB traces. In addition, CINT provides an AC path for the output ripple. In steady state, the voltage on COMP1/COMP2 pin is the sum of the reference voltage Vr and the output ripple (see *Figure 32*). In fact when the voltage on the COMP pin reaches Vr, a fixed Ton begins and the output increases.

For example, we consider Vout = 5 V with an output ripple of ΔV = 50 mV. Considering C_{INT} >> C_{FILT}, the C_{INT} DC voltage drop V_{CINT} is about 5 V - Vr + 25 mV = 4.125 V. C_{INT} assures an AC path for the output voltage ripple. Then the COMP pin ripple is a replica of the output ripple, with a DC value of Vr + 25 mV = 925 mV.

For more details about the output ripple compensation network, see the paragraph “Closing the integrator loop” in the design guidelines.

In steady state the FB pin voltage is about Vr and the regulated output voltage depends on the external divider:

Equation 4

$$OUT = Vr \times \left(1 + \frac{R_2}{R_1}\right)$$

7.4 Pulse skip mode

If the SKIP pin is tied to ground, the device works in skip mode.

At light loads a zero-crossing comparator truncates the low-side switch on-time when the inductor current becomes negative. In this condition the section works in discontinuous conduction mode. The threshold between continuous and discontinuous conduction mode is:

Equation 5

$$ILOAD(SKIP) = \frac{V_{IN} - V_{OUT}}{2 \times L} \times T_{ON}$$

For higher loads the inductor current doesn't cross the zero and the device works in the same way as in PWM mode and the frequency is fixed to the nominal value.

Figure 33. PWM and pulse skip mode inductor current

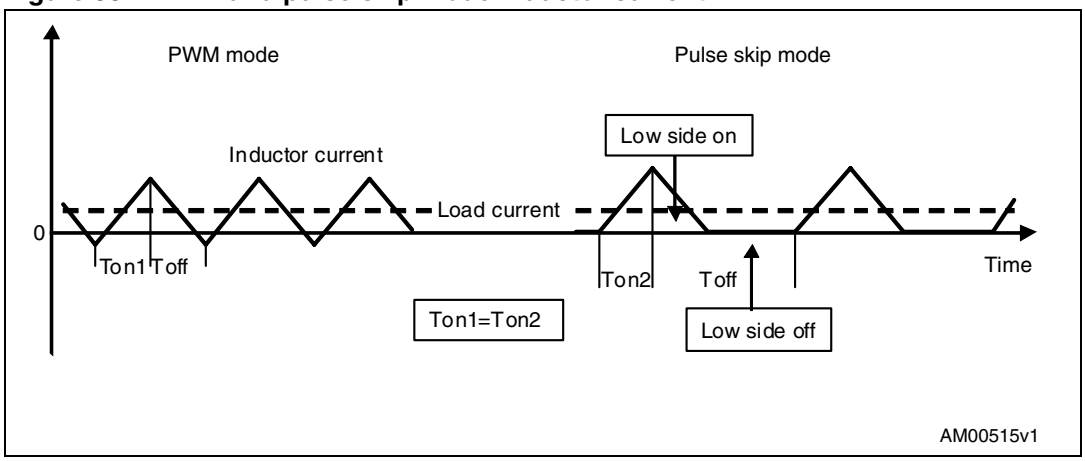


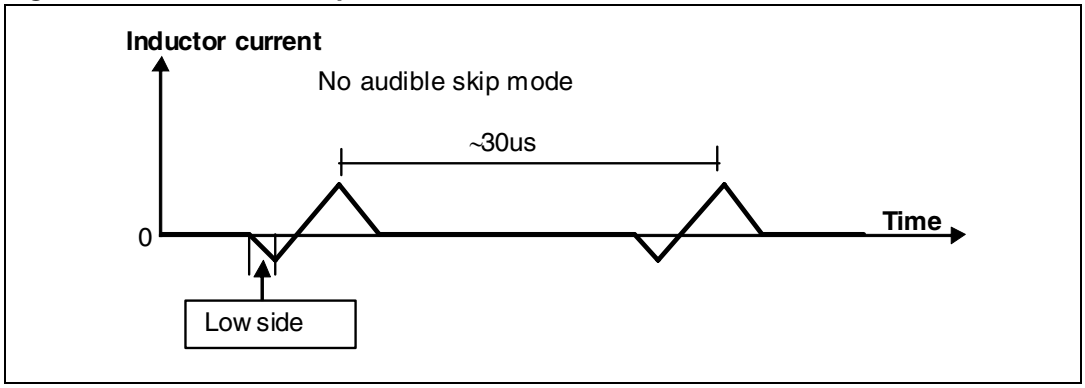
Figure 33 shows inductor current waveforms in PWM and SKIP mode. In order to keep average inductor current equal to load current, in SKIP mode some switching cycles are skipped. When the output ripple reaches the regulated voltage Vreg, a new cycle begins. The off cycle duration and the switching frequency depend on the load condition.

As a result of the control technique, losses are reduced at light loads, improving the system efficiency.

7.5 No-audible skip mode

If SKIP pin is tied to VREF, a no-audible skip mode with a minimum switching frequency of 33 kHz is enabled. At light load condition, If there is not a new switching cycle within a 30 µs (typ.) period, a no-audible skip mode cycle begins.

Figure 34. No audible skip mode



The low side switch is turned on until the output voltage crosses about Vreg+1 %. Then the high side MOSFET is turned on for a fixed on time period. Afterwards the low side switch is enabled until the inductor current reaches the zero-crossing threshold. This keeps the switching frequency higher than 33 kHz. As a consequence of the control, the regulated voltage can be slightly higher than Vreg (up to 1 %).

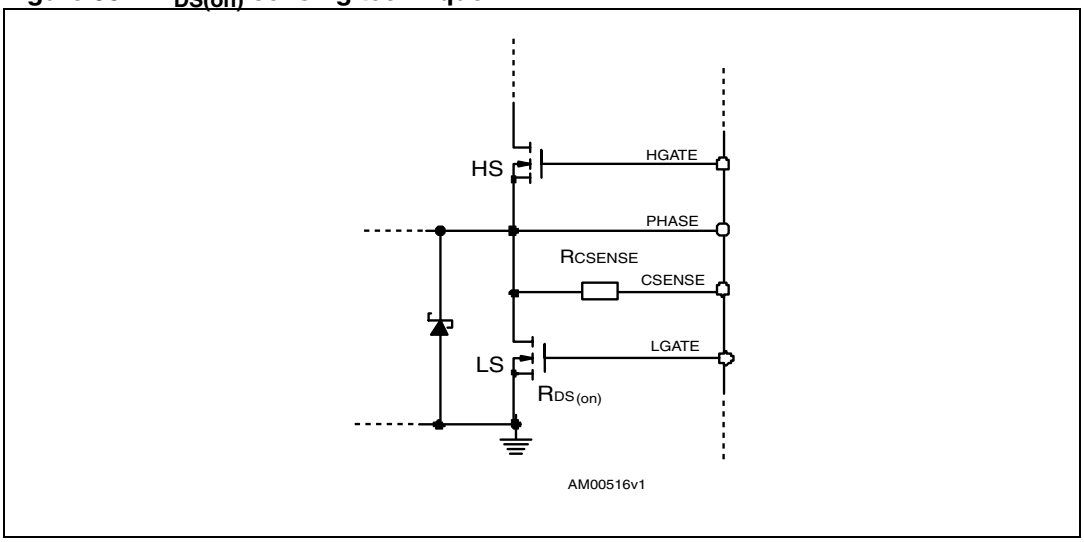
If, due to the load, the frequency is higher than 33 kHz, the device works like in skip mode.

No-audible skip mode reduces audio frequency noise that may occur in pulse skip mode at very light loads, keeping the efficiency higher than in PWM mode.

7.6 Current limit

The current-limit circuit employs a “valley” current-sensing algorithm. During the conduction time of the low side MOSFET the current flowing through it is sensed. The current-sensing element is the low side MOSFET on-resistance (*Figure 35*).

Figure 35. $R_{DS(on)}$ sensing technique



An internal 100 µA current source is connected to CSENSE pin and determines a voltage drop on R_{CSENSE}. If the voltage across the sensing element is greater than this voltage drop, the controller doesn't initiate a new cycle. A new cycle starts only when the sensed current goes below the current limit.

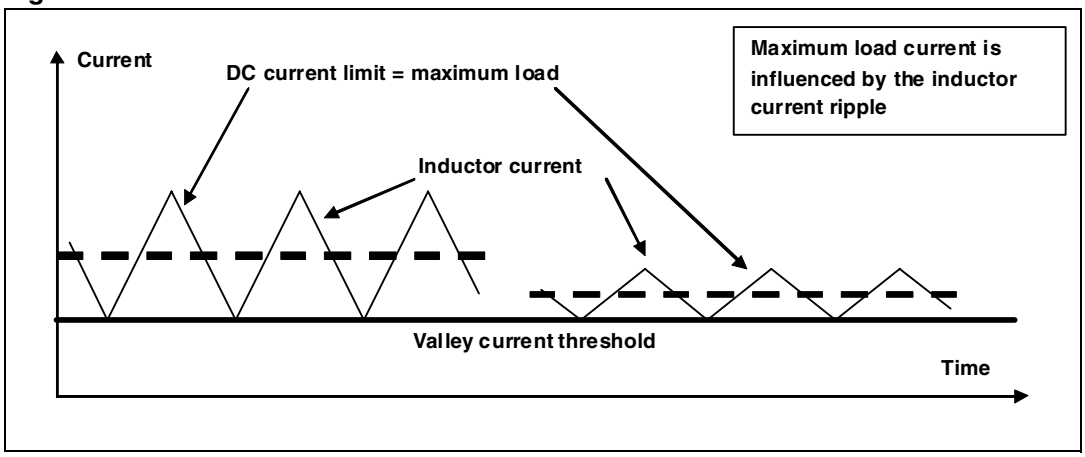
Since the current limit circuit is a valley current limit, the actual peak current limit is greater than the current limit threshold by an amount equal to the inductor ripple current. Moreover the maximum output current is equal to the valley current limit plus half of the inductor ripple current:

Equation 6

$$I_{LOAD}(max) = I_{Lvalley} + \frac{\Delta I_L}{2}$$

The output current limit depends on the current ripple, as shown in *Figure 36*:

Figure 36. Current waveforms in current limit conditions



Being fixed the valley threshold, the greater the current ripple is, greater the DC output current is:

The valley current limit can be set with resistor R_{CSENSE}:

Equation 7 **($R_{DS(on)}$ sensing technique)**

$$R_{CSENSE} = \frac{R_{DSon} \times I_{Lvalley}}{I_{CSENSE}}$$

Where I_{CSENSE} = 100 µA, $R_{DS(on)}$ is the drain-source on resistance of the low side switch. Consider the temperature effect and the worst case value in $R_{DS(on)}$ calculation.

The accuracy of the valley current threshold detection depends on the offset of the internal comparator (ΔV_{OFF}) and on the accuracy of the current generator(ΔI_{CSENSE}):

Equation 8

$$\frac{\Delta I_{Lvalley}}{I_{Lvalley}} = \frac{\Delta I_{CSENSE}}{I_{CSENSE}} + \left[\frac{\Delta V_{OFF}}{R_{CSENSE} \times I_{CSENSE}} \times 100\right] + \frac{\Delta R_{CSENSE}}{R_{CSENSE}} + \frac{\Delta R_{SNS}}{R_{SNS}}$$

Where R_{SNS} is the sensing element ($R_{DS(on)}$).

PM6681A provides also a fixed negative peak current limit to prevent an excessive reverse inductor current when the switching section sinks current from the load in PWM mode. This negative current limit threshold is measured between PHASE and SGND pins, comparing the magnitude drop on the PHASE node during the conduction time of the low side MOSFET with an internal fixed voltage of 120 mV.

The negative valley-current limit INEG (if the device works in PWM mode) is given by:

Equation 9

$$I_{NEG} = \frac{120mV}{R_{DSon}}$$

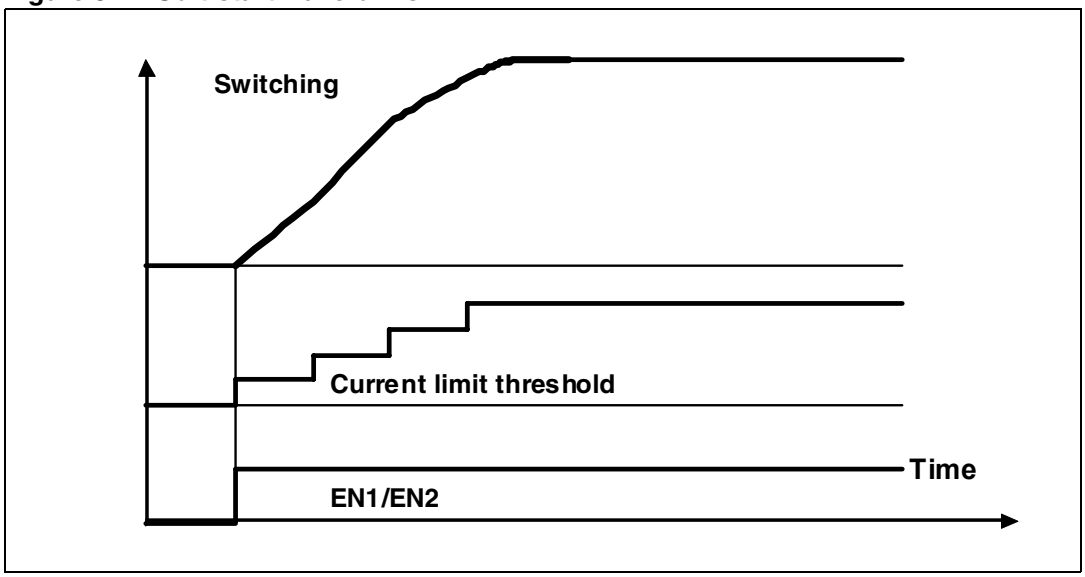
7.7 soft-start and soft-end

Each switching section is enabled separately by asserting high EN1/EN2 pins respectively. In order to realize the soft-start, at the startup the overcurrent threshold is set 25 % of the nominal value and the undervoltage protection (see related sections) is disabled. The controller starts charging the output capacitor working in current limit. The overcurrent threshold is increased from 25 % to 100 % of the nominal value with steps of 25 % every 700 µs (typ.). After 2.8 ms (typ.) the undervoltage protection is enabled. The s oft start time is not programmable. A minimum capacitor C_{INT} is required to ensure a soft-start without any overshoot on the output:

Equation 10

$$C_{INT} \geq \frac{6uA}{\frac{I_{Lvalley}}{4} + \frac{\Delta I_L}{2}} \times C_{out}$$

Figure 37. Soft-start waveforms



When a switching section is turned off (EN1/EN2 pins low), the controller enters in soft-end mode. The output capacitor is discharged through an internal 18 Ω P-MOSFET switch; when the output voltage reaches 0.3 V, the low-side MOSFET turns on, keeping the output to ground. The soft-end time also depends on load condition.

7.8 Gate drivers

The integrated high-current drivers allow to use different power MOSFETs. The high side driver MOSFET uses a bootstrap circuit which is indirectly supplied by LDO5 output. The BOOT and PHASE pins work respectively as supply and return rails for the HS driver.

The low side driver uses the internal LDO5 output for the supply rail and PGND pin as return rail.

An important feature of the gate drivers is the adaptive anti-cross conduction protection, which prevents high side and low side MOSFETs from being on at the same time. When the