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PM6685

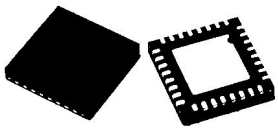
Dual step-down main supply controller with auxilary voltages for notebook system power

Features

- 6 V to 28 V input voltage range
- Fixed 5 V - 3.3 V output voltages
- 5 V and 3.3 V voltage always available to deliver 100 mA of peak current
- 1.230 V ±1% reference voltage available
- Lossless current sensing using low side
- MOSFETs' $R_{DS(on)}$
- Negative current limit
- Soft-start internally fixed at 2 ms
- Soft output discharge
- Latched OVP and UVP
- Selectable pulse skipping at light loads
- Selectable minimum frequency (33 kHz) in pulse skip mode
- 4 mW maximum quiescent power
- Independent power good signals
- Output voltage ripple compensation

Applications

- Notebook computers
- Tablet PC or slates
- Mobile system power supply
- 3 and -4 Cells Li+ battery-powered devices



VFQFPN-32 (5mm x 5mm)

Description

PM6685 is a dual step-down controller specifically designed to provide extremely high efficiency conversion with loss-less current sensing technique. The constant on-time architecture assures fast load transient response and the embedded voltage feed-forward provides nearly constant switching frequency operation.

An embedded integrator control loop compensates the DC voltage error due to the output ripple. The pulse skipping technique increases efficiency for very light loads. Moreover, a minimum switching frequency of 33kHz is selectable in order to avoid audio noise issues.

The PM6685 provides a selectable switching frequency, allowing either 200 kHz/300 kHz, 300 kHz/400 kHz, or 400 kHz/500 kHz operation of the 5 V/3.3 V switching sections.

Table 1. Device summary

Order code	Package	Packaging
PM6685	VFQFPN-32 (5 mm x 5 mm)	Tube
PM6685TR		Tape and reel

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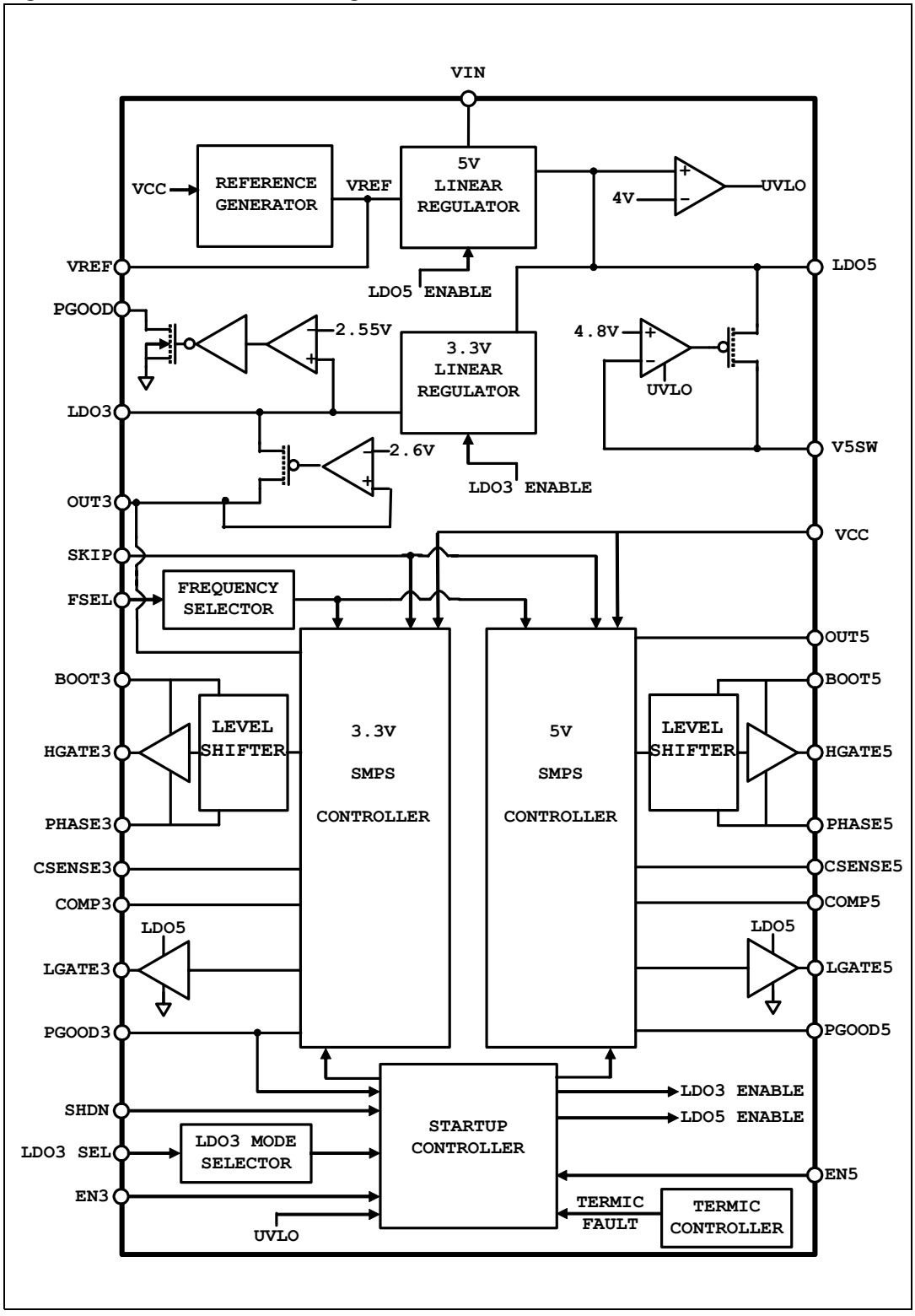
1 Block diagram

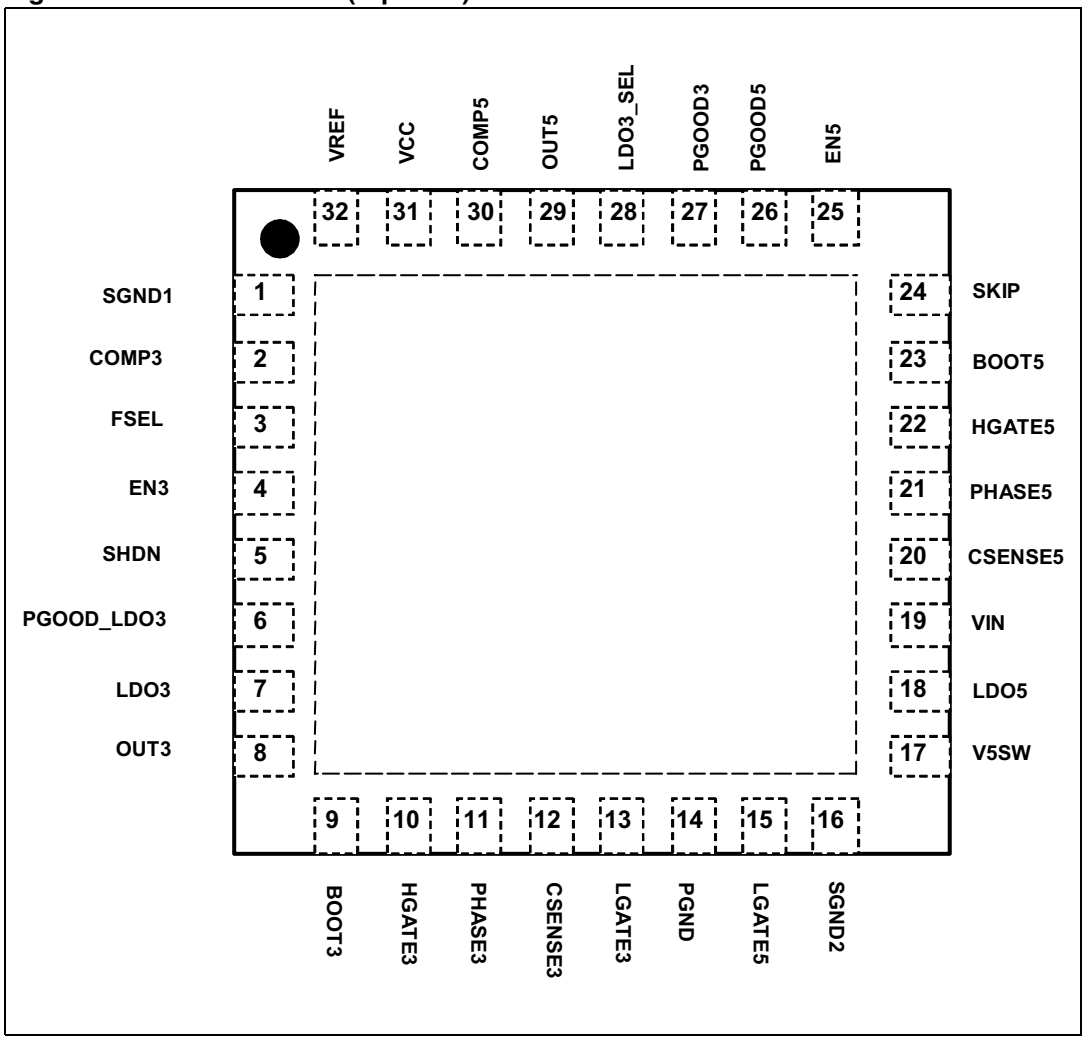
Figure 1. Functional block diagram



2 Pin settings

2.1 Connections

Figure 2. Pin connection (top view)



2.2 Functions

Table 2. Pin functions

Pin	Name	Description
1	SGND1	Signal ground. Reference for internal logic circuitry. It must be connected to the signal ground plan of the power supply. The signal ground plan and the power ground plan must be connected together in one point near the PGND pin.
2	COMP3	DC voltage error compensation pin for the 3.3V switching section.
3	FSEL	Frequency selection pin. It provides a selectable switching frequency, allowing, allowing three different values of switching frequencies for the 5V/3.3V switching sections.
4	EN3	3.3V SMPS enable input. – The 3.3V section is enabled applying a voltage greater than 2.4V to this pin. – The 3.3V section is disabled applying a voltage lower than 0.8V. When the section is disabled the High Side gate driver goes low and Low Side gate driver goes high. If both EN3 and EN5 pins are low and SHDN pin is high the device enters in standby mode.
5	SHDN	Shutdown control input. – The device switch off if the SHDN voltage is lower than 0.8V (Shutdown mode) – The device switch on if the SHDN voltage is greater than 1.7V. The SHDN pin can be connected to the battery through a voltage divider to program an undervoltage lockout. In shutdown mode, the gate drivers of the two switching sections are in high impedance (high-Z).
6	PGOOD LDO3	Power Good signal for the 3.3V linear regulator. This pin is an open drain output. It is shorted to GND if LDO3_SEL pin is at its low level or if the output voltage on LDO3 pin is lower than 2.6V.
7	LDO3	3.3V Linear regulator output. LDO3 can provide 100mA peak current.
8	OUT3	Output voltage sense for the 3.3V switching section.This pin must be directly connected to the output voltage of the switching section.
9	BOOT3	Bootstrap capacitor connection for the switching 3.3V section. It supplies the high-side gate driver.
10	HGATE3	High-side gate driver output for the 3.3V section.
11	PHASE3	Switch node connection and return path for the high side driver for the 3.3V section.
12	CSENSE3	Current sense input for the 3.3V section. This pin must be connected through a resistor to the drain of the synchronous rectifier (R_{DSON} sensing) to set the current limit threshold.
13	LGATE3	Low-side gate driver output for the 3.3V section.
14	PGND	Power ground. This pin must be connected to the power ground plan of the power supply.
15	LGATE5	Low-side gate driver output for the 5V section.
16	SGND2	Signal ground for analog circuitry. It must be connected to the signal ground plan of the power supply.
17	V5SW	Internal 5V regulator bypass connection. – If V5SW is connected to OUT5 (or to an external 5V supply) and V5SW is greater than 4.9V, the LDO5 regulator shuts down and the LDO5 pin is directly connected to OUT5 through a 3W (max) switch. – If V5SW is connected to GND, the LDO5 linear regulator is always on.
18	LDO5	5V internal regulator output. It can provide up to 100mA peak current. LDO5 pin supplies embedded low side gate drivers and an external load.

Table 2. Pin functions (continued)

Pin	Name	Description
19	VIN	Device input supply voltage. A bypass filter (4W and 4.7mF) between the battery and this pin is recommended.
20	CSENSE5	Current sense input for the 5V section. This pin must be connected through a resistor to the drain of the synchronous rectifier (R_{DSON} sensing) to set the current limit threshold.
21	PHASE5	Switch node connection and return path for the high side driver for the 5V section.
22	HGATE5	High-side gate driver output for the 5V section.
23	BOOT5	Bootstrap capacitor connection for the 5V section. It supplies the high-side gate driver.
24	SKIP	Pulse skip mode control input. – If the pin is connected to LDO5 the PWM mode is enabled. – If the pin is connected to GND, the pulse skip mode is enabled. – If the pin is connected to VREF the pulse skip mode is enabled but the switching frequency is kept higher than 33kHz (No-audible pulse skip mode).
25	EN5	5V SMPS enable input. – The 5V section is enabled applying a voltage greater than 2.4V to this pin. – The 5V section is disabled applying a voltage lower than 0.8V. When the section is disabled the High Side gate driver goes low and Low Side gate driver goes high.
26	PGOOD5	Power Good signal for the 5V section. This pin is an open drain output. The pin is pulled low if the output is disabled or if it is out of approximately +/- 10% of its nominal value.
27	PGOOD3	Power Good signal for the 3.3V section. This pin is an open drain output. The pin is pulled low if the output is disabled or if it is out of approximately +/- 10% of its nominal value.
28	LDO3SEL	Control pin for the 3.3V internal linear regulator. This pin determines three operative modes for the LDO3. – If LDO3_SEL pin is connected to GND the LDO3 output is always disabled. – If LDO3_SEL pin is connected to LDO5 the LDO3 internal regulator is always enabled. – If LDO3_SEL pin is connected to VREF and OUT3 is greater than about 3V, the LDO3 regulator shuts down and the LDO3 pin is be directly connected to OUT3 through a 3W (max) switch.
29	OUT5	Output voltage sense for the 5V switching section.This pin must be directly connected to the output voltage of the switching section.
30	COMP5	DC voltage error compensation pin for the 5V switching section.
31	VCC	Device Supply Voltage pin. It supplies the all the internal analog circuitry except the gate drivers (see LDO5). Connect this pin to LDO5.
32	VREF	High accuracy output voltage reference (1.230V). It can deliver 50uA. Bypass to SGND with a 100nF capacitor.
33	EXP PAD	Exposed pad.

3 Electrical data

3.1 Maximum rating

Table 3. Absolute maximum ratings

Parameter		Value	Unit
COMPx,FSEL,LDO3_SEL,VREF,SKIP to SGND1,SGND2		-0.3 to VCC + 0.3	V
ENx,SHDN,PGOOD_LDO3,OUTx,PGOODx,VCC to SGND1,SGND2		-0.3 to 6	V
LDO3 to SGND1,SGND2		-0.3 to LDO5 + 0.3	V
LGATEx to PGND		-0.3 (1) to LDO5 + 0.3	V
HGATEx and BOOTx, to PHASEx		-0.3 to 6	V
PHASEx to PGND		-0.6 (2) to 36	V
CSENSEx, to PGND		-0.6 to 42	V
CSENSEx to BOOTx_		-6 to 0.3	V
V5SW, LDO5 _to PGND		-0.3 to 6	V
VIN to PGND		-0.3 to 36	V
PGND to SGND1,SGND2_		-0.3 to 0.3	V
Power Dissipation at Tamb = 25ºC		2	W
Maximum withstanding Voltage range test condition: CDF-AEC-Q100-002- “Human Body Model” acceptance criteria: “Normal Performance”	VIN pin	±1000	V
	Other pins	±2000	

1. LGATEx to PGND up to -1V for t < 40ns
2. PHASE to PGND up to -2.5V for t < 10ns

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	35	°C/W
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction operating temperature range	-10 to 125	°C

4 Electrical characteristics

V_{IN} = 12V, T_A = 0°C to 85°C, unless otherwise specified

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Supply section						
VIN	Input voltage range	Vout=Vref, LDO5 in regulation FSEL to GND	5.5		28	V
Vcc	IC supply voltage		4.5		5.5	V
V_{V5SW}	Turn-on voltage threshold			4.8	4.9	V
	Turn-off voltage threshold		4.6	4.75		V
	Hysteresis		20	50		mV
V_{V5SW}	Maximum operating range				5.5	V
Rdson	LDO5 internal bootstrap switch resistance	V5SW > 4.9V		1.8	3	Ω
Rdson	LDO3 internal bootstrap switch resistance	VOUT3 = 3.3V		1.8	3	Ω
	OUT3, OUT5 discharge mode on-resistance			16	25	Ω
	OUT3, OUT5_ discharge mode synchronous rectifier turn-on level		0.2	0.35	0.5	V
Pin	Operating power consumption	V_{OUT5}>5.1V,V_{OUT3}>3.34V V5SW to 5V LDO5, LDO3 no load			4	mW
Ish	V_{IN} shutdown current	SHDN connected to GND,		14	18	µA
Isb	V_{IN} standby current	ENx to GND, V5SW to GND, LDO3_SEL to 5V		270	380	µA
Shutdown section						
V_{SHDN}	Device on threshold		1.2	1.5	1.7	V
	Device off threshold		0.8	0.85	0.9	V
Soft start section						
	Soft start ramp time		2		3.5	ms
Current limit and zero crossing comparator						

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
I_{CSENSE}	Input bias current limit			90	100	110	µA
	Comparator offset	V_{CSENSE}-V_{PGND}		-6		6	mV
	Zero crossing comparator offset	V_{PGND}-V_{PHASE}		-1		11	mV
	Fixed negative current limit threshold	V_{PGND}-V_{PHASE}			-120		mV
On time pulse width							
Ton	ON-time duration	FSEL to GND	OUT5=5V	1685	1985	2285	ns
			OUT3=3.3V	780	920	1060	
		FSEL to VREF	OUT5=5V	1115	1315	1515	
			OUT3=3.3V	585	690	795	
		FSEL to LDO5	OUT5=5V	830	980	1130	
			OUT3=3.3V	470	555	640	
OFF time							
T_{OFFMIN}	Minimum off time				400	500	ns
Voltage reference							
V_{REF}	Voltage accuracy	4.2V<V_{LDO5}< 5.5V		1.217	1.230	1.243	V
	Load regulation	-100µA< I_{REF} < 100µA		-4		4	mV
	Undervoltage lockout fault threshold	Falling edge of REF				0.95	V
Integrator							
COMP	Over voltage clamp	Normal mode			250		mV
		Pulse skip mode			60		
	Under voltage clamp				-150		
Line regulation							
		Both SMPS, 6V<Vin<28V(1)			0.004		%/V
LDO5 linear regulator							
V_{LDO5}	LDO5 linear output voltage	6V<VIN<28V, 0<I_{LDO5}<50mA		4.9	5.0	5.1	V
	LDO5 line regulation	6V< VIN < 28V, I_{LDO5} =50mA , LDO3_SEL tied to GND				0.004	%/V
I_{LDO5}	LDO5 current limit	V_{LDO5} > UVLO, I_{LDO3}=0A V_{OUT5}>5.1V, V_{OUT3}>3.34V		270	350	400	mA
UVLO	Under voltage lockout of LDO5			3.94	4	4.13	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
LDO3 linear regulator						
V_{LDO3}	LDO3 linear output voltage	0.5mA<I_{LDO3}<50mA	3.23	3.3	3.37	V
I_{LDO3}	LDO3 current limit	V_{LDO5} > UVLO	130	165	200	mA
High and low gate drivers						
	HGATE Driver On-resistance	HGATEx high state (pull-up)		2.0	3	Ω
		HGATEx low state (pull-down)		1.6	2.7	Ω
	LGATE Driver On-resistance	LGATEx high state (pull-up)		1.4	2.1	Ω
		LGATEx low state (pull-down)		0.8	1.2	Ω
PGOOD pins UVP/OVP protections						
OVP	Over voltage threshold	Both SMPS sections with respect to VREF.	113	116	120	%
UVP	Under voltage threshold		66	70	72	%
PGOOD3,5	Upper threshold (VFB-VREF)		107	110	113	%
	Lower threshold (VFB-VREF)		90	92	94	%
$I_{PGOOD3,5}$	PGOOD leakage current	$V_{PGOOD3,5}$ forced to 5.5V			1	uA
$V_{PGOOD3,5}$	Output low voltage	ISink = 4mA		150	250	mV
PGOOD LDO3	Rising voltage threshold			77.7	81.1	%
	Falling voltage threshold		72.1	76.6		%
	Hysteresis		20	30		mV
I_{PGOOD_LDO3}	PGOOD leakage current	$V_{PGOOD\ LDO3}$ forced to 5.5V			1	uA
V_{PGOOD_LDO3}	Output low voltage	ISink = 4mA		150	250	mV
Thermal shutdown						
T_{SDN}	Shutdown temperature			150		°C
Power management pins						
EN3,5	SMPS disabled threshold	(2)	0.8			V
	SMPS enabled threshold	(2)			2.4	

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
FSEL	Frequency selection range	Low level(2)			0.5	V
		Middle level(2)	1.0		V_{LDO5}-1.5	
		High level(2)	V_{LDO5}-0.8			
LDO3 SEL	3.3V linear regulator selection pin	Always-off level(2)			0.5	
		Bootstrap level(2)	1.0		V_{LDO5}-1.5	
		Always-on level(2)	V_{LDO5}-0.8			
SKIP	Pulse skip mode	(2)			0.5	V
	PWM mode	(2)	1.0		V_{LDO5}-1.5	
	Frequency clamp mode	(2)	V_{LDO5}-0.8			
	Input leakage current	$V_{EN3,4}$= 0 to 5V			1	µA
		V_{SKIP}= 0 to 5V			1	
		V_{SHDN}= 0 to 5V			0.1	
		V_{FSEL}= 0 to 5V			1	
		V_{LDO3_SEL}= 0 to 5V			1	

1. by demonstration board test
2. by design

5 Typical operating characteristics

FSEL = GND (200/300 kHz), SKIP = GND (skip mode), LDO3_SEL = VREF, V5SW = OUT5, input voltage VIN = 12 V, SHDN, EN3 and EN5 high, no load unless specified.

Figure 3. 5 V output efficiency vs load current

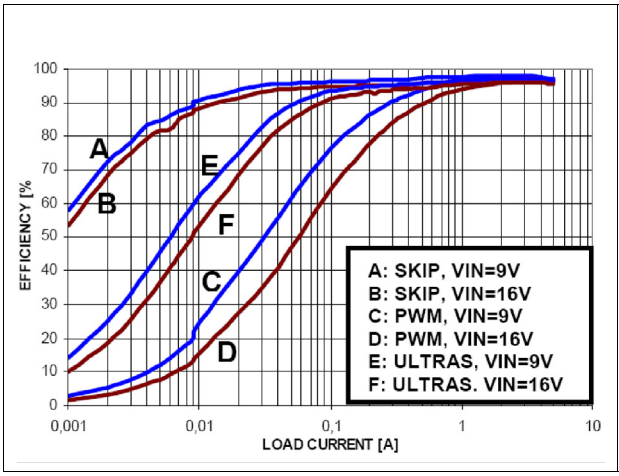


Figure 4. 3.3 V output efficiency vs load current

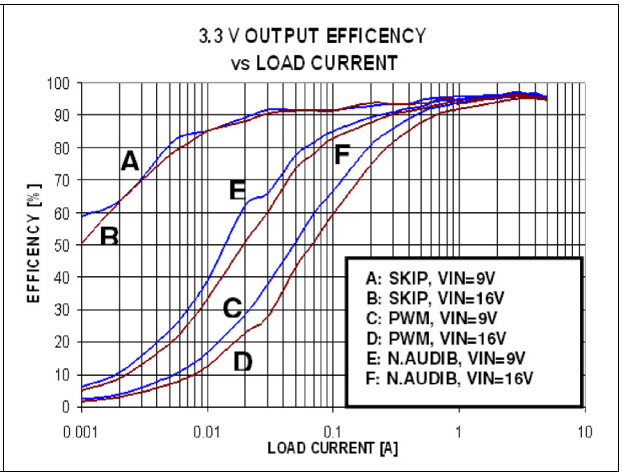


Figure 5. PWM no load input battery vs input voltage

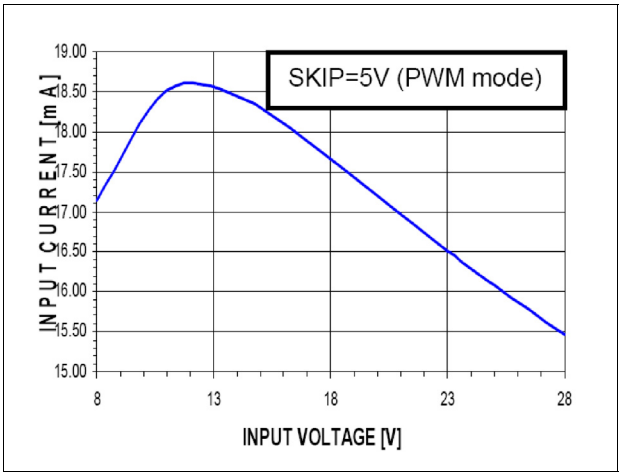


Figure 6. Skip no load battery current vs input voltage

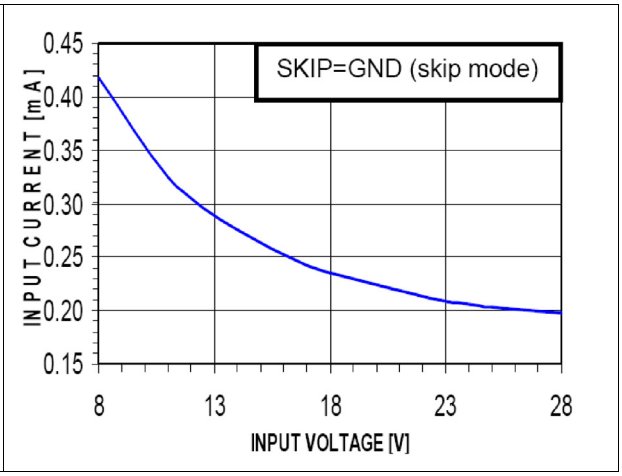


Figure 7. Standby mode input battery current vs input voltage

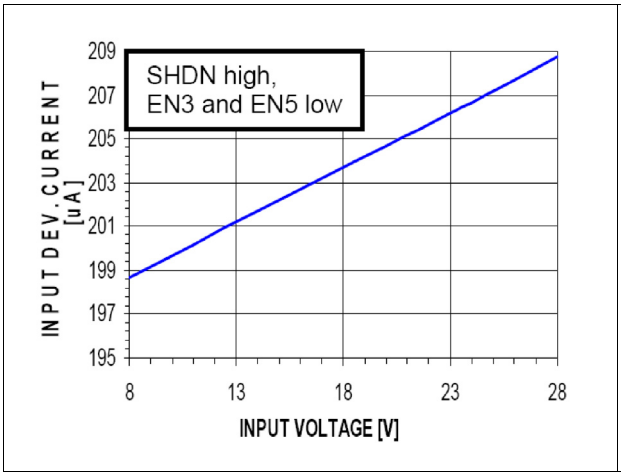


Figure 8. Shutdown mode input device current vs input voltage

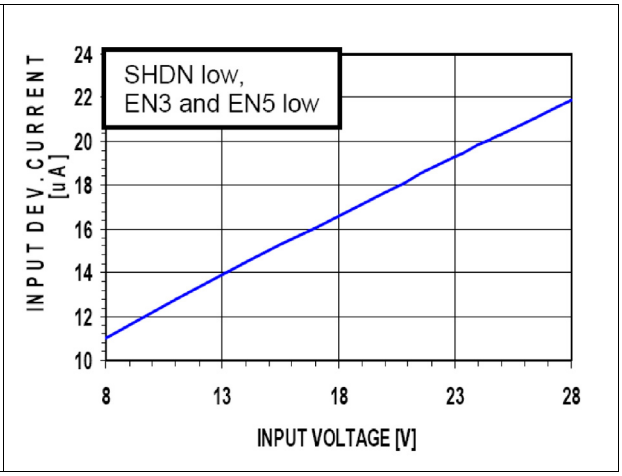


Figure 9. 5V switching frequency vs load current

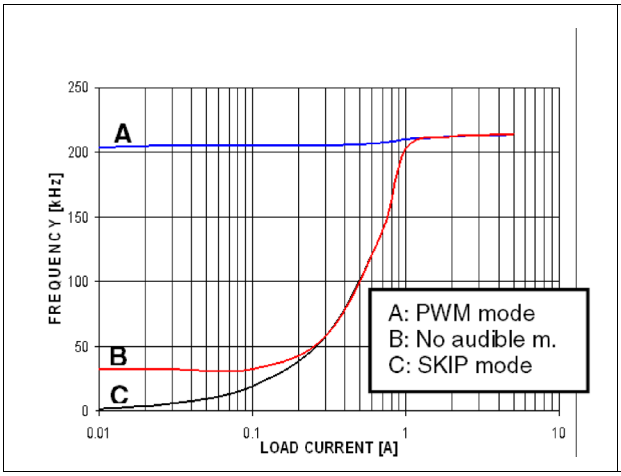


Figure 10. 3.3V switching frequency vs load current

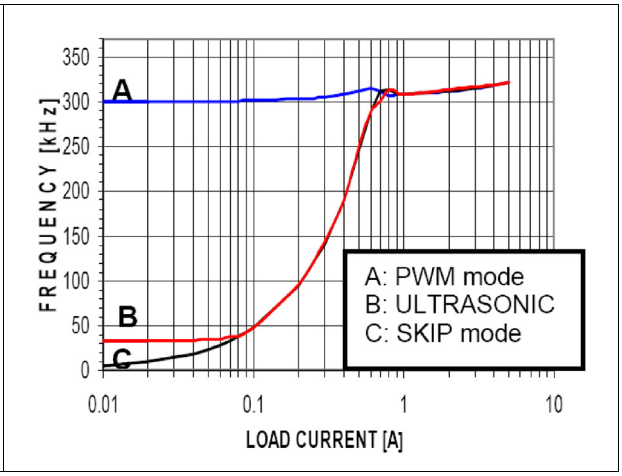


Figure 11. LDO5 vs output voltage

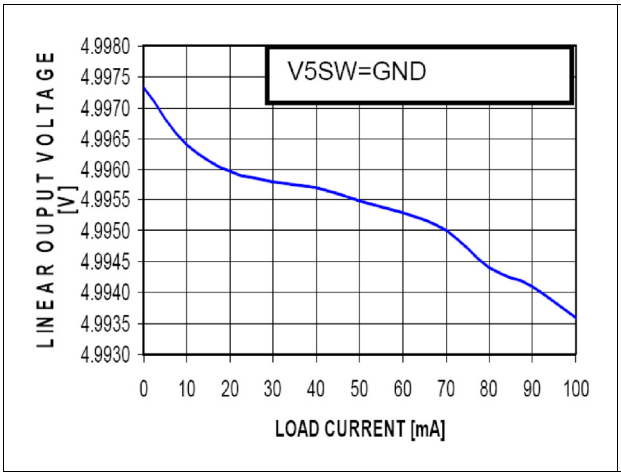


Figure 12. LDO3 vs output voltage

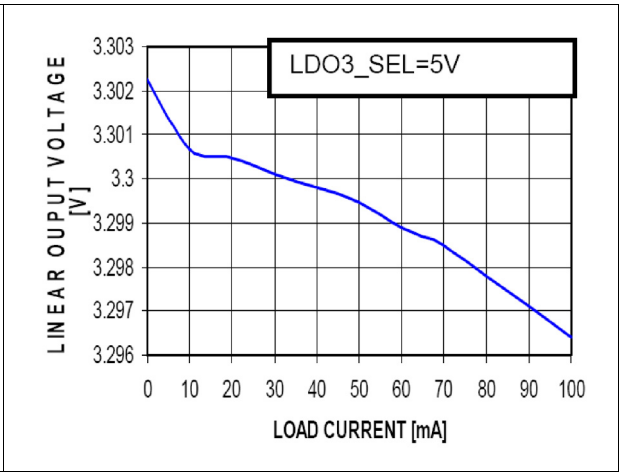


Figure 13. 5V voltage regulation vs load current

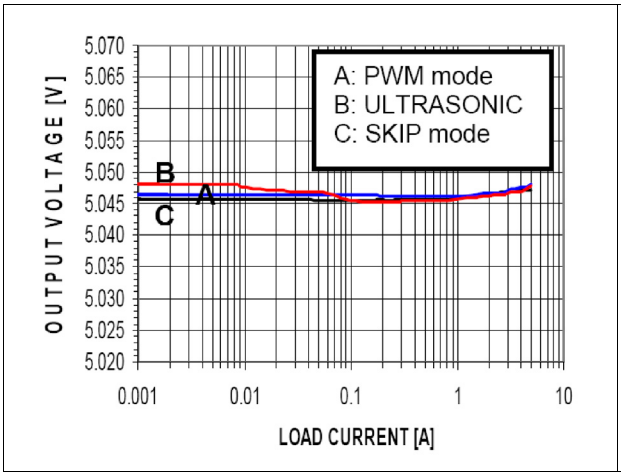


Figure 14. 3.3 V voltage regulation vs load current

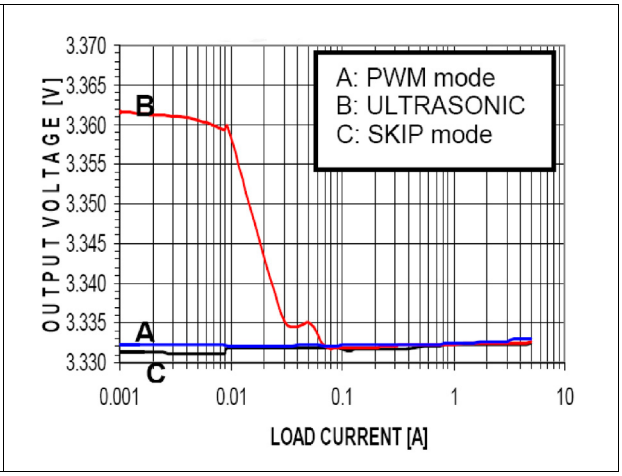


Figure 15. Voltage reference vs load current

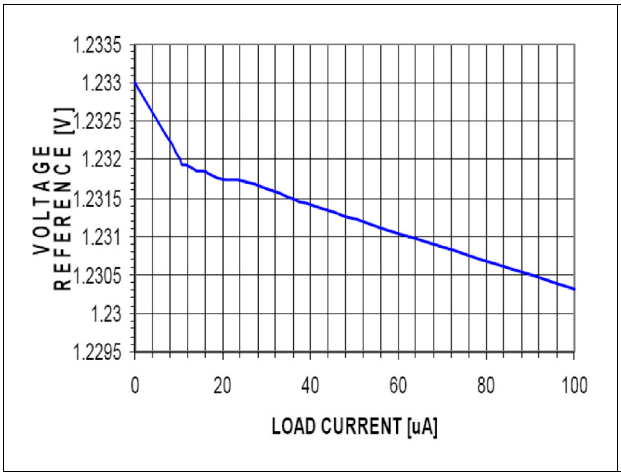


Figure 16. OUT5, LDO3 and LDO5 Power-Up

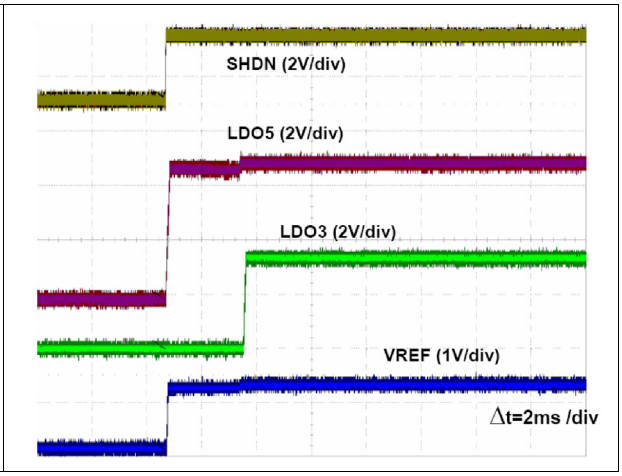


Figure 17. 5 V PWM load transient

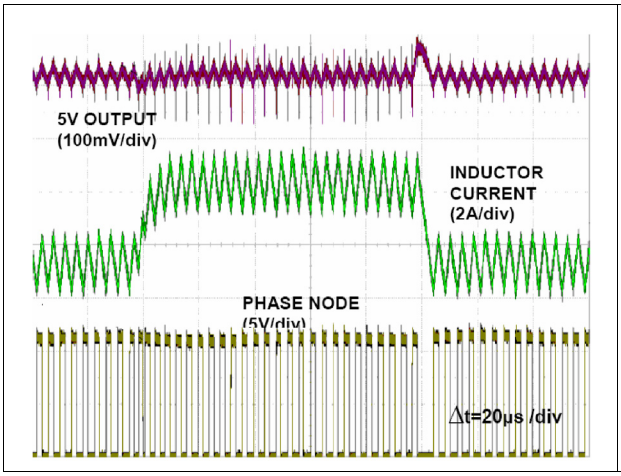


Figure 18. 3.3 V PWM load transient

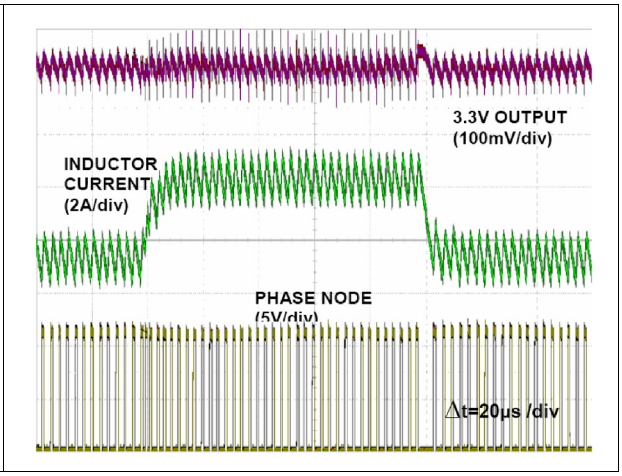


Figure 19. 5 V soft start (0.75 Ω load)

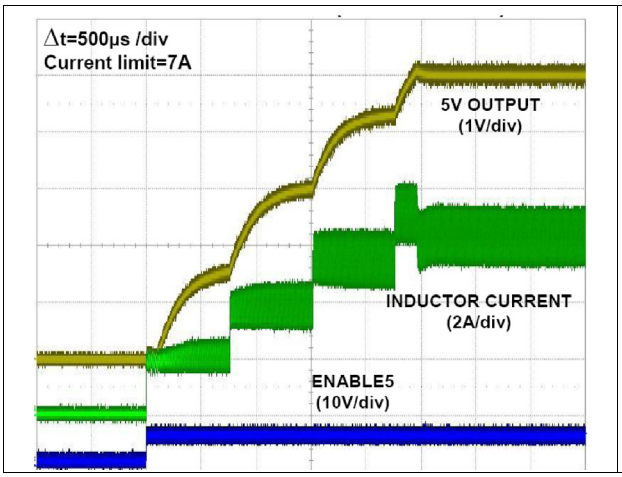


Figure 20. 3.3 V soft start (0.55 Ω load)

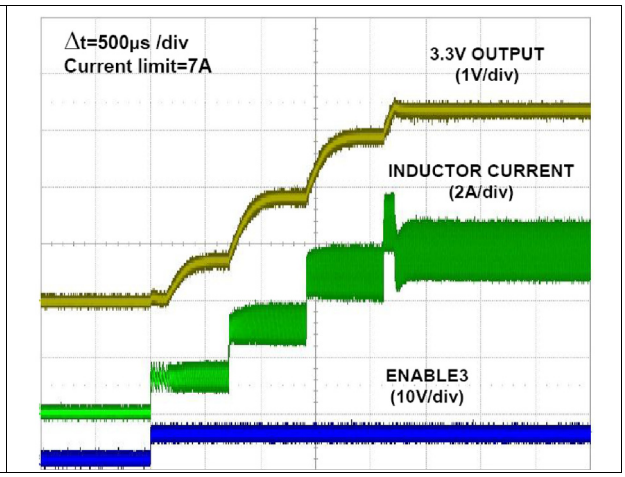


Figure 21. 5 V soft end (no load)

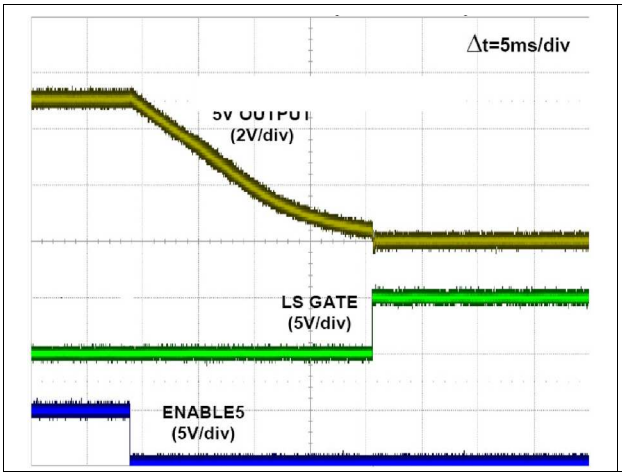


Figure 22. 3.3 V soft end (no load)

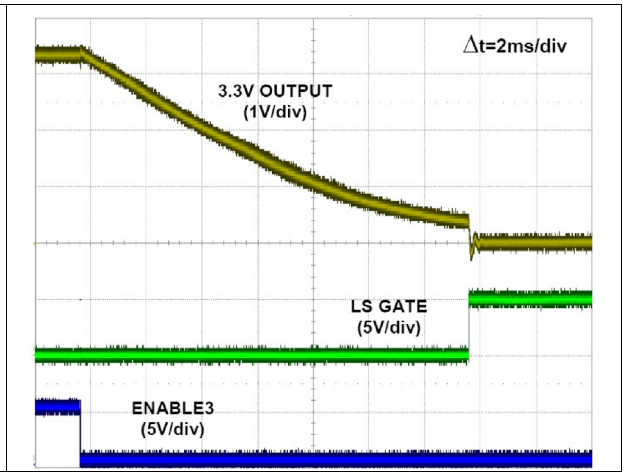


Figure 23. 5 V soft end (1 Ω load)

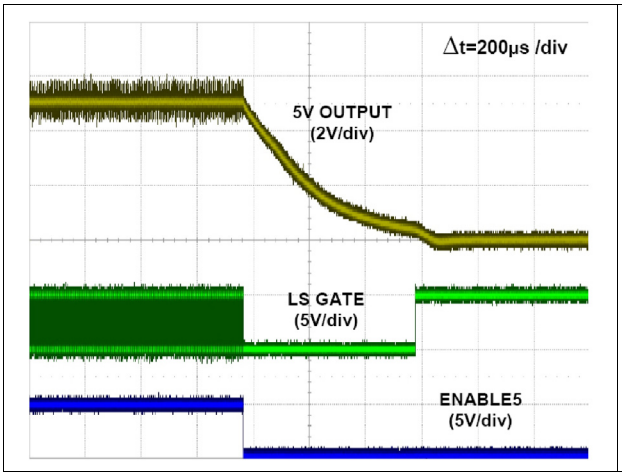


Figure 24. 3.3 V soft end (1 Ω load)

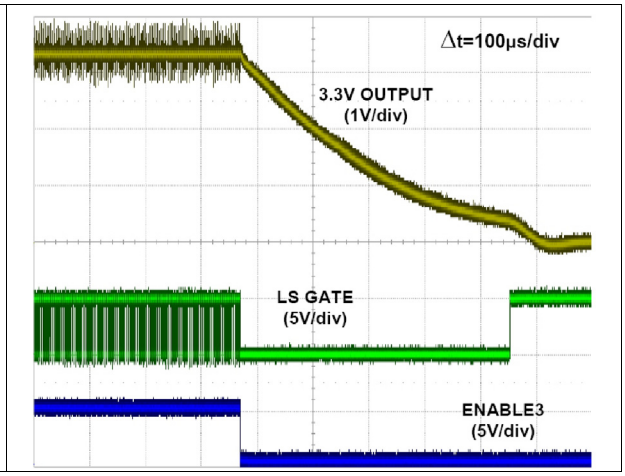


Figure 25. 5 V no audible skip mode

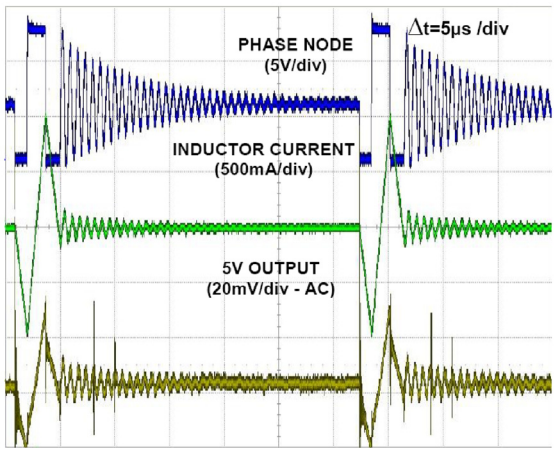
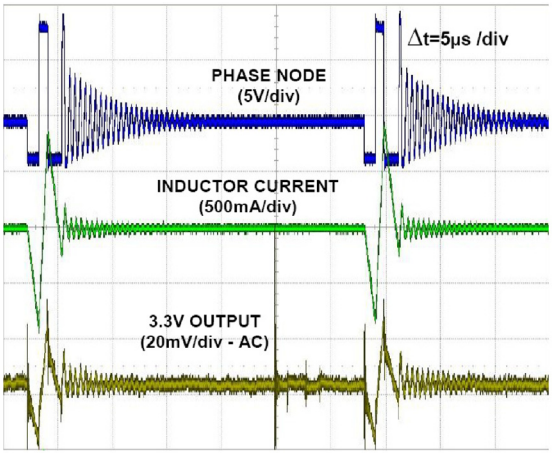
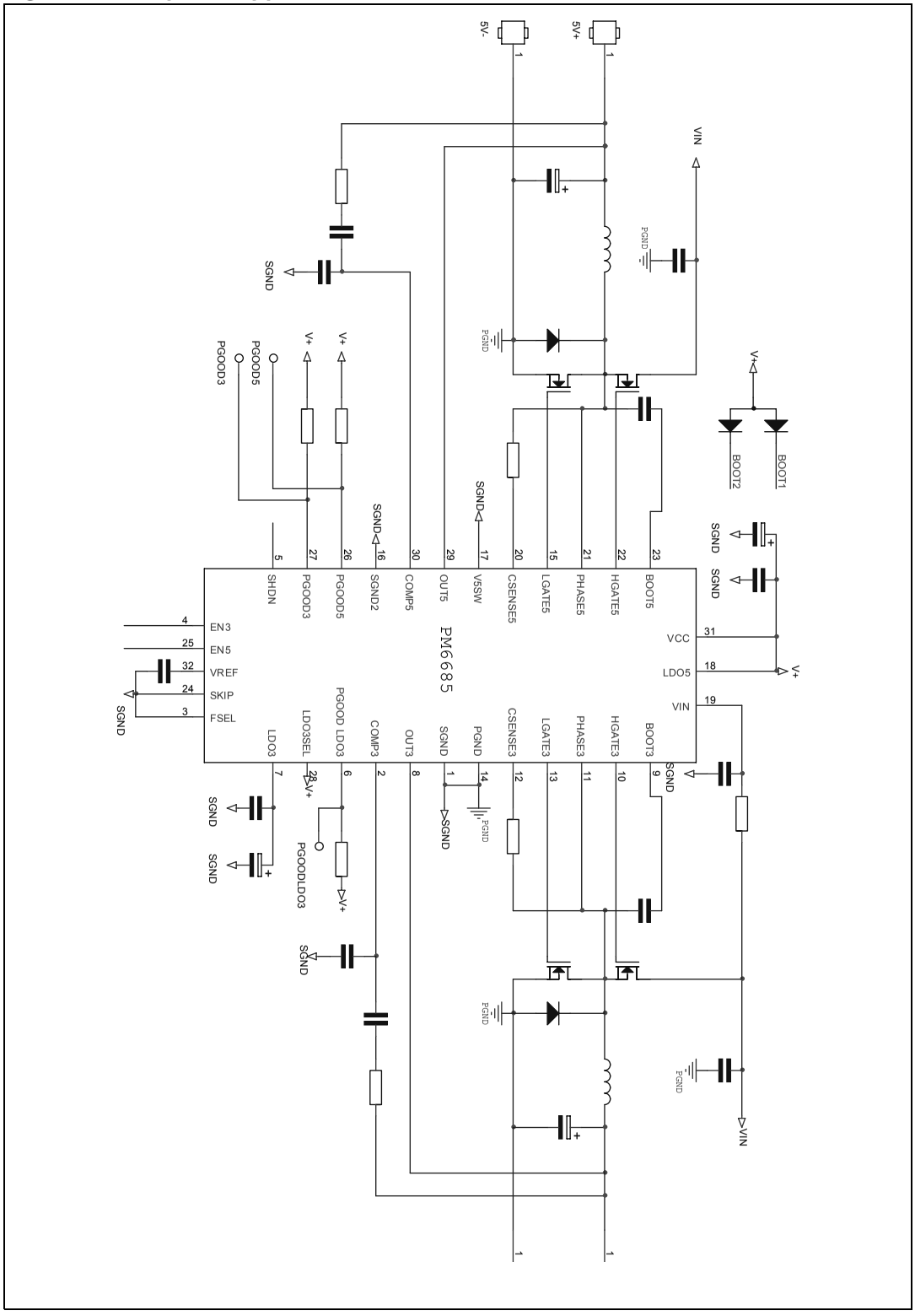


Figure 26. 3.3 V no audible skip mode



6 Application schematic

Figure 27. Simplified application schematic



7 Device description

The PM6685 is a dual step-down controller dedicated to provide logic voltages for notebook computers.

It is based on a Constant On Time control architecture. This type of control offers a very fast load transient response with a minimum external component count. A typical application circuit is shown in *Figure 27 on page 18*. The PM6685 regulates two fixed output voltages: 5 V and 3.3 V. The switching frequency of the two sections can be adjusted to approximately 200/300 kHz, 300/400 kHz or 400/500 kHz respectively. In order to maximize the efficiency at light load condition, a pulse skipping mode can be selected. The PM6685 includes also two linear regulators (LDO5 and LDO3) that allow the shutdown of the respective switching sections in low consumption status. On the other hand, to maximize the efficiency in higher consumption status, the linear regulators can be turned off and their outputs can be supplied directly from the switching outputs. The PM6685 provides protection versus overvoltage, undervoltage and overtemperature as well as power good signals for monitoring purposes. An external 1.230 V reference is available.

7.1 Constant on time PWM control

If the SKIP pin is tied to 5 V, the device works in PWM mode. Each power section has an independent on time control.The PM6685 implements a pseudo-fixed switching frequency, constant on time (COT) controller as core of the switched mode section. Each power section has an independent COT control.

The COT controller is based on a relatively simple algorithm and uses the ripple voltage due to the output capacitor's ESR to trigger the fixed on-time one-shot generator. In this way, the output capacitor's ESR acts as a current sense resistor providing the appropriate ramp signal to the PWM comparator. On-time one-shot duration is directly proportional to the output voltage VOUT, sensed at the OUT5/OUT3 pins, and inversely proportional to the input voltage VIN, sensed at the VIN pin, as follows:

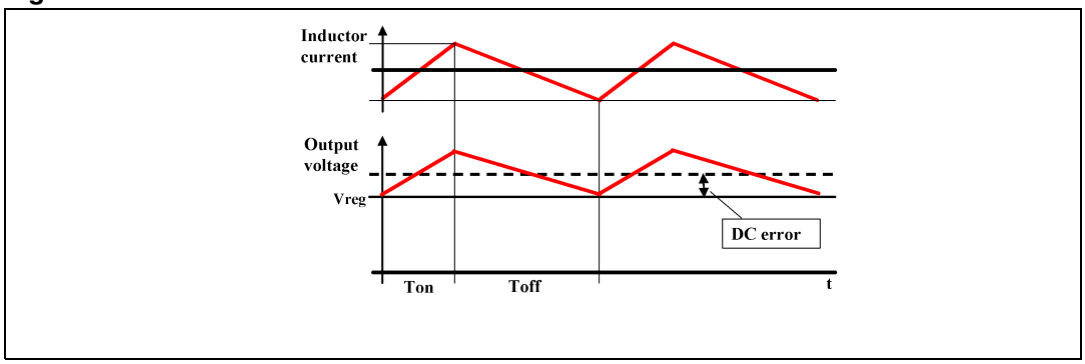
Equation 1

$$T_{ON} = K \times \frac{V_{OUT}}{V_{IN}}$$

This leads to a nearly constant switching frequency, regardless of input and output voltages.

When the output voltage goes lower than the regulated voltage Vreg, the on-time one shot generator directly drives the high side MOSFET for a fixed on time allowing the inductor current to increase; after the on time, an off time phase, in which the low side MOSFET is turned on, follows. *Figure 28 on page 20* shows the inductor current and the output voltage waveforms in PWM mode.

Figure 28. Constant on time PWM control



The duty cycle D of the buck converter in steady state is:

Equation 2

$$D = \frac{V_{OUT}}{V_{IN}}$$

The PWM control works at a nearly fixed frequency f_{SW}:

Equation 3

$$f_{sw} = \frac{D}{T_{ON}} = \frac{\frac{V_{OUT}}{V_{IN}}}{K_{ON} \times \frac{V_{OUT}}{V_{IN}}} = 1/K_{ON}$$

As mentioned the steady state switching frequency is theoretically independent from battery voltage and from output voltage. Actually the frequency depends on parasitic voltage drops that are present during the charging path (high side switch resistance, inductor resistance (DCR)) and discharging path (low side switch resistance, DCR). As a result the switching frequency increases as a function of the load current. Standard switching frequency values can be selected for both sections by pin FSEL as shown in the following table:

Table 6. FSEL pin selection

FSEL	SMPS 5V		SMPS 3.3V	
	Frequency	K_{ON}	Frequency	K_{ON}
SGND	212kHz	4,7µs	297,6kHz	3.36µs
VREF	323kHz	3µs	400kHz	2.5µs
LDO5	432kHz	2.31µs	500kHz	2.0µs

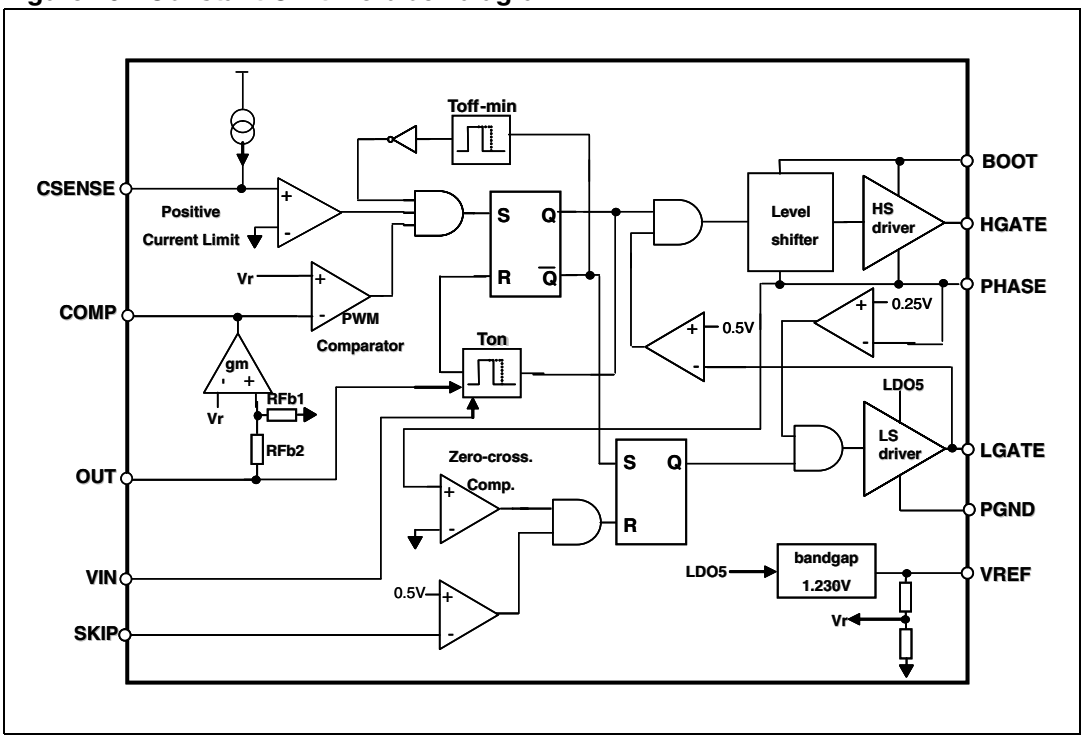
The values in the table are measured with V_{in} =12 V, operation mode = PWM and I_{load} = 2 A. The other output are unloaded.

7.2 Constant on time architecture

Figure 29 on page 21 shows the simplified block diagram of a constant on time controller. A minimum off-time constrain (380 ns typ) is introduced to allow inductor valley current sensing on the synchronous switch. A minimum on-time(150 ns typ) is also introduced to assure the start-up switching sequence.

PM6685 has a one-shot generator for each power section that turns on the high side MOSFET when the following conditions are satisfied simultaneously: the PWM comparator is high, the synchronous rectifier current is below the current limit threshold, and the minimum off-time has timed out. Once the on-time has timed out, the high side switch is turned off, while the synchronous switch is turned on according to the anti-cross conduction circuitry management. When the negative input voltage at the PWM comparator, which is a scaled-down replica of the output voltage ripple (see the R_{fb1}/R_{fb2} divider in *Figure 29*), reaches the valley limit (determined by internal reference V_r=0.9 V), the low-side MOSFET is turned off according to the anti-cross conduction logic once again, and a new cycle begins.

Figure 29. Constant ON-time block diagram

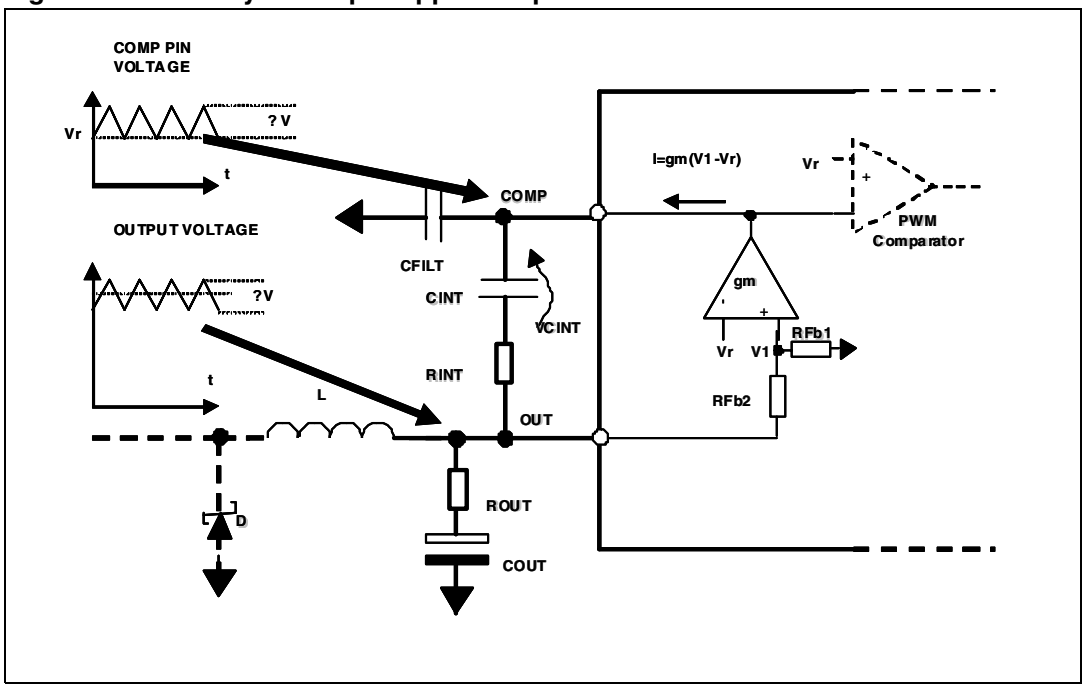


7.3 Output ripple compensation

In a classic constant on time control, the system regulates the valley value of the output voltage and not the average value, as shown in *Figure 28 on page 20*. In this condition, the output voltage ripple is source of a DC static error.

To compensate this error, an integrator network can be introduced in the control loop, by connecting the output voltage to the COMP5/COMP3(for the 5 V and 3.3 V sections respectively) pin through a capacitor C_{INT} as in *Figure 30 on page 22*.

Figure 30. Circuitry for output ripple compensation



The integrator amplifier generates a current, proportional to the DC errors, which decreases the output voltage in order to compensate the total static error, including the voltage drop on PCB traces. In addition, C_{INT} provides an AC path for the output ripple. In steady state, the voltage on COMP5/COMP3 pin is the sum of the reference voltage V_r and the output ripple (see *Figure 30*). In fact when the voltage on the COMP pin reaches V_r, a fixed Ton begins and the output increases.

For example, we consider V_{OUT}=5 V with an output ripple of ΔV=50m V. Considering C_{INT}>>C_{FILT}, the C_{INT} DC voltage drop V_{CINT} is about 5 V-Vr+25 mV=4.125 V. C_{INT} ensures an AC path for the output voltage ripple. Then the COMP pin ripple is a replica of the output ripple, with a DC value of Vr+25 mV =925 mV.

For more details about the output ripple compensation network, see the paragraph "*Closing the integrator loop*" in the *Design guidelines*.

7.4 Pulse skip mode

If the SKIP pin is tied to ground, the device works in skip mode.

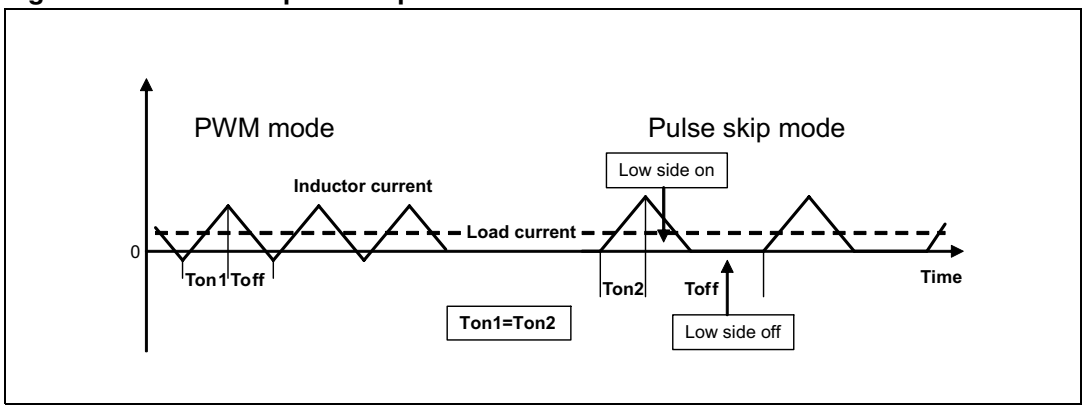
At light loads a zero-crossing comparator truncates the low-side switch on-time when the inductor current becomes negative. In this condition the section works in discontinuous conduction mode. The threshold between continuous and discontinuous conduction mode is:

Equation 4

$$ILOAD(SKIP) = \frac{V_{IN} - V_{OUT}}{2 \times L} \times T_{ON}$$

For higher loads the inductor current doesn't cross the zero and the device works in the same way as in PWM mode and the frequency is fixed to the nominal value.

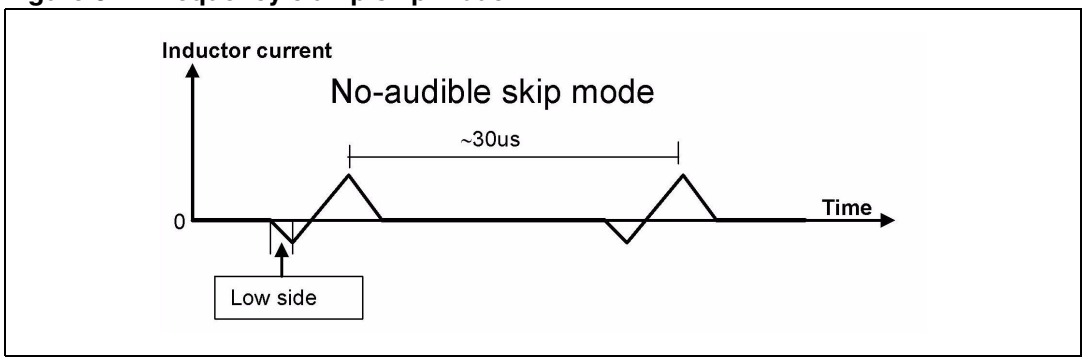
Figure 31. PWM and pulse skip mode inductor current



7.5 No-audible skip mode

If SKIP pin is tied to V_{REF}, a no-audible skip mode with a minimum switching frequency of 33 kHz is enabled. At light load condition, If there is not a new switching cycle within a 30 µs (typ.) period, a no-audible skip mode cycle begins.

Figure 32. Frequency clamp skip mode



The low side switch is turned on until the output voltage crosses about Vreg+1%. Then the high side MOSFET is turned on for a fixed on time period. Afterwards the low side switch is enabled until the inductor current reaches the zero-crossing threshold. This keeps the switching frequency higher than 33 kHz. As a consequence of the control, the regulated voltage can be slightly higher than Vreg (up to 1%).

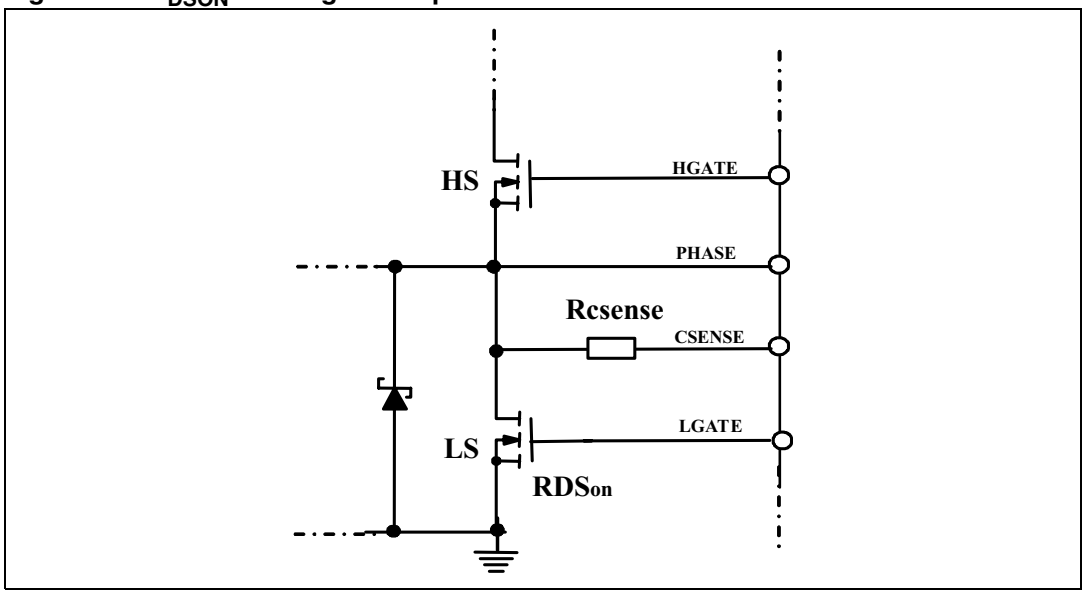
If, due to the load, the frequency is higher than 33 kHz, the device works like in skip mode.

No-audible skip mode reduces audio frequency noise that may occur in pulse skip mode at very light loads, keeping the efficiency higher than in PWM mode.

7.6 Current limit

The current-limit circuit employs a “valley” current-sensing algorithm. During the conduction time of the low side MOSFET the current flowing through it is sensed. The current-sensing element is the low side MOSFET on-resistance(*Figure 33*)

Figure 33. R_{DSON} sensing technique



An internal 100 µA ΔI_L current source (I_{CSENSE}) is connected to C_{SENSE} pin and determines a voltage drop on R_{CSENSE}. If the voltage across the sensing element is greater than this voltage drop, the controller doesn't initiate a new cycle. A new cycle starts only when the sensed current goes below the current limit.

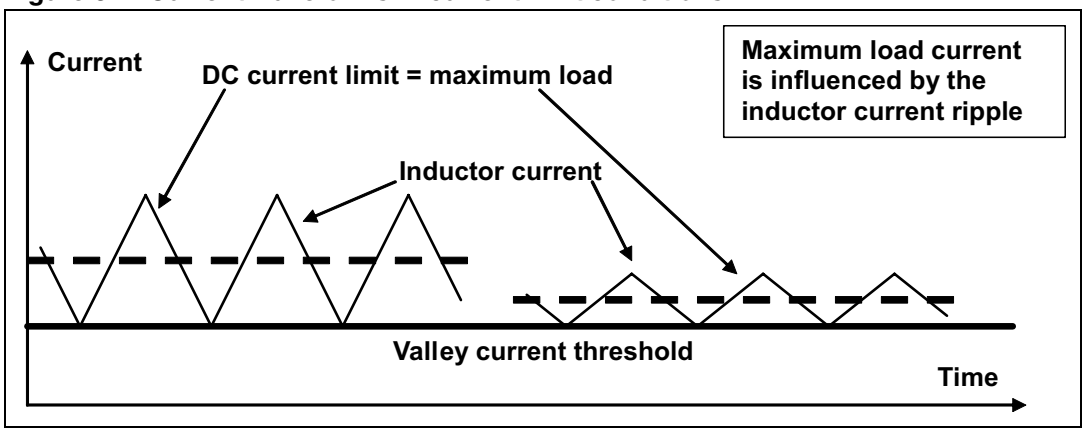
Since the current limit circuit is a valley current limit, the actual peak current limit is greater than the current limit threshold by an amount equal to the inductor ripple current. Moreover the maximum output current is equal to the valley current limit plus half of the inductor ripple current:

Equation 5

$$I_{LOAD}(max) = I_{Lvalley} + \frac{\Delta I_L}{2}$$

The output current limit depends on the current ripple, as shown in *Figure 34 on page 24*:

Figure 34. Current waveforms in current limit conditions



Being fixed the valley threshold, the greater the current ripple is, greater the DC output current is

The valley current limit can be set with resistor R_{CSENSE}:

Equation 6

$$R_{CSENSE} = \frac{R_{DSon} \times I_{Lvalley}}{I_{CSENSE}}$$

Where I_{CSENSE} = 100 µA, R_{DSon} is the drain-source on resistance of the low side switch. Consider the temperature effect and the worst case value in R_{DSon} calculation.

The accuracy of the valley current threshold detection depends on the offset of the internal comparator (ΔV_{OFF}) and on the accuracy of the current generator(ΔI_{CSENSE}):

Equation 7

$$\frac{\Delta I_{Lvalley}}{I_{Lvalley}} = \frac{\Delta I_{CSENSE}}{I_{CSENSE}} + \left[\frac{\Delta V_{OFF}}{R_{CSENSE} \times I_{CSENSE}} \times 100\right] + \frac{\Delta R_{CSENSE}}{R_{CSENSE}} + \frac{\Delta R_{SNS}}{R_{SNS}}$$

Where RSNS is the sensing element (R_{DSon}).

PM6685 provides also a fixed negative peak current limit to prevent an excessive reverse inductor current when the switching section sinks current from the load in PWM mode. This negative current limit threshold is measured between PHASE and SGND pins, comparing the magnitude drop on the PHASE node during the conduction time of the low side MOSFET with an internal fixed voltage of 120 mV.

If the current is sensed on the low side MOSFET, the negative valley-current limit INEG (if the device works in PWM mode) is given by:

Equation 8

$$I_{NEG} = \frac{120mV}{R_{DSon}}$$

7.7 Soft start and soft end

Each switching section is enabled separately by asserting high EN5/EN3 pins respectively. In order to realize the soft start, at the startup the overcurrent threshold is set 25% of the nominal value and the undervoltage protection (see related sections) is disabled. The controller starts charging the output capacitor working in current limit. The overcurrent threshold is increased from 25% to 100% of the nominal value with steps of 25% every 700 µs (typ.). After 2.8 ms (typ.) the undervoltage protection is enabled. The soft start time is not programmable. A minimum capacitor C_{INT} is required to ensure a soft start without any overshoot on the output:

Equation 9

$$C_{INT} \geq \frac{6uA}{\frac{I_{Lvalley}}{4} + \frac{\Delta I_L}{2}} \times C_{out}$$