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PM6686

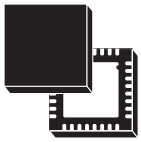
Dual step-down controller with adjustable voltages, adjustable LDO and auxiliary charge pump controller for notebook

Features

- 5.5 V to 28 V input voltage range
- Dual fixed OUT1 = 1.5 V/5 V and OUT2 = 1.05 V / 3.3 V outputs or adjustable OUT1 = 0.7 V to 5.5 V and OUT2 = 0.7 V to 2.5 V outputs, ± 1.5% accuracy over valley regulation
- Low-side MOSFETs' $R_{DS(on)}$ current sensing and programmable current limit
- Constant ON-time control
- Frequency selectable
- Soft-start internally fixed at 2 ms and soft-stop
- Selectable pulse skipping at light loads
- Selectable minimum frequency (33 kHz) in pulse skip mode
- Independent Power Good and EN signals
- Latched OVP and UVP
- Charge pump feedback
- Fixed 3.3 V/5.0 V, or adjustable output 0.7 V to 4.5 V, ± 1.5% (LDO): 200 mA
- 3.3 V reference voltage ± 2.0%: 5 mA
- 2.0 V reference voltage ± 1.0%: 50 µA

Applications

- Notebook computers
- Main (3.3 V/5 V), chipset (1.5 V/1.05 V), DDR1/2/3, graphic cards power supply
- PDAs, mobile devices, tablet PC or slates
- 3-4 cells Li+ battery powered devices



VFQFPN-32 5 x 5 mm

Description

PM6686 is a dual step-down controller specifically designed to provide extremely high efficiency conversion, with lossless current sensing technique. The constant on-time architecture assures fast load transient response and the embedded voltage feed-forward provides nearly constant switching frequency operation. Pulse skipping technique increases efficiency at very light load. Moreover a minimum switching frequency of 33 kHz is selectable to avoid audio noise issues. The PM6686 provides a selectable switching frequency, allowing three different values of switching frequencies for the two switching sections. The output voltages OUT1 and OUT2 can be programmed to regulate 1.5 V/5 V and 1.05 V/3.3 V outputs respectively or can deliver two adjustable output voltages. An optional external charge pump can be monitored. This device embeds a linear regulator that can provide 3.3 V/5 V or an adjustable voltage from 0.7 V to 4.5 V output. The linear regulator provides up to 100 mA output current. LDO can be bypassed with the switching regulator outputs or with an external power supply (switchover function).

When in switchover, the LDO output can source up to 200 mA.

Table 1. Device summary

Order codes	Package	Packaging
PM6686	VFQFPN-32L 5 x 5 mm	Tray
PM6686TR		Tape and reel

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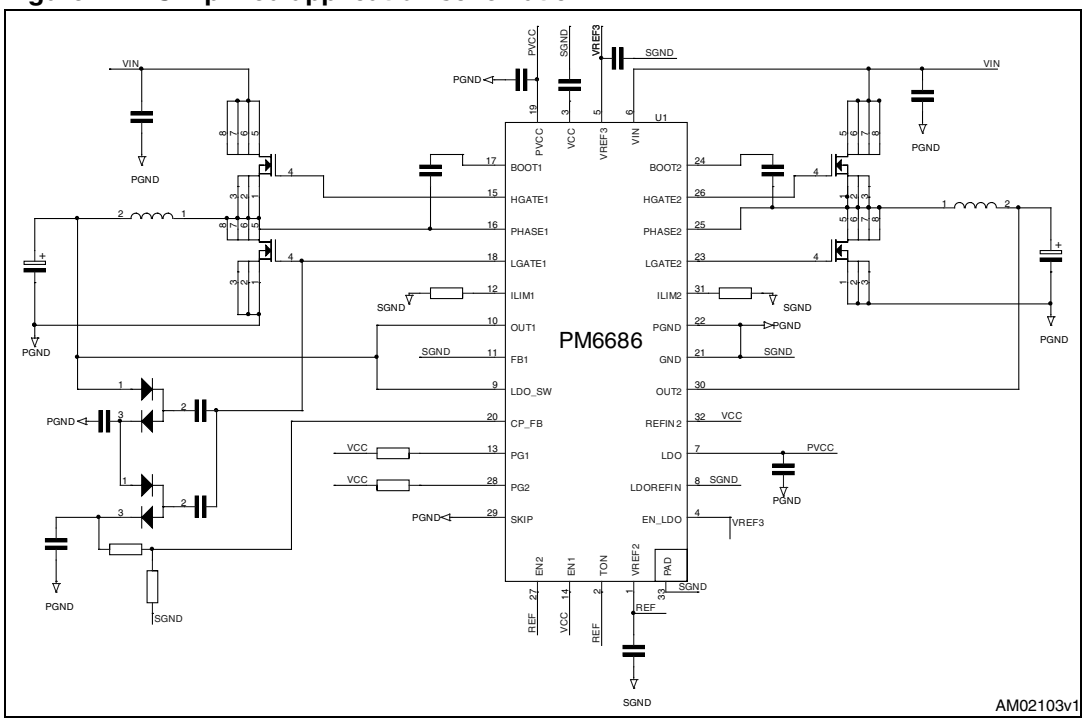
1 Simplified application schematic

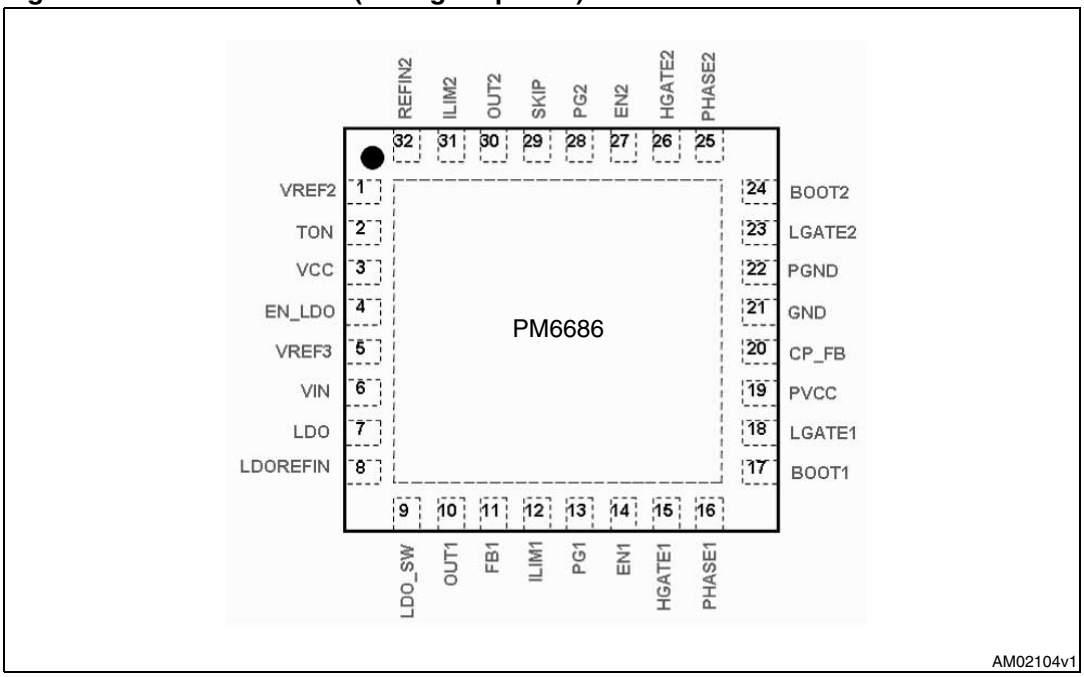
Figure 1. Simplified application schematic



2 Pin settings

2.1 Connections

Figure 2. Pin connection (through top view)



2.2 Pin descriptions

Table 2. Pin descriptions

N°	Pin	Function
1	VREF2	Internal 2 V high accuracy voltage reference. It can deliver 50 µA. Loading VREF2 can affect FB and output accuracy. Bypass to GND with a 100 nF capacitor.
2	TON	Frequency selection pin. It provides a selectable switching frequency, allowing three different values of switching frequencies for the switching sections.
3	VCC	Controller supply voltage input. Bypass to GND with a 1 µF capacitor.
4	EN_LDO	Enable input for the linear regulator. The LDO is enabled if EN_LDO is > 1.6 V and is disabled if EN_LDO < 1 V.
5	VREF3	Internal 3.3 V high accuracy voltage reference. It can deliver 5 mA if bypassed to GND with a 10 nF capacitor. If not used, it can be left floating.
6	VIN	Device supply voltage pin. VIN is used in the on-time generators of the two switching controllers. VIN is also used to power the linear regulator when the switchover function is not active. Connect VIN to the battery input and bypass with a 1 µF capacitor.

Table 2. Pin descriptions (continued)

N°	Pin	Function
7	LDO	Linear regulator output. It can provide up to 100 mA peak current. The LDO regulates at 5 V If LDOREFIN is connected to GND. When the LDO is set at 5 V and LDO_SW is within 5 V switchover threshold, the internal regulator shuts down and the LDO output pin is connected to LDO_SW through a 0.8 Ω switch. The LDO regulates at 3.3 V if LDOREFIN is connected to VCC. When the LDO is set at 3.3 V and LDO_SW is within 3.3 V switchover threshold, the internal regulator shuts down and the LDO output pin is connected to LDO_SW through a 1.1 Ω switch. Bypass LDO output to GND with a minimum of 4.7 µF ceramic capacitor.
8	LDOREFIN	Feedback of the adjustable linear regulator. Connect LDOREFIN to GND for fixed 5 V operation. Connect LDOREFIN to VCC for fixed 3.3 V operation. LDOREFIN can be used to program LDO output voltage from 0.7 V to 4.5 V: LDO output is two times the voltage of LDOREFIN. The switchover function is disabled in adjustable mode.
9	LDO_SW	Source of the switchover connection. LDO_SW is the switchover source voltage for the LDO when LDOREFIN is connected to GND or VCC. Connect LDO_SW to 5 V if LDOREFIN is tied to GND. Connect LDO_SW to 3.3 V if LDOREFIN is tied to VCC.
10	OUT1	Output voltage sense for the switching section 1.This pin must be directly connected to the output voltage of the switching section. It provides also the feedback for the switching section 1 when FB1 is tied to GND/VCC.
11	FB1	Feedback input for the switching section 1: – If this pin is connected to GND, OUT1 operates at 5 V – If this pin is connected to VCC, OUT1 operates at 1.5 V – This pin is connected to a resistive voltage-divider from OUT1 to GND to adjust the output voltage from 0.7 V to 5.5 V.
12	ILIM1	Positive current sense input for the switching section 1. It is possible to set a threshold voltage that is compared with 1/10th of the GND-PHASE1 drop during the off time.
13	PG1	Power Good output signal for the section 1. This pin is an open drain output and It is pulled down when the output of the switching section 1 is out of +/- 10% of its nominal value.
14	EN1	Enable input for the switching section 1. – If EN1 < 0.8 V the switching section OUT1 is turned off and all faults are cleared. – If EN1 > 2.4 V the switching section OUT1 is turned on. – If EN1 is connected to VREF2, the switching section OUT1 turns on after the switching section OUT2 reaches regulation.
15	HGATE1	High-side gate driver output for section 1.
16	PHASE1	Switch node connection and return path for the high-side driver for the section 1.It is also used as positive and negative current sense input.
17	BOOT1	Bootstrap capacitor connection for the switching section 1. It supplies the high-side gate driver.
18	LGATE1	Low-side gate driver output for the section 1.
19	PVCC	5 V low-side gate drivers supply voltage input. Bypass to PGND with a 1 µF capacitor.

Table 2. Pin descriptions (continued)

N°	Pin	Function
20	CP_FB	The CP_FB is used to monitor the optional external 14 V charge pump. Connect a resistive voltage-divider from 14 V charge pump output to GND. If CP_FB drops below the threshold voltage, the device performs a no audible skip cycle. This charges the charge pump output (driven by LGATE1). Leave CP_FB floating if the charge pump feedback is not needed.
21	GND	Signal ground reference for internal logic circuitry and LDO. It must be connected to the signal ground plan of the power supply and to the exposed pad. The signal ground plan and the power ground plan must be connected together in one point near the PGND pin.
22	PGND	Power ground. This pin must be connected to the power ground plan of the power supply.
23	LGATE2	Low-side gate driver output for the section 2.
24	BOOT2	Bootstrap capacitor connection for the switching section 2. It supplies the high-side gate driver.
25	PHASE2	Switch node connection and return path for the high-side driver for the section 2. It is also used as positive and negative current sense input.
26	HGATE2	High-side gate driver output for section 2.
27	EN2	Enable input for the switching section 2. – If EN2 < 0.8 V the switching section OUT2 is turned off and all faults are cleared. – If EN2 > 2.4 V the switching section OUT2 is turned on. If EN2 is connected to VREF2, the switching section OUT2 turns on after the switching section OUT1 reaches regulation.
28	PG2	Power Good output signal for the section 2. This pin is an open drain output and It is pulled down when the output of the switching section 2 is out of + 14% / - 10% of its nominal value.
29	SKIP	Pulse skipping mode control input. – If the pin is connected to VCC the PWM mode is enabled. – If the pin is connected to GND, the pulse skip mode is enabled. – If the pin is connected to VREF2 (or floating) the pulse skip mode is enabled but and the switching frequency is kept higher than 33 kHz (No-audible pulse skip mode).
30	OUT2	Output voltage sense for the switching section 2.This pin must be directly connected to the output voltage of the switching section. It provides also the feedback for the switching section 2 when REFIN2 is tied to VREF3/VCC.
31	ILIM2	Positive current sense input for the switching section 2. It is possible to set a threshold voltage that is compared with 1/10th of the GND-PHASE2 drop during the off time.
32	REFIN2	Feedback input for the switching section 2: – If this pin is connected to VCC, OUT2 operates at 3.3 V – If this pin is connected to VREF3, OUT2 operates at 1.05 V – If this pin is connected to an external reference from 0.7 V to 2.5 V, OUT2 works in tracking with this reference. Bypass REFIN2 to GND with a 100 nF capacitor.

3 Electrical data

3.1 Maximum rating

Table 3. Absolute maximum ratings

Parameter	Value	Unit
VIN to PGND	-0.3 to 38	V
PHASEx to PGND	-0.3 to 38	V
BOOTx to PHASEx	-0.3 to 6	V
PVCC to PGND	-0.3 to 6	V
HGATEx to PHASEx	-0.3 to BOOTx +0.3	V
LGATEx, CP_FB to PGND	-0.3 to PVCC +0.3	V
VCC, ENx, SKIP, PGx, LDO, REFIN2, OUTx, VREF3, LDOREFIN, LDO_SW, TON to GND	-0.3 to 6	V
FB1, ILIMx to GND	-0.3 to VCC+0.3	V
EN_LDO to GND	-0.3 to 7	V
VREF2 to GND	-0.3 to VREF3+0.3	V
PGND to GND	-0.3 to +0.3	V
Power dissipation at T_A = 25 °C	2	W
Maximum withstanding voltage range test condition: CDF-AEC-Q100-002- “human body model” acceptance criteria: “normal performance”	±1250	V

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	35	°C/W
T_J	Junction operating temperature range	-40 to 125	°C
T_{STG}	Storage temperature range	-50 to 150	°C
T_A	Operating ambient temperature range	-40 to 85	°C

4 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
VIN	Input voltage range, LDO = 5 V in regulation	5.5	-	28	V
VCC	VCC operative voltage range	4.5	-	5.5	V
REFIN2	REFIN2 voltage range with OUT2 in adjustable mode, VIN = 5.5 V to 28 V	0.7	-	2.5	V
OUT1	OUT1 output voltage range	0.70	-	5.50	V
ILIM	ILIM voltage range	0.2	-	2	V
LDOREFIN	LDOREFIN setting with LDO = 2 x LDOREFIN (adjustable mode)	0.35	-	2.25	V
LDO DC output current (switchover function enabled)	VIN = 5.5 V to 28 V, LDO_SW = 5 V, LDOREFIN = GND		-	200	mA
	VIN = 5.5 V to 28 V, LDO_SW = 3.3 V, LDOREFIN = VCC		-	100	mA
LDO DC output current (switchover function disabled)	VIN = 5.5 V to 28 V, LDO_SW = 0 V, LDOREFIN = GND, VCC		-	100	mA

5 Electrical characteristics

VIN = 12 V, no load on LDO, OUT1, OUT2, VREF3, and VREF2. EN2 = EN1 = VCC, LDO_SW = 5 V, PVCC = 5 V, EN_LDO = 5 V, T_J = 25 °C unless otherwise specified)

Table 6. Electrical characteristics

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
Switching controller output accuracy							
OUT2	Output voltage	VIN = 5.5 V to 28 V, REFIN2 = VCC, SKIP = VCC		3.25	3.330	3.397	V
		VIN = 5.5 V to 28 V, REFIN2 = VREF3, SKIP = VCC		1.038	1.05	1.062	V
OUT1	Output voltage	VIN = 5.5 V to 28 V, FB1 = VCC, SKIP = VCC		1.482	1.500	1.518	V
		VIN = 5.5 V to 28 V, FB1 = GND, SKIP = VCC		4.975	5.050	5.125	V
FB1	Feedback accuracy with OUT1 in adjustable mode	VIN = 5.5 V to 28 V, SKIP = VCC		0.693	0.700	0.707	V
REFIN2	Accuracy referred to REFIN2	REFIN2 = 0.7 V to 2.5 V, SKIP = VCC		-1		1	%
Current limit and zero crossing comparator							
ILIM	ILIM bias current	T_A = +25 °C.		4.5	5	5.5	µA
	Positive current limit threshold	Adjustable, VILIM = 0.5 V, GND-PHASE		35	50	65	mV
		Adjustable, VILIM = 1 V or VCC, GND-PHASE		85	100	115	mV
		Adjustable, VILIM = 2 V, GND-PHASE		180	200	220	mV
	Zero crossing current threshold	SKIP = GND, VREF2, or OPEN, GND-PHASE		-1		+11	mV
Switching frequency							
	On-time pulse width	OUT1 = 5.125 V	TON = GND or VREF2	0.908	1.068	1.228	µs
			TON = VCC	1.815	2.135	2.455	
		OUT2 = 3.368 V	TON = GND	0.477	0.561	0.655	
			TON = VCC or VREF2	0.796	0.936	1.076	
	Minimum Off-time				350	472	
	No-audible skip mode operating frequency	SKIP = VREF2(or OPEN)		25	33		kHz
Soft-start and soft-end							
	Soft-start ramp time			2		4	ms

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Linear regulator and reference						
LDO	LDO output voltage	LDO_SW = GND, 5.5 V < VIN < 28 V, LDOREFIN < 0.3 V, 0 < ILDO < 100 mA	4.925	5.000	5.075	V
		LDO_SW = GND, 5.5 V < VIN < 28 V, LDOREFIN = VREF3, 0 < ILDO < 100 mA	3.250	3.300	3.350	V
	LDO accuracy in adjustable mode	VIN = 5.5 V to 28 V, LDOREFIN = 0.35 V to 2.25 V, no load	-2.5		+2.5	%
	LDO short circuit current (linear regulator enabled)	LDO = 4.3 V, LDO_SW = GND	260	320	380	mA
LDO_SW	LDO_SW switch on threshold	LDO = 5 V, rising edge of LDO_SW, LDOREFIN = GND	4.64	4.75	4.84	V
LDO_SW	LDO_SW hysteresis	LDO = 5 V, falling edge of LDO_SW, LDOREFIN = GND		200	400	mV
	LDO_SW switch resistance	LDO = 5 V, rising edge of LDO_SW, LDOREFIN = GND, output current = 200 mA		0.81	1.275	Ω
VREF3	VREF3 output voltage	No load	3.235	3.300	3.365	V
	VREF3 current limit	VREF3 = GND		22	30	mA
VREF2	VREF2 output voltage	No load	1.980	2.000	2.02	V
	VREF2 load regulation	0 < Load < 50 µA		6		mV
	VREF2 sink current	VREF2 > 2.030 V	10			µA
	VIN shutdown current	EN1 and EN2 low, EN_LDO low		49	70	µA
	VIN standby current	EN1 and EN2 low, EN_LDO high, LDOREFIN = GND		132	180	µA
	Operating power consumption (VCC and VIN pins consumption)	Switching regulators on, FB1 = SKIP = GND, REFIN2 = VCC, LDOREFIN = GND, OUT1 = LDO_SW = 5.3V, OUT2 = 3.5 V		4,3	6,5	mW
Fault management						
	PVCC UVLO threshold	Rising edge of PVCC		4.33		V
		Falling edge of PVCC		4		V
	Overvoltage trip threshold	Referred to FB1 nominal regulation point		+11		%
		Referred to REFIN2 nominal regulation point. worst case:REFIN2 = 0.7 V		+14		%
	PG threshold	Lower threshold	-13	-10	-7	%
	PG low voltage	ISink = 4 mA	159	235	405	mV
	PG leakage current	PG = 5 V			1	µA

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
	Output undervoltage shutdown threshold	Referred to FB1, REFIN2 nominal regulation point	67	70	73	%
Inputs and outputs						
FB1	FB1 logic level	fixed OUT1 = 5 V			0.528	V
		fixed OUT1 = 1.5 V	4.1			V
REFIN2	REFIN2 logic level	fixed OUT2 = 1.05 V, VCC = 5 V		VREF3		V
		fixed OUT 2= 3.3 V, VCC = 5 V	VCC-0.838			V
LDOREFIN	LDOREFIN logic level	fixed LDO = 5 V			0.4	V
		fixed LDO = 3.3 V	2.43			V
SKIP	SKIP logic level	Pulse skip mode			0.8	V
		No audible skip mode (VREF2 or floating)		VREF2		V
		PWM mode	2.4			V
TON	TON logic level	Low level			0.8	V
		Middle level		VREF2		V
		High level	2.4			V
EN1,2	EN level	Switching regulators off level			0.8	V
		Delay start level		VREF2		V
		Switching regulators on level	2.4			V
EN_LDO	EN_LDO level	Linear regulator off level	0.905	1.00	1.050	V
		Linear regulator on level	1.500	1.6	1.650	V
	Input leakage current	FB1 = 0.7 V	-1		+1	µA
		REFIN2 = 2.5 V		12		
Internal bootstrap diode						
	Diode forward voltage	PVCC = -BOOT, Idiode = 10 mA		0.2		V
	Diode Leakage current	BOOT= 30 V, PHASE = 28 V, PVCC = 5 V			500	nA
High-side and low-side gate drivers						
	HGATE driver on-resistance	HGATEx high state (pull-up) Isource = 100 mA		1.8		Ω
		HGATEx low state (pull-down) Isink = 100 mA		1.3	1.9	
	LGATE driver on-resistance	LGATEx high state (pull-up) Isource = 100 mA		1.3		
		LGATEx low state (pull-down) Isink = 100 mA		0.6	0.8	

6 Typical operating characteristics

(T_{ON} = VCC (200 / 300 kHz), SKIP = GND (skip mode), LDOREFIN = SGND (LDO = 5 V), LDO_SW = OUT1, PVCC connected to LDO, V_{IN} = 12 V, EN1-EN2-EN_LDO are high, no load unless specified). Measures performed on the demonstration kit (PM6686_SYSTEM and PM6686_CHIPSET)

Efficiency traces: Green: VIN = 7 V, red: VIN = 12 V, blue: VIN = 19 V.

Figure 3. Efficiency vs load OUT1 = 5 V, T_{ON} = VCC

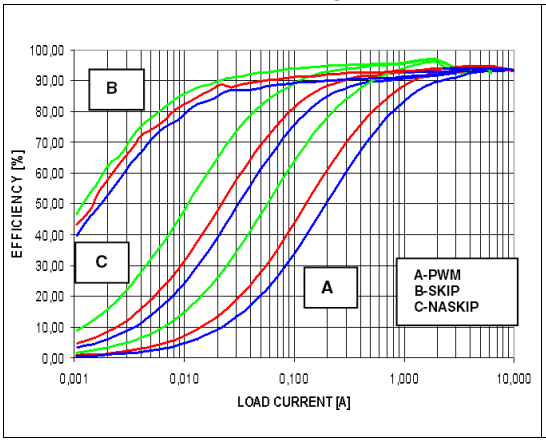


Figure 4. Efficiency vs load OUT2 = 3.3 V, T_{ON} = VCC

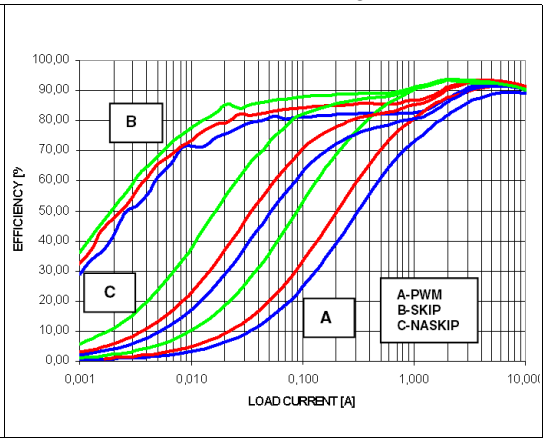


Figure 5. Efficiency vs load OUT1 = 1.5 V, T_{ON} = VCC

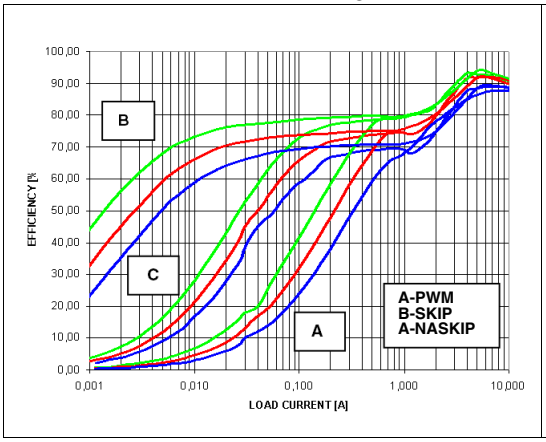


Figure 6. Efficiency vs load OUT2 = 1.05 V, T_{ON} = VCC

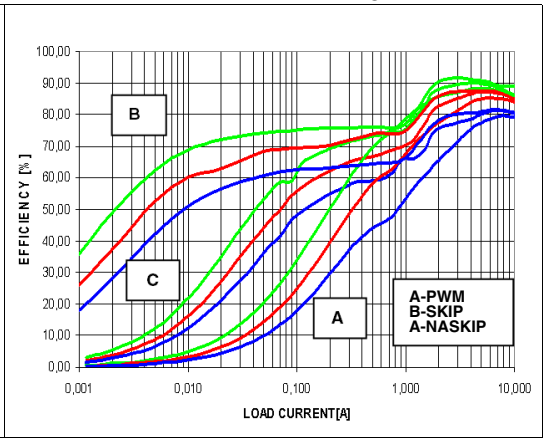


Figure 7. Load regulation OUT1 = 5 V, T_{ON} = VCC

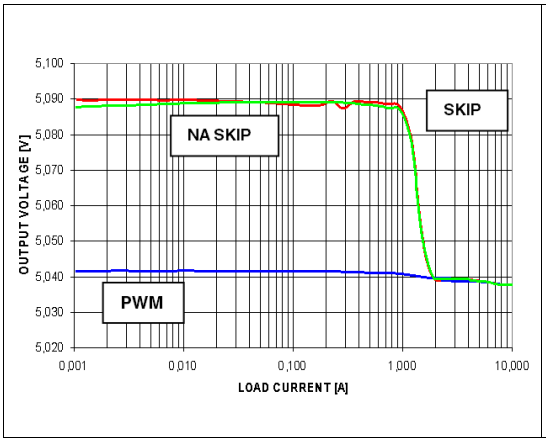


Figure 8. Load regulation OUT2 = 3.3 V, T_{ON} = VCC

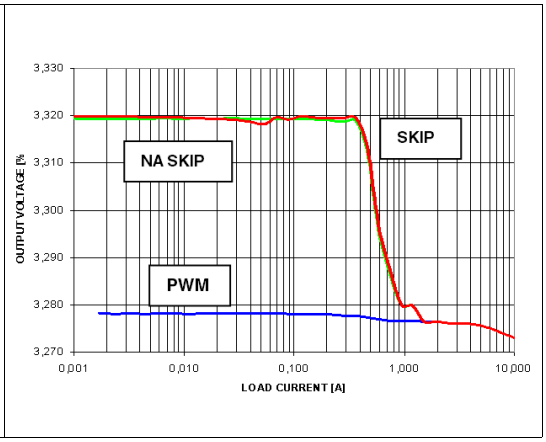


Figure 9. Load regulation OUT1 = 1.5 V, T_{ON} = VCC

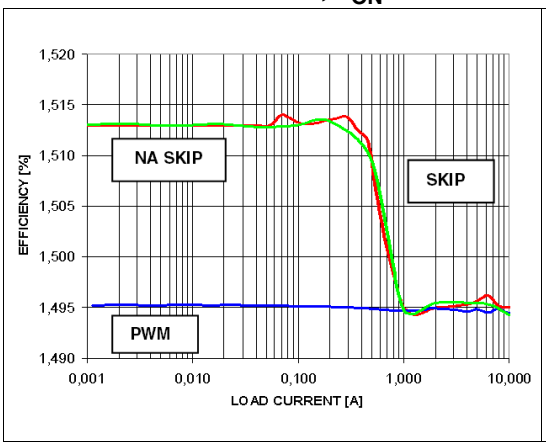


Figure 10. Load regulation OUT2 = 1.05 V, T_{ON} = VCC

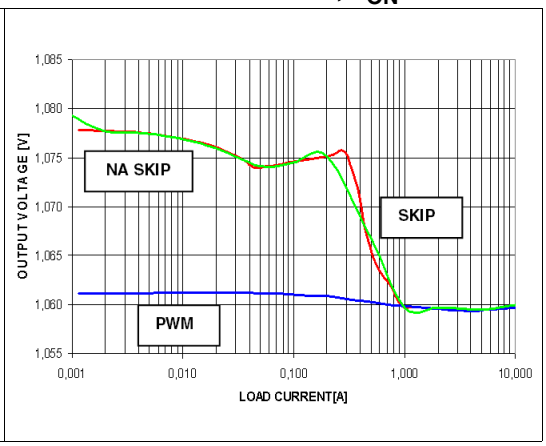


Figure 11. Switching frequency vs load OUT1 = 5 V, T_{ON} = VCC

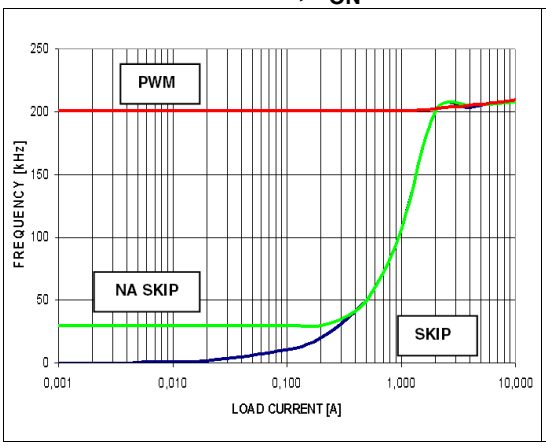


Figure 12. Switching frequency vs load OUT2 = 3.3 V, T_{ON} = VCC

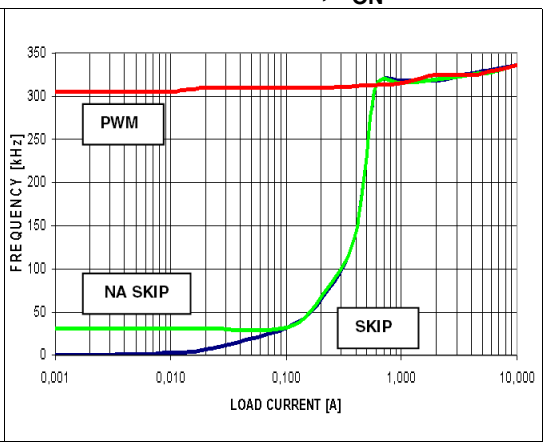


Figure 13. Section 1 line regulation OUT1 = 5 V, T_{ON} = VCC

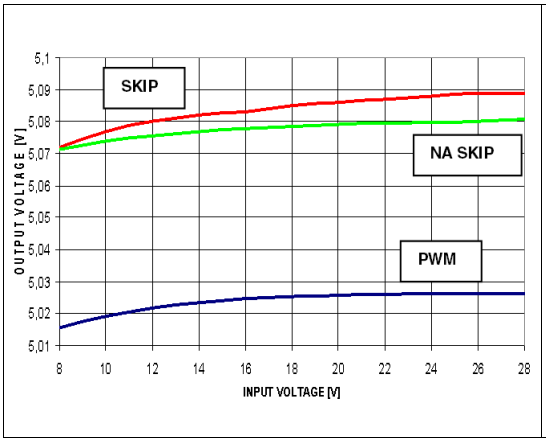


Figure 14. Section 2 line regulation OUT2 = 3.3 V, T_{ON} = VCC

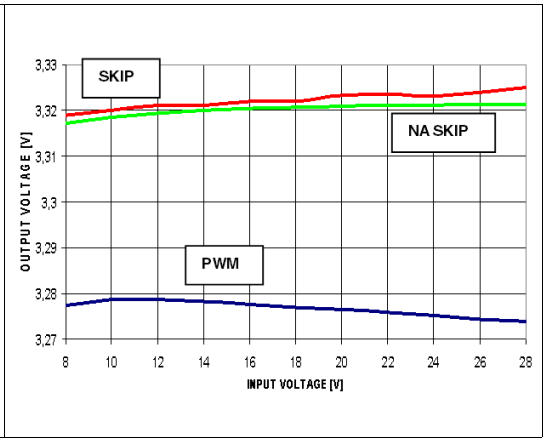


Figure 15. Section 1 line regulation OUT1 = 1,5 V, T_{ON} = VCC

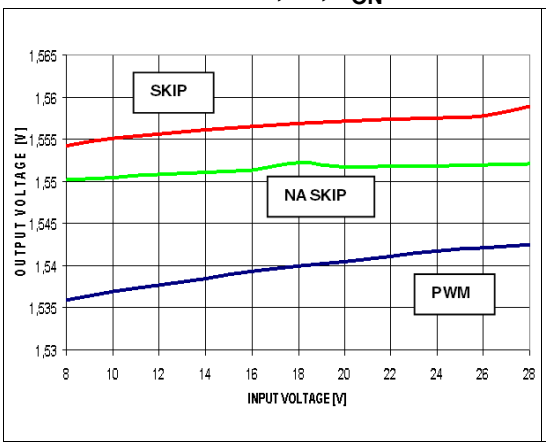


Figure 16. Section 2 line regulation OUT2 = 1,05 V, T_{ON} = VCC

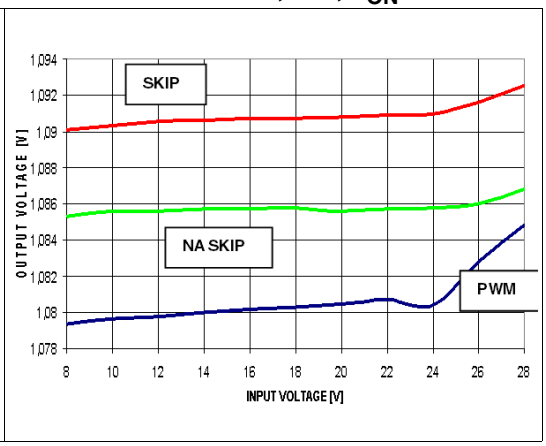


Figure 17. Stand-by mode input battery current vs input voltage

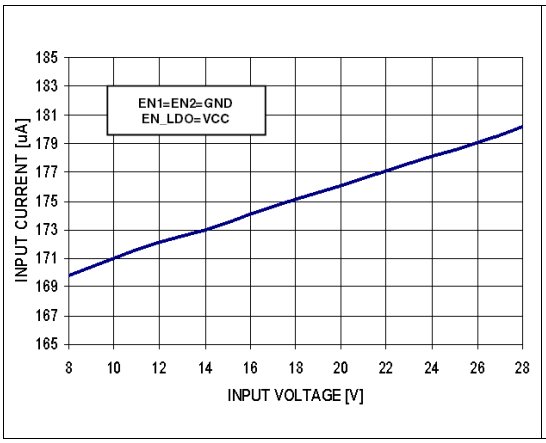


Figure 18. Shut-down mode input battery current vs input voltage

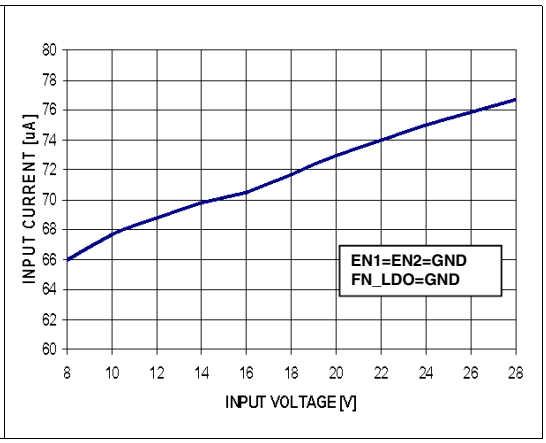


Figure 19. PWM no load input currents vs input voltage

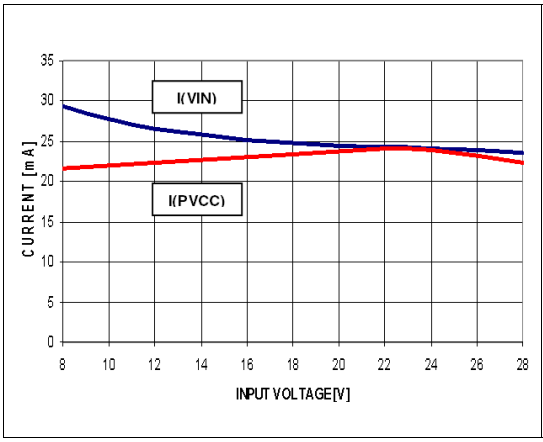


Figure 20. SKIP no load input currents vs input voltage

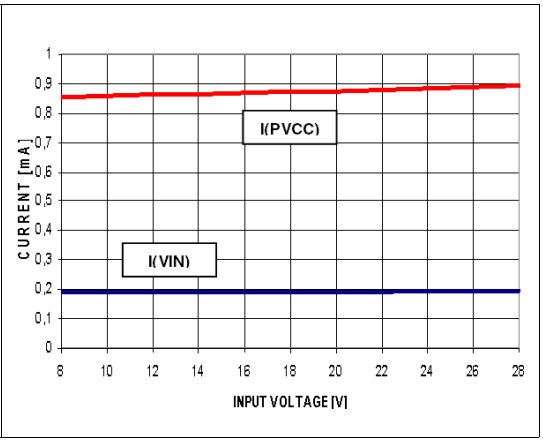


Figure 21. NA SKIP no load input currents vs input voltage

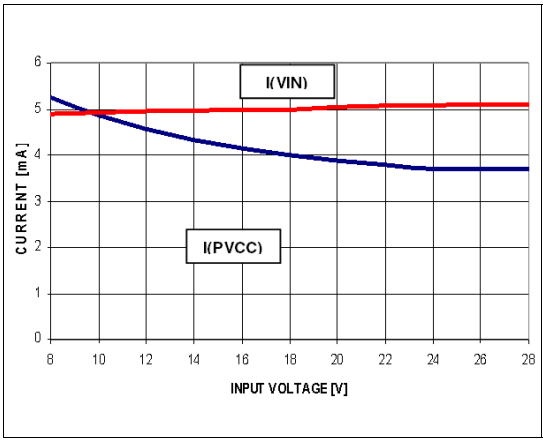


Figure 22. VREF3 load regulation

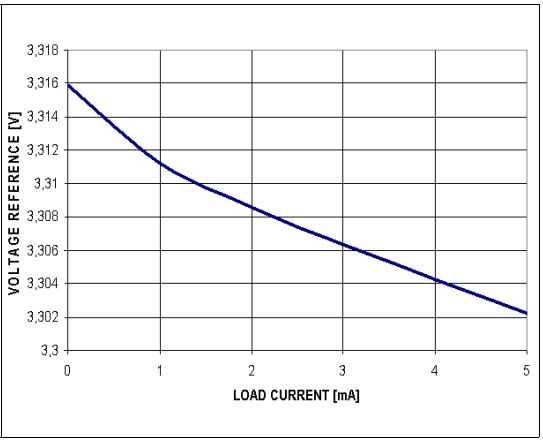


Figure 23. VREF2 load regulation

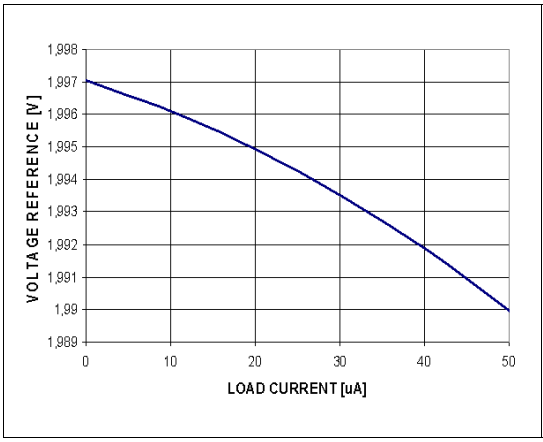


Figure 24. LDO = 3.3 V load regulation

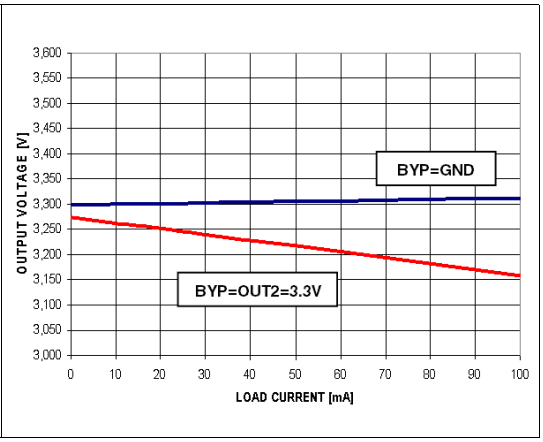
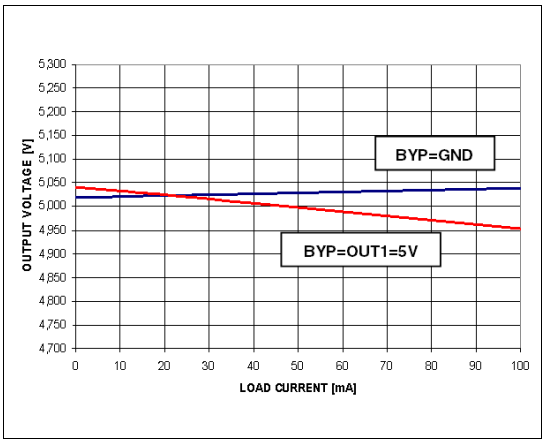


Figure 25. LDO = 5 V load regulation



6.1 Screen shots

Typical operating characteristic (T_{ON} = VCC (200 / 300 kHz), SKIP = GND (skip mode), FB1 = GND (OUT1 = 5 V), REFIN2 = VCC (OUT2 = 3.3 V), LDOREFIN = SGND (LDO = 5 V), CP_FB = floating, LDO_SW = OUT1, PVCC connected to LDO, VIN = 12 V, EN1-EN2-EN_LDO are high, no load unless specified)

Figure 26. OUT1 soft-start no load

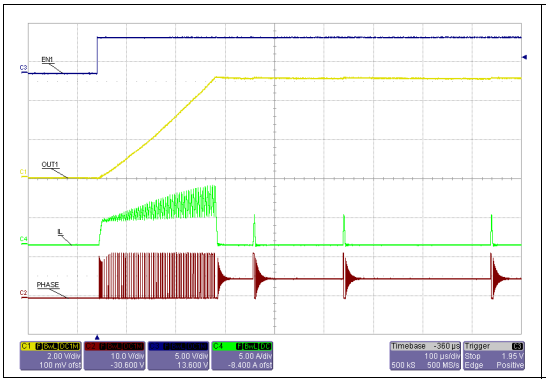


Figure 27. OUT2 soft-start no load

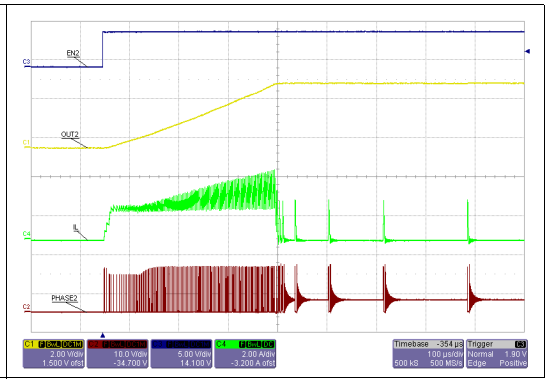


Figure 28. OUT1 soft-start 8 A constant current load

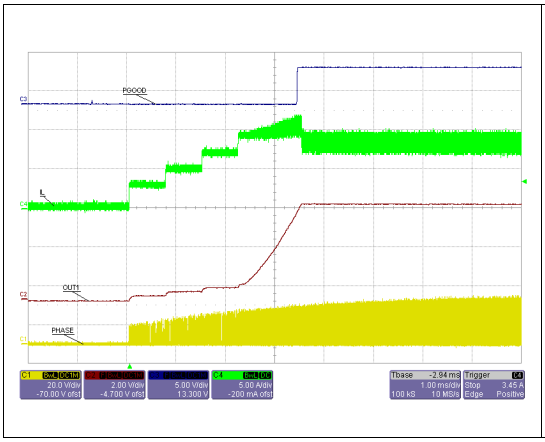


Figure 29. OUT2 soft-start loaded 8 A constant current load

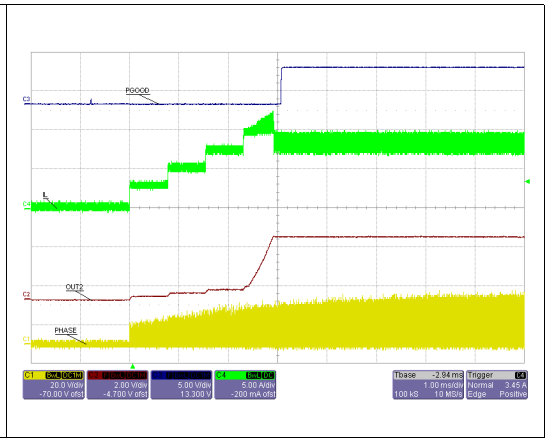


Figure 30. OUT1 soft-end, no load

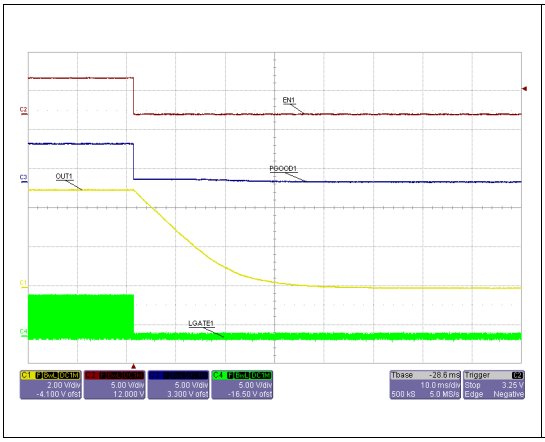


Figure 31. OUT2 soft-end, no load

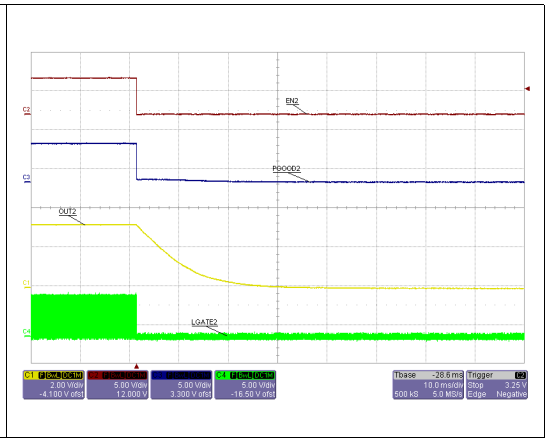


Figure 32. OUT1 soft-start, EN2 = VREF2 no loads applied

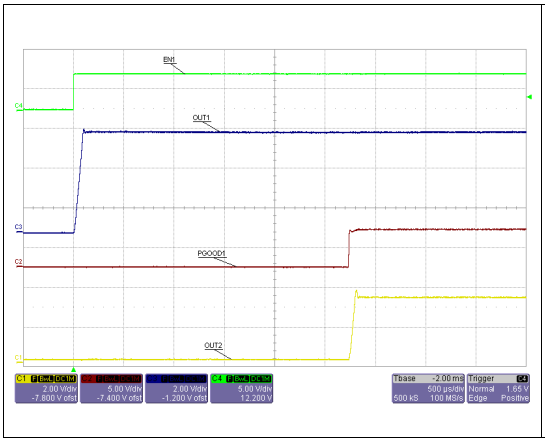


Figure 33. OUT2 soft-start, EN1=VREF2 no loads applied

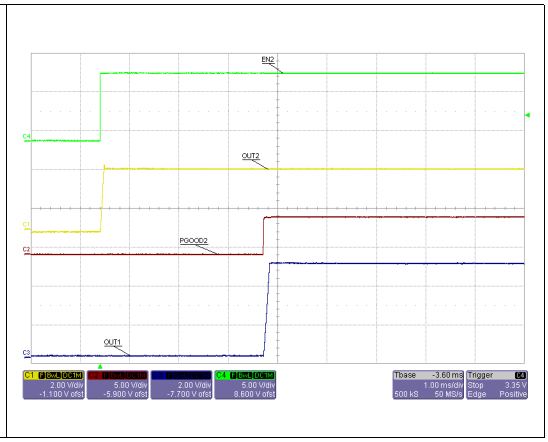


Figure 34. Soft-end, EN2 = VREF2 no loads applied

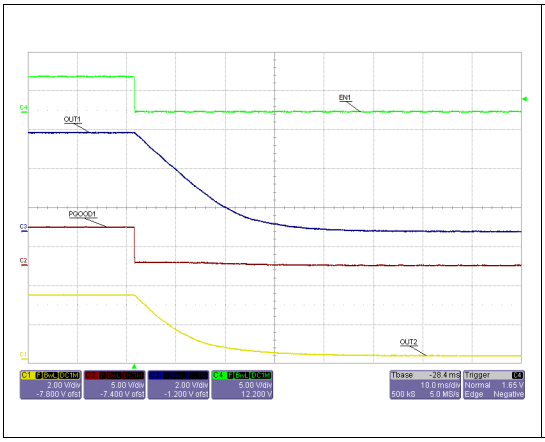


Figure 35. Soft-end, EN1=VREF2 no loads applied

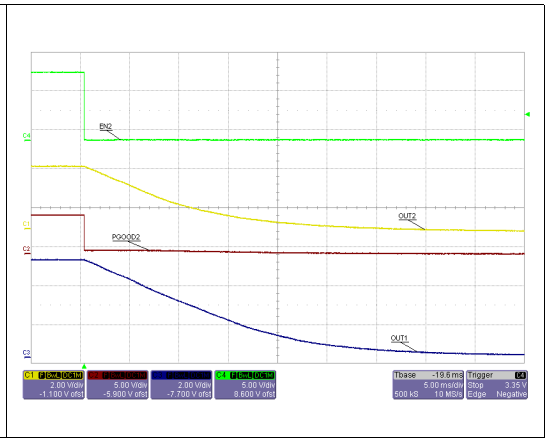


Figure 36. Load transient 0-5 A 2 A/µs OUT1 = 5 V PWM mode

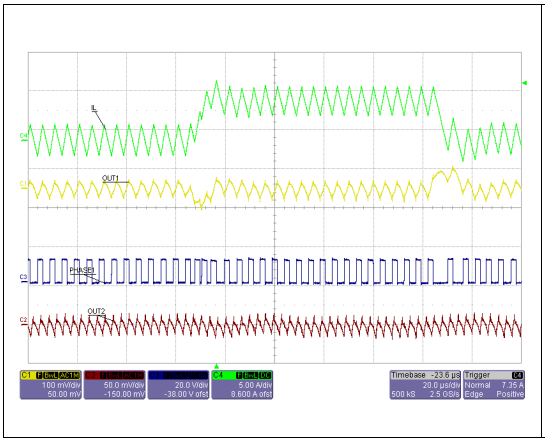


Figure 37. Load transient 0-5 A 2 A/µs OUT1 = 5 V SKIP mode

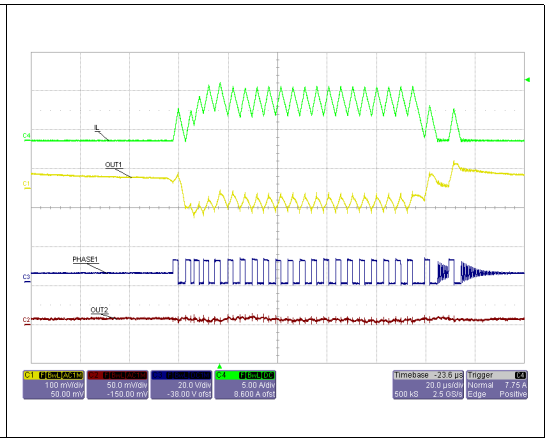


Figure 38. Load transient 0-5 A 2 A/ µs OUT1 = 1.5 V PWM mode

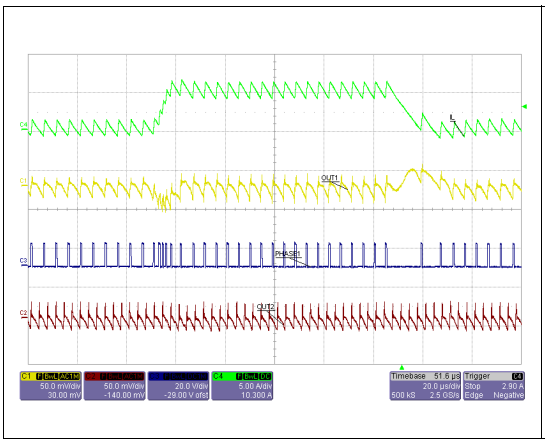


Figure 39. Load transient 0-5 A 2 A/ µs OUT1 = 1.5 V SKIP mode

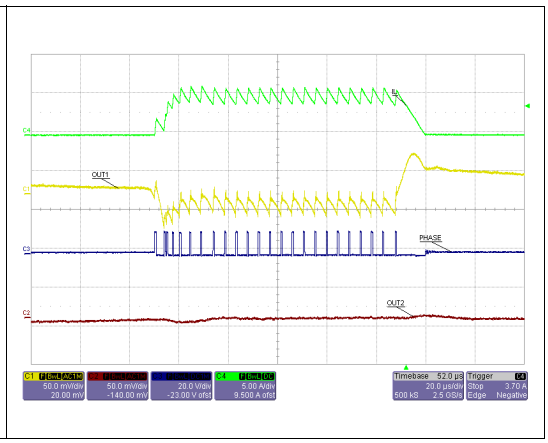


Figure 40. Load transient 0-5 A 2 A/µs OUT2 = 3.3 V PWM mode

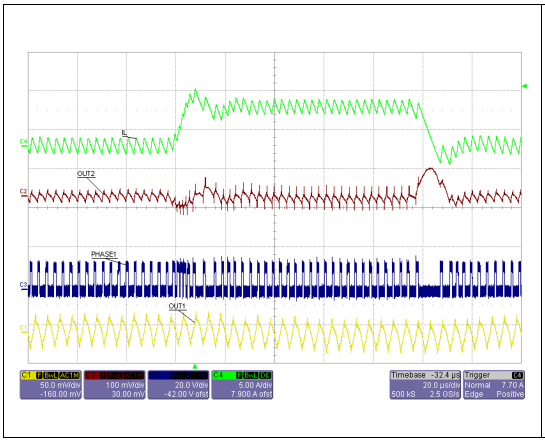


Figure 41. Load transient 0-5 A 2 A/µs OUT2 = 3.3 V SKIP mode

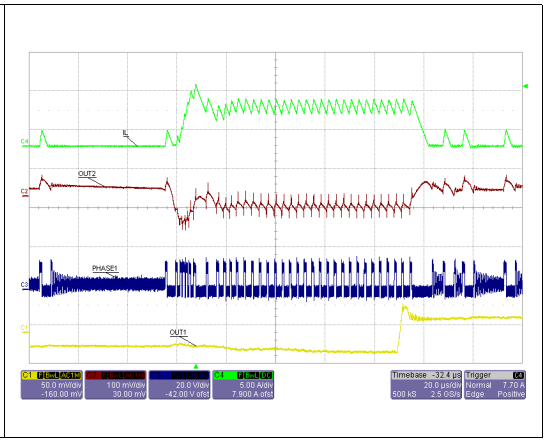


Figure 42. Load transient 0-5 A 2 A/ µs OUT2 = 1.05 V PWM mode

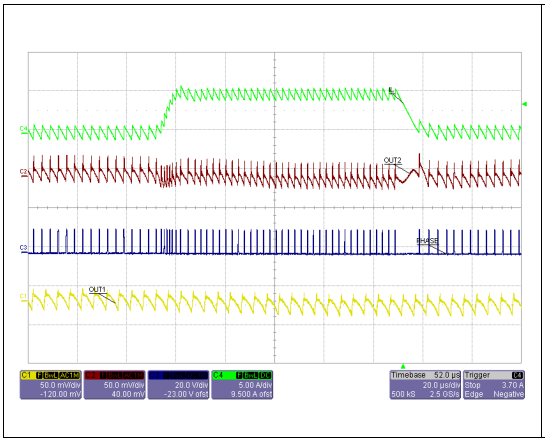
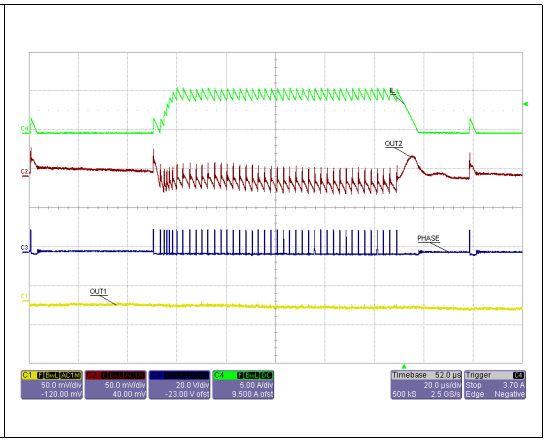
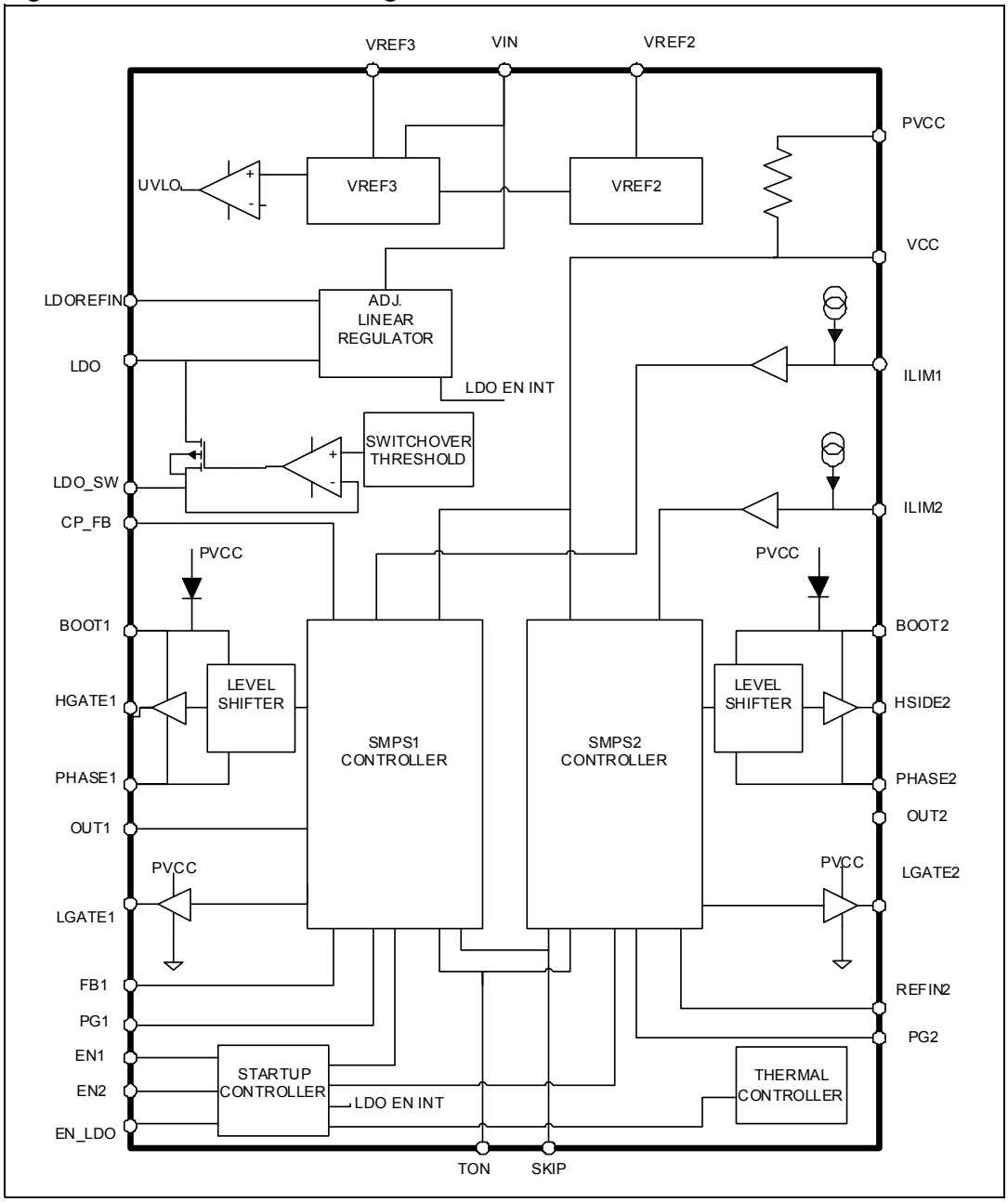


Figure 43. Load transient 0-5 A 2 A/ µs OUT2 = 1.05 V SKIP mode



7 Block diagram

Figure 44. Functional block diagram



8 Device description

The PM6686 is a dual step down controller dedicated to provide logic voltages for notebook computers. It offers several operating configurations: it combines two synchronous buck controllers, an internal linear regulator (LDO), two voltage references and a charge pump controller.

Each buck controller is based on constant on time (COT) architecture. This type of control offers a very fast load transient response with a minimum external components count.

The two switching sections (SMPS) generate two output voltages OUT1 and OUT2 that regulate adjustable voltages. A fixed output voltage configuration can also be selected, reducing further the external components count because no external resistor divider is needed.

In fixed mode, OUT1 provides 5 V or 1.5 V; in adjustable mode OUT1 can regulate an output voltage between 0.7 V and 5.5 V. In fixed mode, OUT2 provides 3.3 V or 1.05 V, in adjustable mode OUT2 can regulate an output between 0.7 V to 2.5 V by tracking an external reference.

The switching frequencies of both switching controllers can be adjusted to 200 kHz/300 kHz, 400 kHz/300 kHz or 400 kHz/500 kHz respectively. To maximize the efficiency at light loads a pulse skipping mode can be selected. Moreover a pulse skipping mode with a minimum switching frequency of 33 kHz (non audible skip operation mode) can be selected to avoid audible noise issue. The linear regulator can provide a fixed (5 V or 3.3 V) or an adjustable output voltage. In order to reduce the power consumption the internal LDO can be turned off and the LDO output can be supplied with an external voltage applied at LDO_SW pin (switch-over function).

The PM6686 supplies two voltage references: 3.3 V and 2 V. The charge pump controller can be programmed to regulate a 14 V output. The switching sections and the LDO have independent enable signals. Moreover the switching sections have a selectable power up sequence and a turn off management.

The device is protected against overvoltage, undervoltage and over temperature. Two independent Power Good signals monitor the output voltage range of each switching sections.

8.1 Switching sections

8.1.1 Output voltage set up

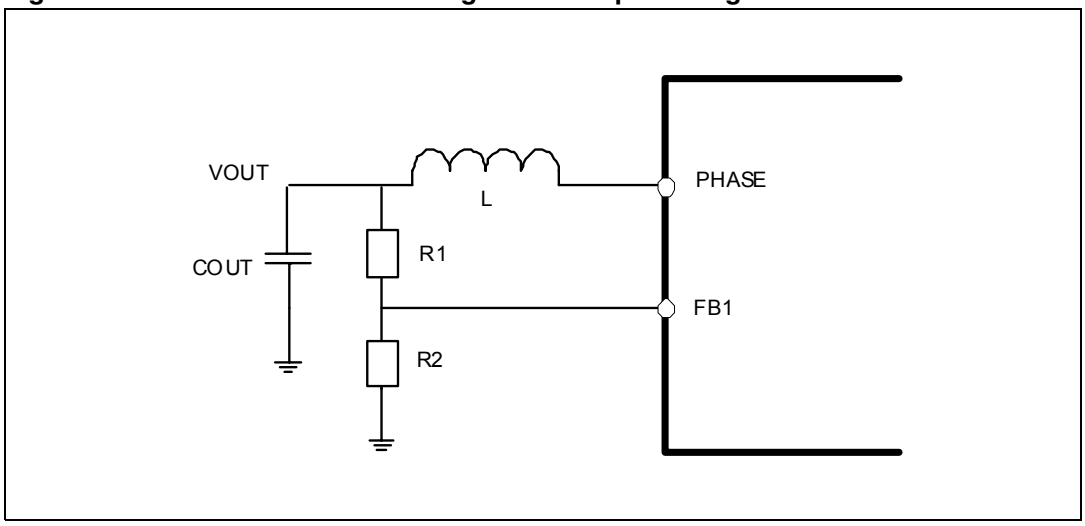
The switching sections can be configured in several ways.

OUT1 output voltage is configured with FB1 pin. If FB1 pin is tied to GND the PM6686 regulates 5 V while if FB1 is connected to VCC the controller set OUT1 at 1.5 V. Using an external resistor divider the output can be adjusted following this equation:

Equation 1

$$V_{OUT1} = 0{,}7V \cdot \left(\frac{R1}{R2} + 1\right)$$

Figure 45. Resistor divider to configure the output voltage



Where R1, R2 are the resistors of the FB1 pin divider, as shown in Figure 2.

OUT2 output voltage is programmed with REFIN2 pin. Fixed output voltage is selected connecting REFIN2 to VREF3 (OUT2 = 1.05 V) or to VCC (OUT2 = 3.3 V).
When the REFIN2 voltage is between 0.7 V and 2.5 V, OUT2 output voltage tracks REFIN2 voltage. When REFIN2 is lower than 0.5 V the section is turned OFF.

Table 7. Switching output voltages configuration

Output	control pin	Control pin connected to	Operation mode	Output voltage
OUT1	FB1	GND	Fixed	5 V
		VCC	Fixed	1.5 V
		Resistor divider	Adj	$V_{OUT1} = 0.7V \cdot \left(\frac{R1}{R2} + 1\right)$
OUT2	REFIN2	VCC	Fixed	3.3 V
		VREF3	Fixed	1.05 V
		Ext source	Tracking	=REFIN2