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PM-7528

DUAL 8-BIT BUFFERED MULTIPLYING CMOS D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- On-Chip Latches For Both DACs
- +5V To +15V Single Supply Operation
- DACs Matched To 1%
- Four-Quadrant Multiplication
- TTL/CMOS Compatible
- 8-Bit Endpoint Linearity ($\pm 1/2$ LSB)
- Full Temperature Operation
- Low Power Consumption
- Microprocessor Compatible
- Improved ESD Resistance
- Automatically Insertable Cerdip and Plastic Packages
- Available in Surface Mount SO, PLCC and LCC Packages

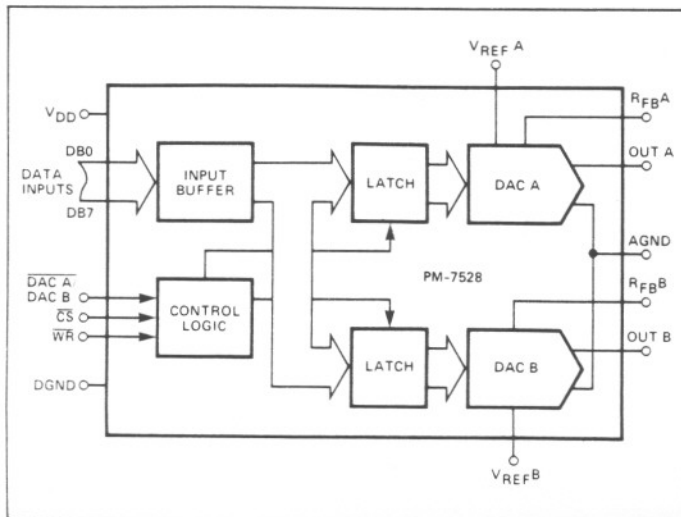
APPLICATIONS

- Digital Gain/Attenuation Control
- Digital Control Of Filter Parameters
- Digitally-Controlled Audio Circuits
- X-Y Graphics
- Digital/Synchro Conversion
- Robotics
- Ideal For Battery-Operated Equipment

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7528AR	AD7528UD	MILITARY
PM7528BR	AD7528TD	
PM7528BR	AD7528SD	
PM7528ER	AD7528CQ	INDUSTRIAL
PM7528FR	AD7528BQ	
PM7528FR	AD7528AQ	
PM7528GP	AD7528LN	COMMERCIAL
PM7528HP	AD7528KN	
PM7528HP	AD7528JN	
PM7528HPC	AD7528KP	
PM7528HPC	AD7528JP	

FUNCTIONAL DIAGRAM



ORDERING INFORMATION†

PACKAGE: 20-PIN				
RELATIVE ACCURACY	GAIN ERROR	MILITARY* TEMPERATURE -55°C TO +125°C	INDUSTRIAL TEMPERATURE -25°C TO +85°C	COMMERCIAL TEMPERATURE 0°C TO +70°C
$\pm 1/2$ LSB	± 1 LSB	PM7528AR	PM7528ER	PM7528GP
$\pm 1/2$ LSB	± 1 LSB	PM7528ARC/883	—	—
$\pm 1/2$ LSB	± 2 LSB	PM7528BR	PM7528FR	PM7528HP
$\pm 1/2$ LSB	± 2 LSB	PM7528BRC/883	—	PM7528HPC††
$\pm 1/2$ LSB	± 2 LSB	—	—	PM7528HS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

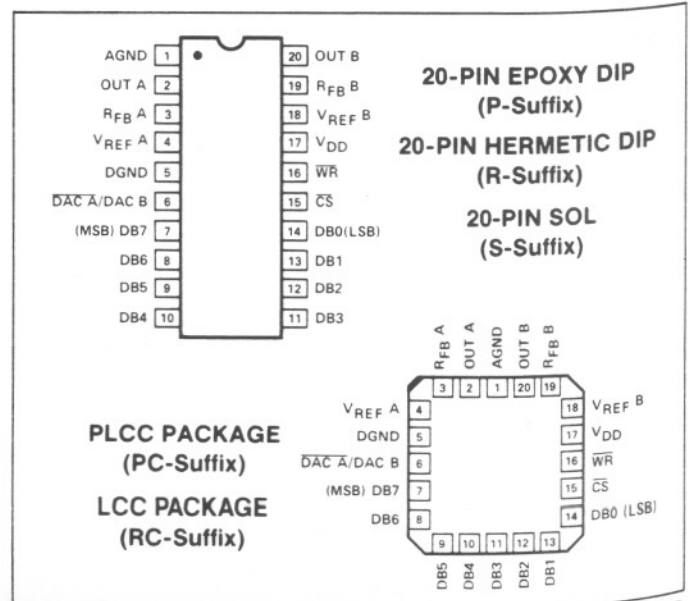
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The PM-7528 contains two 8-bit multiplying digital-to-analog converters. Excellent DAC-to-DAC matching and tracking results from monolithic construction. The PM-7528 consists of two thin-film R-2R resistor-ladder networks, tracking span resistors, two data latches, one input buffer, and control logic. Operation from a 5 to 15 volt single power supply dissipates only 20mW of power in a space saving 20-pin 0.3" wide DIP. The PM-7528 features circuitry designed to protect against damage from electrostatic discharges.

Digital input data is directed into one of the DAC data latches determined by the DAC selection control line DAC A/DAC B. The 8-bit wide input data path provides TTL/CMOS compatibility. The data load cycle is similar to the write cycle of a random access memory. The PM-7528 is bus compatible with most 8-bit microprocessors, including the 6800, 8080, 8085, and Z80.

PIN CONNECTIONS





ABSOLUTE MAXIMUM RATINGS

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
AGND to DGND	0V, V_{DD}
Digital Input Voltage to DGND	-0.3V, +15V
$V_{PIN 2}$, $V_{PIN 20}$ to AGND	-0.3V, +15V
$V_{REF A}$, $V_{REF B}$ to AGND	$\pm 25\text{V}$
$V_{RFB A}$, $V_{RFB B}$ to AGND	$\pm 25\text{V}$
Power Dissipation (Any Package) to $+75^\circ\text{C}$	450mW
Derate Above $+75^\circ\text{C}$ by	6mW/ $^\circ\text{C}$
Operating Temperature Range	
AR, ARC, BR, BRC Versions	-55°C to $+125^\circ\text{C}$
ER, FR Versions	-25°C to $+85^\circ\text{C}$
GP, HP, HPC, HS Versions	0°C to $+70^\circ\text{C}$

Dice Junction Temperature	$+150^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	$+300^\circ\text{C}$

CAUTION:

- Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} .
- The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
- Do not insert this device into powered sockets; remove power before insertion or removal.
- Use proper anti-static handling procedures.
- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5\text{V}$ or $+15\text{V}$, $V_{REF A} = V_{REF B} = +10\text{V}$, $\text{OUT A} = \text{OUT B} = 0\text{V}$; $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ apply for PM-7528AR/ARC/BR/BRC; $T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$ apply for PM-7528ER/FR; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ apply for PM-7528GP/HP/HPC/HS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7528			UNITS	
			MIN	TYP	MAX		
STATIC ACCURACY (Note 1)							
Resolution	N		8	—	—	Bits	
Relative Accuracy (Note 2)	NL		—	—	$\pm 1/2$	LSB	
Differential Nonlinearity (Note 3)	DNL		—	—	± 1	LSB	
Full Scale Gain Error (Note 4)	G_{FSE}	$T_A = +25^\circ\text{C}$			± 1	LSB	
			PM7528A/E/G	—	—		± 1
			PM7528B/F/H	—	—		± 2
		$V_{DD} = +5\text{V}$	PM7528A/E/G	—	—		± 3
		$T_A = \text{Full Temp. Range}$	PM7528B/F/H	—	—	± 4	
		$V_{DD} = +15\text{V}$	PM7528A/E/G	—	—	± 1	
		$T_A = \text{Full Temp. Range}$	PM7528B/F/H	—	—	± 3	
Gain Temperature Coefficient ($\Delta\text{Gain}/\Delta\text{Temperature}$) (Notes 4, 10)	TCG_{FS}	$V_{DD} = +5\text{V}$	—	—	± 0.007	$\%/^\circ\text{C}$	
		$V_{DD} = +15\text{V}$	—	—	$+0.0035$		
Output Leakage Current Out A (Pin 2)/Out B (Pin 20) (Note 5)	I_{LKG}	$T_A = +25^\circ\text{C}$	—	5	± 50	nA	
		$V_{DD} = +5\text{V}$	—	—	± 400		
		$T_A = \text{Full Temp. Range}$	—	—	± 400		
		$V_{DD} = +15\text{V}$	—	—	$+200$		
		$T_A = \text{Full Temp. Range}$	—	—	$+200$		
Input Resistance ($V_{REF A}$, $V_{REF B}$) (Note 6)	R_{REF}		8	—	15	k Ω	
$V_{REF A}/V_{REF B}$ (Input Resistance Match)	$\Delta V_{REF A, B}$		—	0.1	± 1	%	



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$, $V_{REF A} = V_{REF B} = +10V$, $OUT A = OUT B = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7528AR/ARC/BR/BRC; $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7528ER/FR; $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7528GP/HP/HPC/HS, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7528			UNITS
			MIN	TYP	MAX	
DIGITAL INPUTS (Note 9)						
Digital Input High (Note 8)	V_{INH}	$V_{DD} = +5V$ $V_{DD} = +15V$	2.4 13.5	— —	— —	V
Digital Input Low (Note 8)	V_{INL}	$V_{DD} = +5V$ $V_{DD} = +15V$	— —	— —	0.8 1.5	V
Input Current (Note 7)	I_{IN}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	— —	.001 —	± 1 ± 10	μA
Input Capacitance (Note 10)	C_{IN}	DB0-DB7 WR, CS, DAC A/DAC B	— —	— —	10 15	pF
SWITCHING CHARACTERISTICS at $V_{DD} = +5V$ (Notes 10, 11)						
Chip Select to Write Set-Up Time	t_{CS}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	200 230	— —	— —	ns
Chip Select to Write Hold Time	t_{CH}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	20 30	— —	— —	ns
DAC Select to Write Set-Up Time	t_{AS}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	200 230	— —	— —	ns
DAC Select to Write Hold Time	t_{AH}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	20 30	— —	— —	ns
Data Valid to Write Set-Up Time	t_{DS}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	110 130	— —	— —	ns
Data Valid to Write Hold Time	t_{DH}		0	—	—	ns
Write Pulse Width	t_{WR}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	180 200	— —	— —	ns
SWITCHING CHARACTERISTICS at $V_{DD} = +15V$ (Notes 10, 11)						
Chip Select to Write Set-Up Time	t_{CS}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	60 80	— —	— —	ns
Chip Select to Write Hold Time	t_{CH}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	10 15	— —	— —	ns
DAC Select to Write Set-Up Time	t_{AS}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	60 80	— —	— —	ns
DAC Select to Write Hold Time	t_{AH}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	10 15	— —	— —	ns
Data Valid to Write Set-Up Time	t_{DS}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	50 70	— —	— —	ns
Data Valid to Write Hold Time	t_{DH}		10	—	—	ns
Write Pulse Width	t_{WR}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	60 80	— —	— —	ns



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$, $V_{REF A} = V_{REF B} = +10V$, $OUT A = OUT B = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7528AR/ARC/BR/BRC; $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7528ER/FR; $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7528GP/HP/HPC/HS, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7528			UNITS
			MIN	TYP	MAX	
POWER SUPPLY (Note 12)						
Supply Current (Note 21)	I_{DD}	All Digital Inputs V_{INL} or V_{INH}	—	—	1	mA
		All Digital Inputs $0V$ or V_{DD}	—	—	100	μA
AC PERFORMANCE CHARACTERISTICS (Note 13)						
DC Supply Rejection Ratio ($\Delta Gain / \Delta V_{DD}$) (Note 14)	PSRR	$V_{DD} = +5V$	—	—	0.02	%/%
		$T_A = +25^\circ C$	—	—	0.04	
		$T_A = \text{Full Temp. Range}$	—	—	0.01	
		$V_{DD} = +15V$	—	—	0.02	
Propagation Delay (Notes 15, 16, 17)	t_{PD}	$V_{DD} = +5V$	—	—	220	ns
		$T_A = +25^\circ C$	—	—	270	
		$T_A = \text{Full Temp. Range}$	—	—	80	
		$V_{DD} = +15V$	—	—	100	
Current Settling Time (Notes 16, 17, 22)	t_s	$V_{DD} = +5V$	—	—	350	ns
		$T_A = +25^\circ C$	—	—	400	
		$T_A = \text{Full Temp. Range}$	—	—	180	
		$V_{DD} = +15V$	—	—	200	
Digital Charge Injection (Note 18)	Q	$T_A = +25^\circ C$	—	160	—	nVs
		$V_{DD} = +5V$	—	440	—	
		$V_{DD} = +15V$	—	—	—	
Output Capacitance	$C_{OUT A}$	DAC Latches Loaded	—	—	50	pF
	$C_{OUT B}$	with 00000000	—	—	50	
	$C_{OUT A}$	DAC Latches Loaded	—	—	120	
	$C_{OUT B}$	with 11111111	—	—	120	
AC Feedthrough (Note 19)	FT_A	$V_{REF A}$ to $OUT A$;	—	—	-70	dB
		$T_A = +25^\circ C$	—	—	-65	
	FT_B	$V_{REF B}$ to $OUT B$;	—	—	-70	
		$T_A = +25^\circ C$	—	—	-65	
		$T_A = \text{Full Temp. Range}$	—	—	—	



PM-7528 DUAL 8-BIT BUFFERED MULTIPLYING CMOS D/A CONVERTER

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$, $V_{REF A} = V_{REF B} = +10V$, $OUT A = OUT B = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7528AR/ARC/BR/BRC; $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7528ER/FR; $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7528GP/HP/HPC/HS, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7528			UNITS
			MIN	TYP	MAX	
AC PERFORMANCE CHARACTERISTICS						
(Note 13)						
Channel-to-Channel Isolation (Note 20)	CCI_{BA}	$V_{REF A}$ to OUT B; $V_{REF A} = 20V_{p-p}$ Sinewave @ $f = 100kHz$ $V_{REF B} = 0V$. $T_A = +25^\circ C$	—	-77	—	dB
	CCI_{AB}	$V_{REF B}$ to OUT A; $V_{REF B} = 20V_{p-p}$ Sinewave @ $f = 100kHz$ $V_{REF A} = 0V$. $T_A = +25^\circ C$	—	-77	—	
Digital Crosstalk	Q	For Code Transition From 00000000 to 11111111. $T_A = +25^\circ C$ $V_{DD} = +5V$ $V_{DD} = +15V$	—	30 60	—	nVs
Harmonic Distortion	THD	$V_{IN} = 6V_{rms}$ @ $f = 1kHz$. $T_A = +25^\circ C$	—	-85	—	dB

NOTES:

- Specifications apply to both DAC A and DAC B.
- This is an endpoint linearity specification.
- All grades guaranteed to be monotonic over the full operating temperature range.
- Measured using internal $R_{FB A}$ and $R_{FB B}$. Both DAC latches loaded with 11111111. Gain error is adjustable using circuits of Figures 5 and 6.
- DAC loaded with 00000000.
- Input resistance $TC = +50ppm/^\circ C$; typical input resistance = $11k\Omega$.
- $V_{IN} = 0V$ or V_{DD} .
- For all data bits DB0-DB7, \overline{WR} , \overline{CS} , $\overline{DAC A/DAC B}$.
- Logic inputs are MOS gates. Typical input current ($+25^\circ C$) is less than $1nA$.
- Guaranteed and not tested.
- See timing diagram.
- See Figure 3.
- These characteristics are for design guidance only and are not subject to test.
- $\Delta V_{DD} = \pm 5\%$.
- From digital input to 90% of final analog-output current.
- $V_{REF A} = V_{REF B} = +10V$; $OUT A$, $OUT B$ load = 100Ω , $C_{EXT} = 13pF$.
- \overline{WR} , $\overline{CS} = 0V$, $DB0-DB7 = 0V$ to V_{DD} or V_{DD} to $0V$.
- For code transition 00000000 to 11111111.
- $V_{REF A}$, $V_{REF B} = 20V_{p-p}$ Sinewave @ $f = 100kHz$.
- Both DAC latches loaded with 11111111.
- $I_{DD} = 500\mu A$ at $T_A =$ Full Temp. Range.
- Extrapolated: t_s (1/2 LSB) = $t_p D + 6.2\tau$, where τ = the measured first time constant of the final RC decay.