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PM8800A

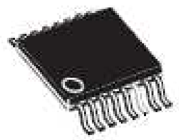
Integrated IEEE 802.3af compliant PoE-PD interface and PWM controller with support of external source

Features

- IEEE 802.3af compliant PD interface
- Works with power supplied from Ethernet LAN cables or from local auxiliary sources
- Integrated 100 V, 0.5 Ω, 800 mA hot-swap MOSFET
- Integrated signature resistor
- Programmable in-rush current limit
- Programmable classification current
- Programmable DC current limit up to 800 mA
- High voltage start-up bias regulator
- Thermal shutdown protection
- Current mode pulse width modulator
- Programmable oscillator frequency
- Programmable soft-start
- Power good indication
- 80 % maximum duty cycle with internal slope compensation
- Supports both isolated and non-isolated Applications.
- HTSSOP16 package

Applications

- VoIP phones, WLAN access points
- Security cameras
- PoE powered device appliances
- High power (>12.95 W) powered devices



HTSSOP16

Description

The PM8800A integrates a standard power over Ethernet (PoE) interface and a current mode PWM controller to simplify the design of the power supply sections of all powered devices.

The PoE interface incorporates all the functions required by the IEEE 802.3af including detection, classification, under-voltage lockout (UVLO) and in-rush current limitation.

PM8800A specifically targets PD with extended power requirement with respect to the limit imposed by the 802.3af standard, embedding a hot-swap MOSFET capable of sustaining twice the current of the 802.3af standard with a programmable DC current limit.

The integrated switching regulator has been designed to work with power either form the Ethernet cable connection or from an external power source such as AC adapter.

The DC-DC section of the PM8800A features a programmable oscillator frequency, soft-start, slope compensation and embeds a voltage output error amplifier allowing use in both isolated and non isolated configuration.

Table 1. Device summary

Order codes	Package	Packing
PM8800A	HTSSOP16	Tube
PM8800ATR	HTSSOP16	Tape and reel

Contents

1 Typical application circuit and block diagram

1.1 Application circuits

Figure 1. Simplified application schematic for powered devicesing PM8800A in isolated configuration

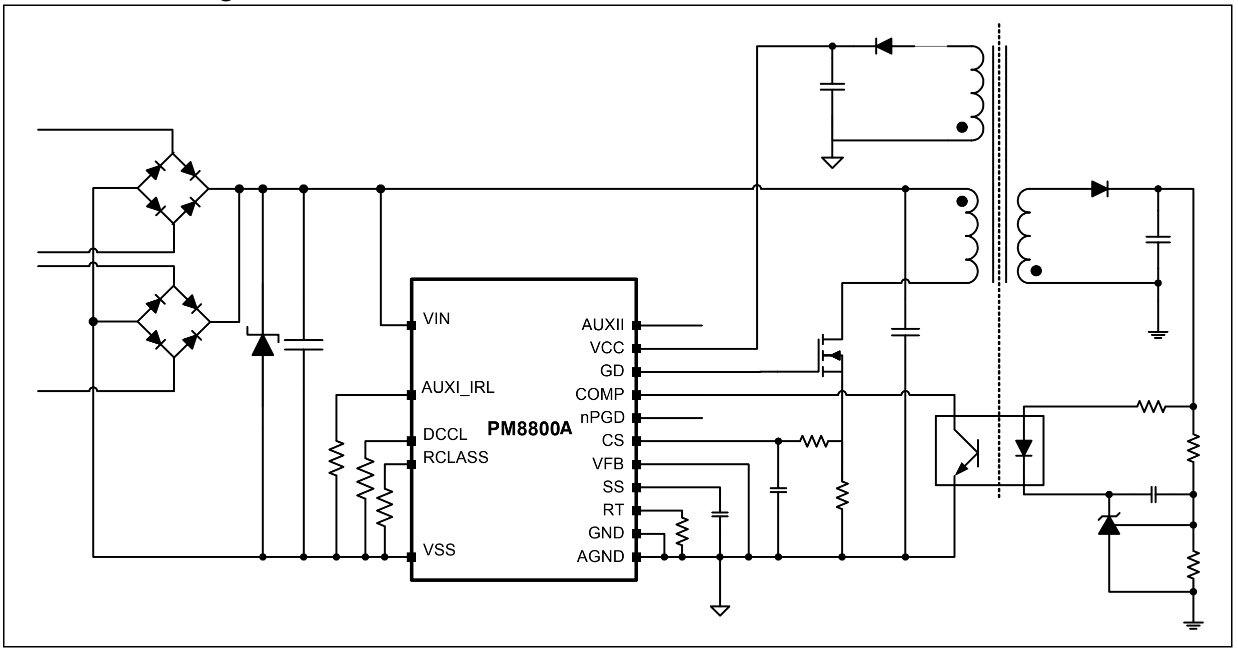
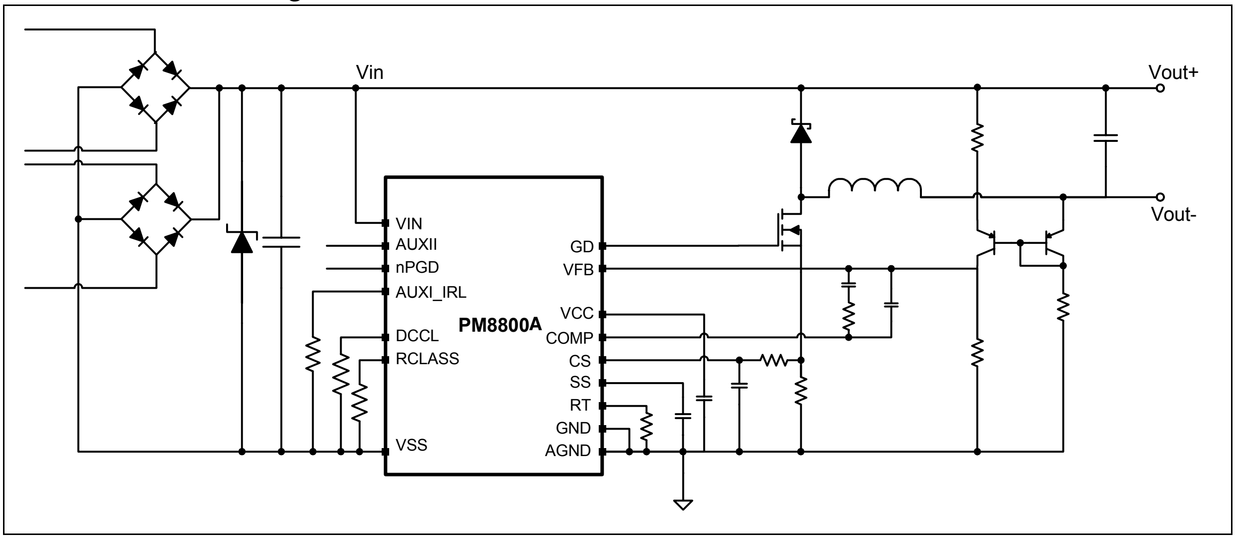


Figure 2. Simplified application schematic for powered device using PM8800A in non-isolated buck configuration



1.2 Block diagram

Figure 3. Block diagram of the PoE PD interface

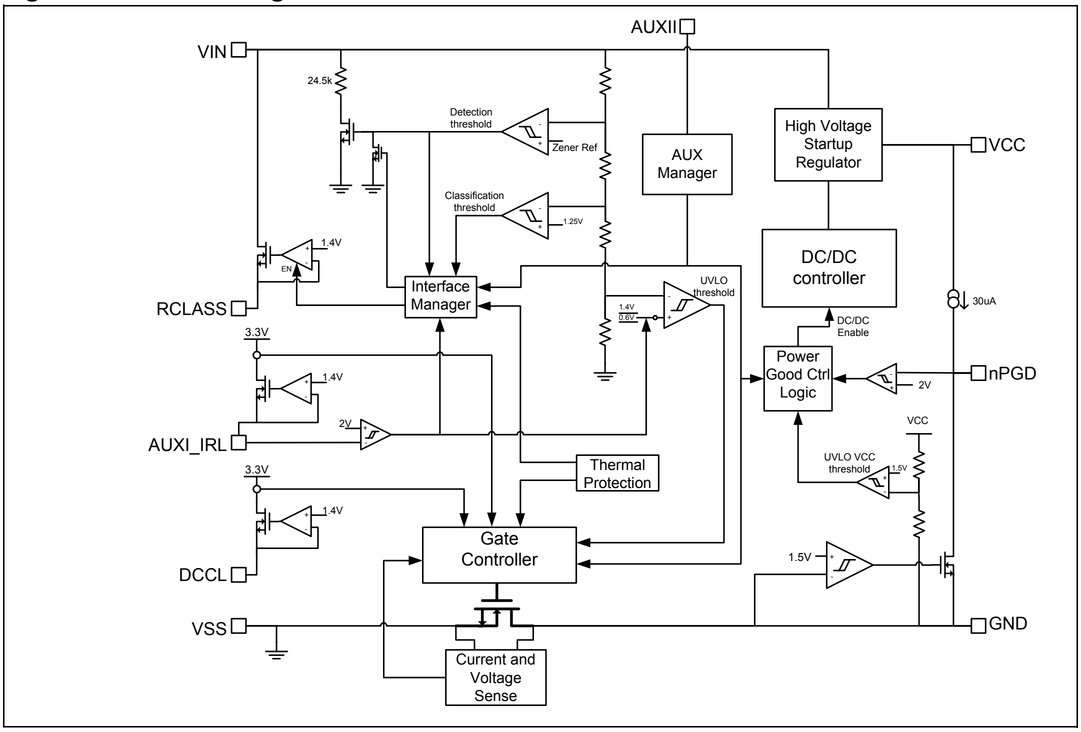
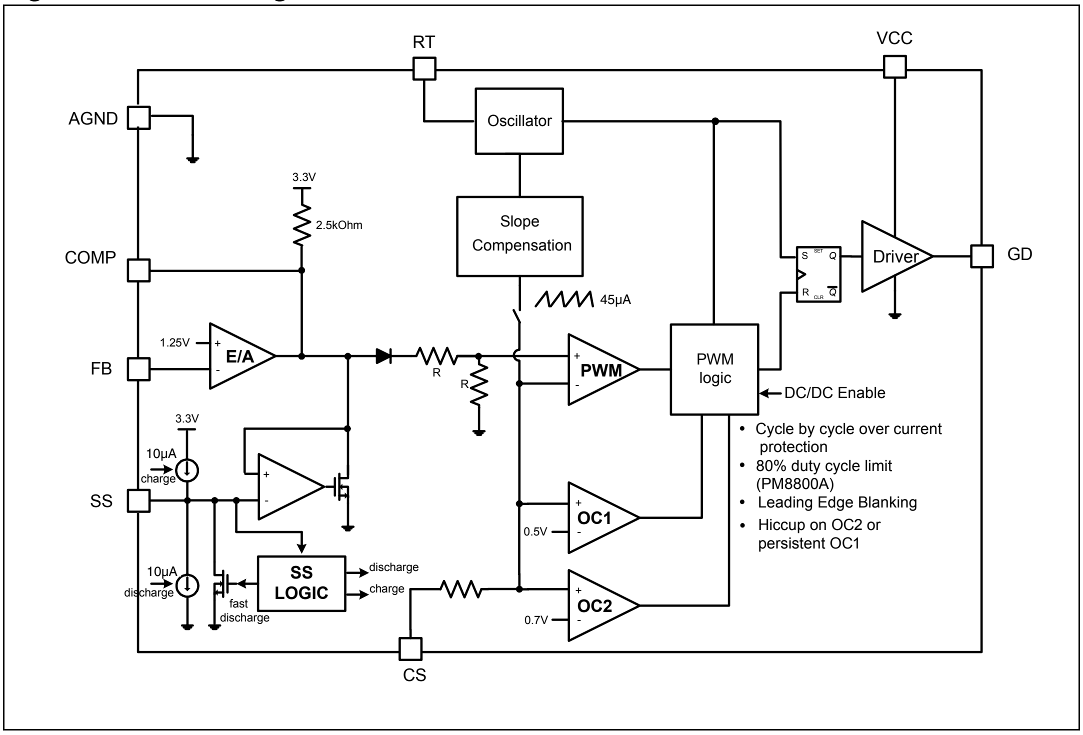
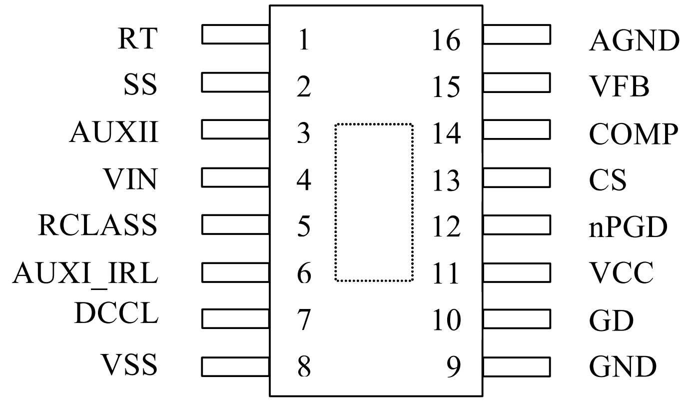


Figure 4. Block diagram of the current mode PWM controller



2 Pins description and connection diagrams

Figure 5. Pins connection (top view)



2.1 Pin descriptions

Table 2. Pin description

Pin#	Name	Function
1	RT	Oscillator timing resistor pin and synchronization input. An external resistor connected from RT to AGND sets the oscillator frequency. This pin will also accept narrow ac-coupled synchronization pulses from an external clock.
2	SS	Soft-start input. An external capacitor connected from SS and AGND and an internal 10 μA current source set the soft-start ramp rate. this pin is also used to set the hiccup timer in case of overcurrent conditions. See *Section 6* for detail.
3	AUXII	Auxiliary source enable pin. Use this pin to power up the DC/DC section only from the external source. The auxiliary source can prevail over the PoE source depending on the value of the resistor between this pin and the external source. See *Section 7* for detail.
4	VIN	System high potential input. The diode “OR” of PoE line and auxiliary sources connected to the PD, it is the most positive input potential.
5	RCLASS	Classification resistor pin. Connect a classification programming resistor between this pin and VSS.
6	AUXI_IRL	In-rush current limit and auxiliary source enable pin. Pulling up this pin to the auxiliary source will change the internal UVLO settings and allow PD to be powered with voltage lower than nominal PoE voltages. In this condition inrush current limit is set to default values. See *Section 7* for details. A resistance between this pin and VSS will set the level of inrush current limit.

Table 2. Pin description (continued)

Pin#	Name	Function
7	DCCL	DC current limit. A resistor between DCCL and VSS will set the current limit for the interface section of the PM8800A. It can be set to exceed the IEEE802.3af current limit. Leave the pin open for standard IEEE 802.3af applications.
8	VSS	System low potential input.
9	GND	System return for the PWM converter. It is the drain of the internal hot-swap power MOSFET.
10	GD	Output of the PWM controller. External power MOSFET gate driver output.
11	VCC	Output of the internal high voltage regulator. When the auxiliary transformer winding (if used) raises the voltage on this pin above the regulation set point, the internal regulator will be switched off, reducing the controller power dissipation.
12	nPGD	Power good, active low signal. A high to low transition indicates that the inrush current phase has been completed, the internal hot swap MOSFET is fully closed and the SMPS portion of the PM8800A is activated.
13	CS	Current sense input. Current sense input for current mode control and over-current protection. Current limiting is obtained with a dedicated current sense comparator. If the CS pin voltage exceeds 0.5 V the GD pin switches low for cycle-by-cycle current limiting. Leading edge blanking is implemented to mask current spikes.
14	COMP	The output of the error amplifier and input of the Pulse Width Modulator. COMP pull-up is provided by an internal 2.5 kΩ resistor which may be used to bias an opto-coupler transistor.
15	VFB	Feedback signal. Inverting input of the internal error amplifier. The non-inverting input is internally connected to a 1.25 V reference. If not used must be grounded to AGND.
16	AGND	Analog PWM supply return. GND for sensitive analog circuitry including the SMPS current limit circuitry. Must be connected to GND to improve noise immunity.
	EP	Exposed pad. Connect this to a board plane to improve heat dissipation; must be electrically connected to VSS

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Max thermal resistance junction to ambient [(1)]	50	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	-40 to 125	°C
T_A	Operative temperature range	-40 to 85	°C

1. Package mounted on 4 layers 35 micron demoboard

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Parameter	Value	Unit
VIN, GND to VSS	-0.3 to 100	V
AUXI_IRL to VSS	-0.3 to 100	V
DCCL, RCLASS to VSS	-0.3 to 3.6	V
AUXII to AGND	-0.3 to 100	V
COMP, SS to AGND	-0.3 to 3.6	V
VFB, RT, CS to AGND	-0.3 to 3.6	V
VCC, GD to AGND	-0.3 to 15	V
nPGD to AGND	-0.3 to 15	V
GND to AGND	-0.3 to 0.3	V

Note: Absolute maximum ratings are limits beyond which damage to the device may occur.

3.2 Electrical characteristic

Table 5. Electrical characteristics - interface section

(V_{IN} = 48 V, VCC = open, T_A = 25 °C unless otherwise specified).

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Detection and classification						
	Signature enable	V_{IN} rising			1.5 (1)	V
	Signature resistance		23.5 (1)	24.5	25.5 (1)	kΩ
	Signature disable classification turn on	V_{IN} rising	10.5 (1)	11.5	12.5 (1)	V
	Classification turn on hysteresis			1.40		V
	Classification turn-off	V_{IN} rising	21.5 (1)	23	24.5 (1)	V
	RCLASS voltage during classification		1.37 (1)	1.4	1.43 (1)	V
	Supply current during classification	V_{IN} inside classification range		1.8		mA
Bias current						
IIN	V_{IN} supply current	V_{IN} = 48 V; VCC = 10 V		3		mA
Under Voltage Lock-Out						
V_{UVLO_R}	UVLO release	V_{IN} rising	37	38.5	40 (1)	V
V_{UVLO_F}	UVLO lock-out	V_{IN} falling	30 (1)	31.5	33.5	V
	UVLO hysteresis			7.0		V
Hot swap MOSFET						
R_{DSON}	MOSFET resistance			0.5	1 (1)	Ω
	Default in-rush current limit	V_{IN} > 30 V	120 (1)	140	160 (1)	mA
	Default in-rush current limit	15 V < V_{IN} < 30 V	220 (1)	250	280 (1)	mA
	Default in-rush current limit	1.5 V < V_{IN} < 15 V	390 (1)	440	490 (1)	mA
	Adjustable in-rush current limit	R_{AUXI_IRL} = 82 kΩ	120 (1)	140	160 (1)	mA
	Default DC current limit		390 (1)	440	490 (1)	mA
	Adjustable DC current limit precision	R_{DCLL} = From 15.4 kΩ to 82 kΩ	-15 (1)	-	+15 (1)	%

Table 5. Electrical characteristics - interface section (continued)

(V_{IN} = 48 V, VCC = open, T_A = 25 °C unless otherwise specified).

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Power good indication						
	Hot-swap V_{DS}	V_{DS} falling	1.45 (1)	1.60	1.75 (1)	V
	Hysteresis			1.45		V
	Hot-swap V_{GS} required for power good	Guaranteed by design		2		V
nPGD	nPGD current source		25 (1)	30	35	µA
	nPGD pull down resistance	nPGD low; I = -5 mA			0.5 (1)	V
	nPGD threshold	nPGD rising	1.7 (1)	2	2.3 (1)	V
Auxiliary power						
AUX I	AUXI_IRL UVLO release	VIN rising	15 (1)	16	17 (1)	V
	AUXI_IRL UVLO lock-out	VIN falling	11.5 (1)	12.5	13.5 (1)	V
	AUXI / IRL switch-over threshold	V_{AUXI_IRL} rising		2		V
AUX II	Bias voltage	I_{AUXII} = 0 to -250 µA	0.85	1.1	1.4	V
	Lower threshold current		20	35	50	µA
	Upper threshold current		80	100	120	µA

Table 6. Electrical characteristics - SMPS section

(V_{IN} = 48 V, VCC = open, T_A = 25 °C unless otherwise specified).

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Oscillator						
f_{osc}	Free running	R_T = open	85 [(1)]	100	115 [(1)]	kHz
	Frequency programmability	R_T = 88 kΩ	210 [(1)]	240	270 [(1)]	kHz
		R_T = 33 kΩ	385 [(1)]	440	495 [(1)]	kHz
	Ext. synch threshold	50 ns pulse		2.8		V
Error amplifier						
V_{EA}	EA input voltage	FB = COMP	1.21 [(1)]	1.25	1.29 [(1)]	V
GBW	Gain bandwidth	Guaranteed by design		10		MHz
G_0	DC gain	Guaranteed by design		75		dB
COMP	Sink current capability	COMP to GND	-8 [(1)]	-15		mA
Soft start						
I_{SS}	Soft start current	Charging	7 [(1)]	10	13 [(1)]	µA
		Discharging	-7 [(1)]	-10	-13 [(1)]	µA
	SS voltage	After soft start	2.1 [(1)]	2.3	2.5 [(1)]	V
Current limit						
	Delay to output	Guaranteed by design		20		ns
	Cycle by cycle current limit threshold voltage		0.44 [(1)]	0.50	0.56 [(1)]	V
	Leading edge blanking time			80		ns
PWM comparator						
	Delay to output	Guaranteed by design		25		ns
	Minimum duty cycle				0 [(1)]	%
	Maximum duty cycle			80	83 [(1)]	%
	COMP to PWM gain	Guaranteed by design		0.5		
Output driver						
	Output high	I_{GD} = 100 mA; guaranteed by design		Vcc-0.4	Vcc-0.7	V
	Output low	I_{GD} = -100 mA		0.25	0.5	V
	Fall time	C_{LOAD} = 3.3 nF		35		ns
	Rise time	C_{LOAD} = 3.3 nF		35		ns
	Peak source current	C_{LOAD} = 3.3 nF; guaranteed by design		800		mA

Table 6. Electrical characteristics - SMPS section

(V_{IN} = 48 V, VCC = open, T_A = 25 °C unless otherwise specified).

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
	Peak sink current	C_{LOAD} = 3.3 nF; Guaranteed by design		1200		mA
Thermal shutdown						
	Shutdown temp.	1st level; Inrush phase only; Guaranteed by design		130		°C
		2nd Level; guaranteed by design		160		°C
	Th. shutdown Hyst.			30		°C
VCC regulation						
VCC	Internal default	VIN = 48 V; VCC = open	8 (1)	8.3	8.6 (1)	V
	Current capability	VIN = 48 V; GD = open			10 (1)	mA
VCC_{UVLO}	Internal default UVLO, release	V_{CC} rising; wrt VCC	-400 (1)		-50	mV
	Internal default; UVLO, lock-out	V_{CC} falling	6.4 (1)	6.7	7.1 (1)	V
ICC	V_{CC} supply current	V_{CC} = 10 V		4		mA
	V_{CC} regulator dropout	ICC = 5 mA; GD = open		2		V

Note: 1 *These values applies over the full operating temperarure range.*

2 *Device thermal limitations could limit useful operating range.*

3 *The V_{CC} regulator is intended for internal use only as bias supply of PM8800A; any additional external V_{CC} current has to be limited within the specified max current limit.*

4 Device description and operation

The PM8800A is a monolithic device embedding an IEEE 802.3af compliant PD interface together with a current mode pulse width modulator to be used in all power over Ethernet powered devices.

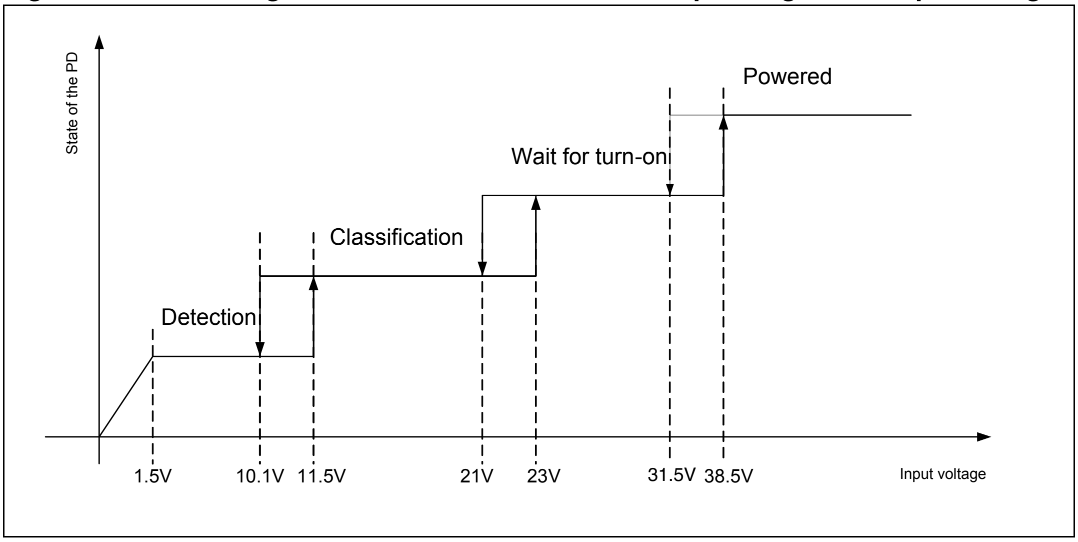
In addition to the standard.3af features, PM8800A anticipates some features of the forthcoming.3at standard, specifically targeting appliances or systems requiring higher power with respect to the 12.95 W allowed by standard PSE.

The PD interface integrates the 24.5 kΩ signature resistor used in detection and disabled during the rest of operating modes. Classification is done through an external resistor detached when classification is over, in order to save power.

The PM8800A integrates standard compliant UVLO thresholds to determine normal operating mode (UVLO rising) or recognize disconnection (UVLO falling).

A graphical representation of the voltage thresholds and hysteresis during all the operating phases is depicted in the following figure:

Figure 6. State diagram of the PM8800A interface depending on the input voltage



For input voltages in the range 1.5 to 11.5 V, PM8800A exposes a 24.5 kΩ resistance. After detection is over, the internal resistor is disabled and the external classification resistor is presented. When classification is over, the external resistor is disconnected and the PM8800A wait for the input voltage to overpass the UVLO voltage.

The hot-swap MOSFET is specifically designed to have a low R_{DSon} to contain the conduction losses and sustain up to 800 mA. A constant dissipated power method is used to limit the current in the in-rush phase. The integrated in-rush current limit controls in a safe manner the current flowing through the MOSFET, shortening the duration of the hot-swap event itself. Designers have the possibility to further limit the current in the in-rush by acting on the proper programming resistor.

Designers have the possibility to set the limit of the current through the interface during normal operation. For non standard application, this limit exceeds the 350 mA foreseen by the 802.3af and can reach up to 800 mA.

PM8800A can work with power either from PoE networks or from auxiliary sources - like AC adapters -. Alternative sources are present in PoE appliances where devices can work also outside the context of the PoE networks or to ensure normal operation even if PoE becomes unavailable. PM8800A limits the number of external components to handle the coexistence of both PoE and auxiliary supplies.

External sources can be connected so to exploit the in-rush current limitation provided by the MOSFET or enabling the PWM section, bypassing the interface section.

A state-of-the-art current mode pulse with modulator is embedded in the PM8800A to support low side single ended isolated and non isolated topologies. A high gain bandwidth product error amplifier is embedded for non isolated configuration.

PM8800A has a 80 % maximum duty cycle, featuring embedded slope compensation.

The PWM switching frequency of PM8800A is programmable with an appropriate resistor and it is also capable of working with an external clock reference.

5 PD interface

5.1 Detection

In power over Ethernet systems, the PSE senses the connection to detect whether an IEEE 802.3af compatible device is plugged to the cable termination by applying a small voltage (2.7 to 10 V) on the Ethernet cable and measuring in two successive steps the equivalent resistance. During this phase, the Powered Device must present a resistance between 23.75 kΩ and 26.25 kΩ

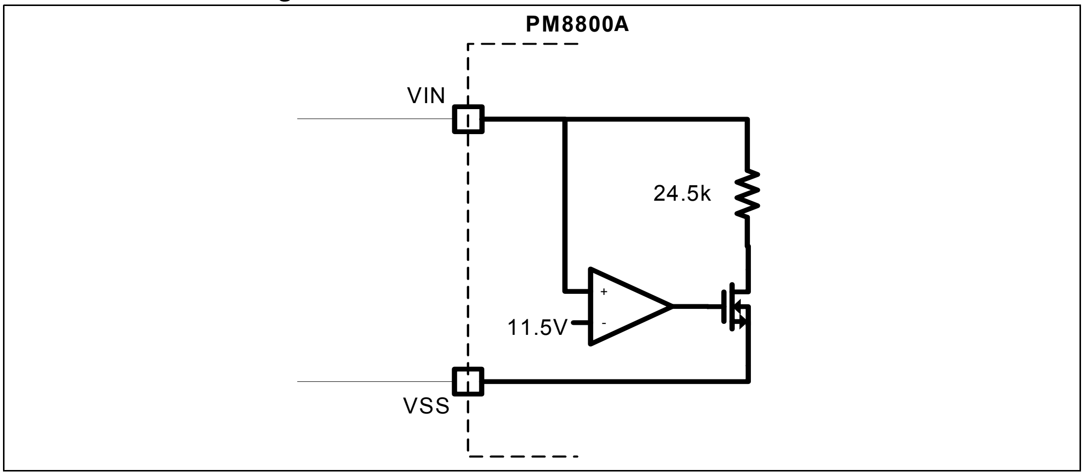
PM8800A integrates a 24.5 kΩ signature resistor to simplify the design of PoE powered Device appliances and to reduce the overall component count.

Signature resistor is in series to a pass transistor (see *Figure 7*) used to disconnect the resistor itself upon completion of the detection phase.

The value of the integrated detection resistance has been selected taking into account also the diode bridges typical voltage drop.

During detection, most of the circuits inside the PM8800A are disabled to minimize the offset current.

Figure 7. PM8800A: reference schematic of the integrated 24.5 kΩ and resistor disable logic



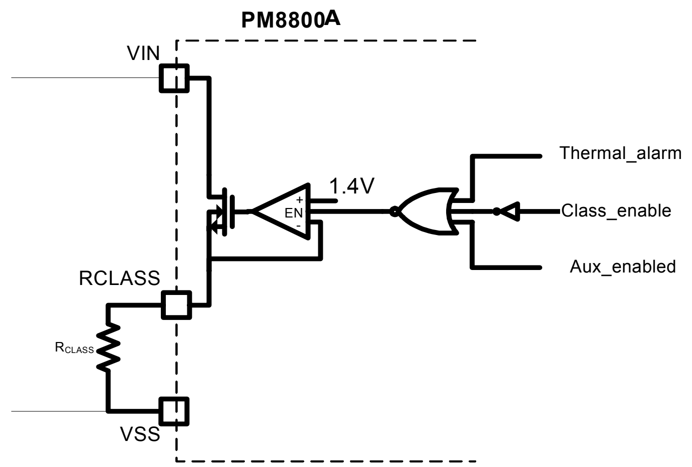
5.2 Classification

Classification process in the IEEE 802.3af standard is optional for the powered device. This feature allows PSE to plan and allocate the available power to the appliances connected to the PoE network. IEEE 802.3af specification groups the need for power of the PD in 5 classes, one is reserved for future use. After successful detection, the PSE sets a constant voltage between 15.5 V and 20.5 V for a maximum duration of 75 ms and senses the current flowing through the cable to determine the PD's class.

The relevant thresholds in PM8800A are 11.5 V and 23 V, with a turn off hysteresis of 1.4 V.

To support the classification function, an equivalent programmable constant current generator has been implemented. The following figure depicts a principle schematic of the classification circuit. Just after the detection phase has been successfully completed, the voltage of the RCLASS pin is set to the 1.4 V voltage reference and a pass transistor connects the VIN pin to RCLASS pin.

Figure 8. PM8800A: reference schematic of the PoE classification logic



Classification resistor can be detached by three main causes:

– An auxiliary power source (front or rear) has been connected (see *Section 7*),
– The device is in thermal protection
– The classification has been successfully completed.

Designers can set the current by changing the value of the external resistor according to the following table.

Table 7. value of the external classification resistor for the different PD class of power

CLASS	PD power (W)	R_{CLASS} (Ω)	IEEE 802.3af Classification current (mA)	
			min	max
0	0.44 - 12.95	Open	0	4
1	0.44 - 3.84	158	9	12
2	3.84 - 6.49	82.5	17	20
3	6.49 - 12.95	52.3	26	30
4	Reserved	36.5	36	44

5.3 Under voltage lock-out

After the classification is completed, the PSE raises the voltage to provide the Power Devices with the negotiated power. During the transition from low to operating voltage, the internal UVLO is released and the hot-swap MOSFET is activated initiating the in-rush sequence.

The IEEE 802.3af standard sets a maximum turn-on voltage (42 V) and the minimum turn-off voltage (30 V) for the PDs and indicates normal voltage drops across the Ethernet cable.

The PM8800A implements the UVLO mechanism by setting 2 internal thresholds on the voltage across the VIN-VSS pins; one is to activate the hot-swap (V_{UVLO_R}), while the other is to switch off the hot-swap MOSFET upon detection of a supply voltage drop (V_{UVLO_F}) from normal operating conditions.

No additional external components are required to comply with the IEEE 802.3af requirements. Thermal protection alarm overrides the gate driving of the MOSFET immediately switching off the MOSFET itself in case of device overheating. The hot-swap is bypassed also in auxiliary source topology supplying directly the PWM and not requiring the hot-swap to be active.

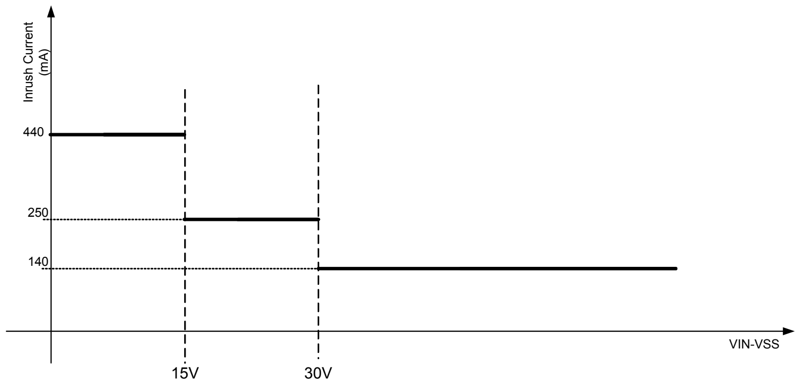
5.4 In rush current limit

Once the detection and classification phases have been successfully completed, the PSE raises the voltage across the Ethernet cable. When the voltage difference between the VIN and VSS is greater than the V_{UVLO_R} threshold, the internal hot-swap MOSFET is switched on and the DC-DC input capacitance is charged in a controlled way.

As depicted in the following figure, the current delivered by the hot-swap MOSFET during inrush period is a function of the voltage drop between GND and VSS (hot-swap drain source terminals). In more detail, the higher the voltage across the internal hot-swap, the lower the current flowing trough it, so that the total dissipated power is almost constant throughout the inrush phase, preventing the IC to reach the thermal protection limit.

The lower current limitation is internally set at 140 mA and takes action when the voltage GND-VSS is above 30 V. The second limit is set at 250 mA when GND-VSS voltage is between 30 V and 15 V. When the voltage falls below 15 V, the limit switches to the higher inrush current level, which is set by default at 440 mA. Connecting a resistor between VSS and AUXI_IRL it's possible to adjust this limit to a lower value.

Figure 9. Relation between the hot-swap drain-source voltage and the default Inrush current.



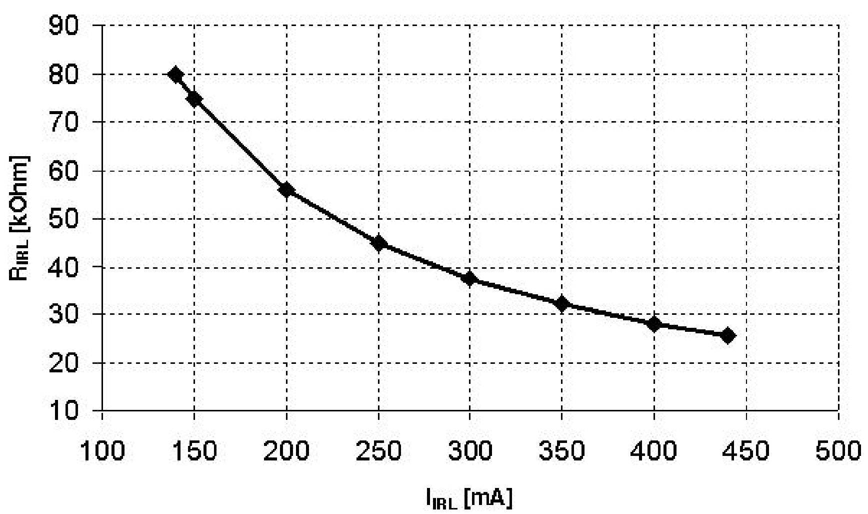
The maximum inrush current can be set by programming the value of the resistor on the AUX_IRL pin. Depending on the chosen value there could be 3 steps (when the selected max current is between 250 and 400 mA), 2 steps (when the selected max current is between 140 and 250 mA) or a single step.

The formulae to select the desired inrush current is the following:

$$R_{IRL}[k\Omega] = \frac{11200}{I_{IRL}[mA]}$$

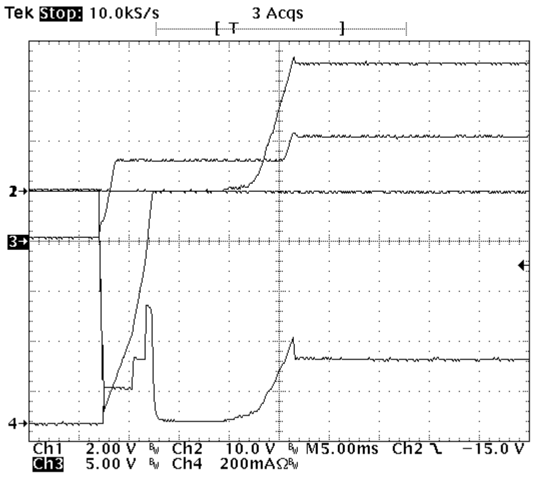
The PM8800A useful programming range for the inrush current limitation is between 140 mA and 440 mA. Practical resistor value ranges between 25 kΩ and 82 kΩ.

Figure 10. Inrush current limit vs R_{IRL}



In the following picture a typical start sequence that can be observed in real circuits.

Figure 11. Typical start up sequence



Ch1 = 5 Vout, Ch2 = VSS - GND, Ch3 = Vcc, Ch4 = I input

Depending on the application, care must be put on the choice of the inrush current limit to avoid that the voltage drop on the external Ethernet cable will cause UVLO conditions during the charging phase of the bulk capacitor.

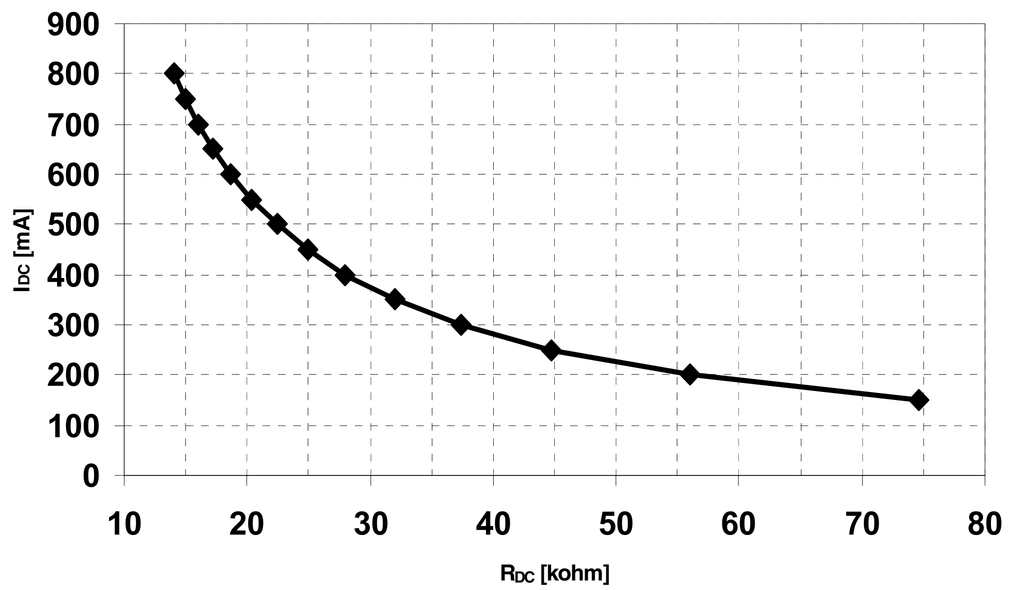
It is recommended to select this voltage drop (20 Ω max for 100 m of cable x I inrush) to be lower than the UVLO hysteresis (7 V) in order to avoid hiccup turn on.

5.5 Continuos current limitation

PM8800A provide a default continuos current limitation of 440 mA. This is achieved by leaving the pin DCCDL floating. A different DC current limit can be set by connecting a resistor between DCCL and VSS whose value can be obtained by the following equation:

$$R_{DC}[k\Omega] = \frac{11200}{I_{DC}[mA]}$$

Figure 12. DC current vs R_{DC}



This limitation is active after nPGD set and when the PD is supplied through the PoE or in the Front connection (see *Section 7*)

The PM8800A useful programming range for the current limitation is between 150 mA and 800 mA. Practical resistor value ranges between 15 kΩ and 75 kΩ.

5.6 HV regulator startup

PM8800A embeds a high voltage start-up regulator to provide a controlled reference voltage of 8.3 V to the Current mode PWM during its start-up phase.

The regulator output is connected to the VCC pin as well as to the DC DC section

In normal isolated topology, the VCC pin is diode connected to the auxiliary winding of the transformer used for the flyback or forward configuration. When the voltage from the transformer exceeds the regulated voltage, the high voltage regulator is shut off, reducing the amount of power dissipated inside the PM8800A.

The external auxiliary voltage must higher then 8.3 V but must be also lower than 15 V under all working conditions, to avoid the intervent of the internal protection clamp.

A VCC UVLO mechanism monitors the level of voltage on the VCC pin. When VCC voltage exceeds the VCC_{UVLO_R} the PWM controller is enabled and it remains enabled until the VCC voltage drops under its VCC_{UVLO_F} value.

5.7 Power good indication

The PM8800A embeds a power good circuit that is used to indicate that PWM input capacitors are fully charged and that the switching regulator can start operation. The power good circuit monitors the status of the internal hot-swap MOSFET and nPGD, an active low signal is asserted when its V_{DS} voltage falls below 1.5 V and V_{GS} rise above 2 V. The power good circuit includes hysteresis to allow the PM8800A to operate near the current limit point without inadvertently disabling nPGD. The MOSFET voltage must increase to 3 V before nPGD is disabled.

An internal comparator monitors the status of the nPGD pin and the PWM controller will be running until the voltage at this pin goes above 2 V.

The power good indication is exposed at nPGD pin with a open drain, 45 Ω MOSFET so that board designers can put a LED and a series current limiting resistor from the VCC pin to the nPGD pin to indicate that the PD is powered from the PoE network.

Since the power good signal is internally used to activate the PWM controller, to avoid that transients on the input voltage could produce intermittent operation of the PWM controller, board designer can connect a capacitor C_{PGD} between the nPGD pin and GND. This will mask the nPGD signal for a duration that can be estimate by the following equation:

$$\Delta t(\mu s) = \frac{(2V \cdot C_{PGD}(nF))}{(0.03mA + I_{LED}(mA))}$$

where 30 µA is an internal current source that act as pull-up on the nPGD pin and I_{LED} is the current flowing through the external LED, if present.

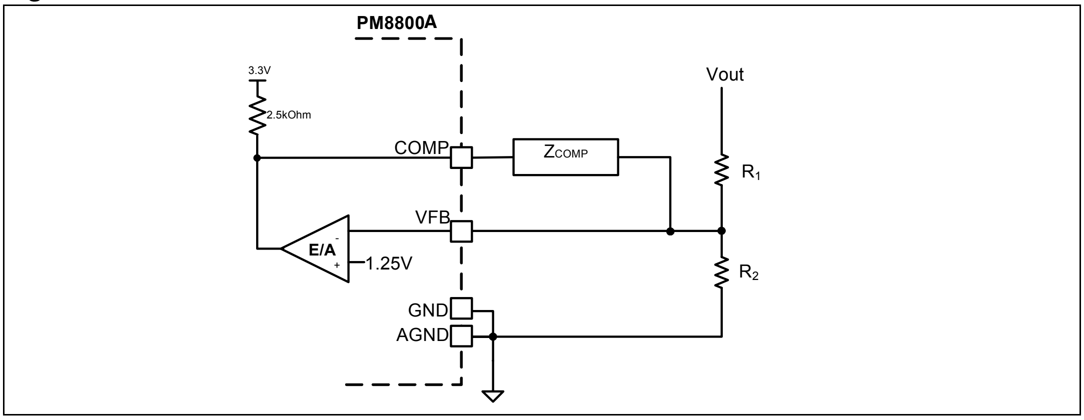
6 PWM section

6.1 Error amplifier and loop compensation

The PM8800A addresses both isolated and non-isolated configuration by embedding a wide band high gain error amplifier.

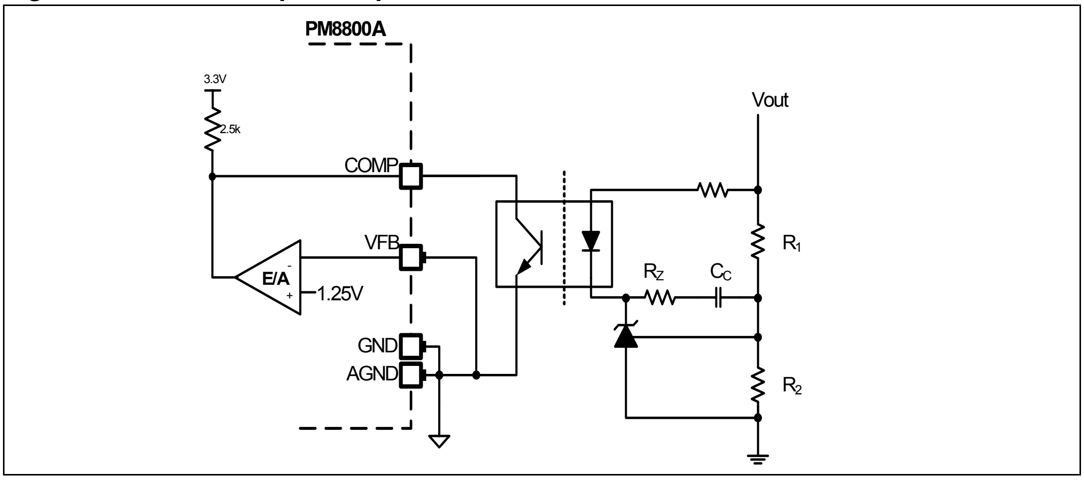
In non-isolated topology, the voltage to be regulated is connected to the FB pin - the inverting input of the EA - through a resistor divider. The non inverting input of the EA is set to a fixed reference value of 1.25 V. The output of the error amplifier is connected to the COMP pin which is pulled up internally with a 2.5 kΩ resistor to a fixed reference of 3.3 V; loop compensation can be done connecting an appropriate compensation network between the FB pin and the COMP pin

Figure 13. Non-isolated feedback



In typical isolated topology, the error amplifier is located outside the IC and the feedback signal is taken on the collector of an opto coupler. The internal error amplifier is to be bypassed connecting the FB pin to AGND. In order to minimize external components count the opto coupler is directly connected to the COMP pin using the internal pull-up resistor as bias for the opto coupler.

Figure 14. Isolated opto coupler feedback.



When a shunt regulator is used for output voltage regulation, the output voltage is set by the ratio of resistors R1 and R2, see *Figure 14* for details. The output voltage is given by the following equation:

$$V_{out} = V_{REF} \cdot \left(1 + \frac{R_2}{R_1}\right)$$

where V_{REF} is the reference voltage of the shunt regulator chosen for the application.

Loop compensation in typical isolated application is done by connecting an appropriate compensation network around the external error amplifier.

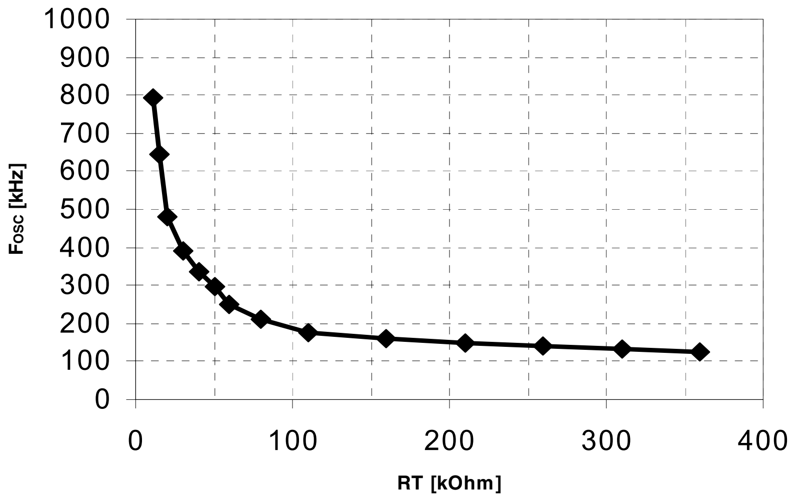
A pull-up current source of few nA is internally connected to FB pin providing a safe switch-off of the DC DC converter in case of feedback disconnection.

6.2 Oscillator and sync capability

The internal oscillator frequency can be programmed by connecting an external resistor between the RT and AGND pins. The relation between the oscillator frequency f_{OSC} and the R_T resistor is:

$$f_{osc}(kHz) = 100 \cdot \left(1 + \frac{125}{3k\Omega + R_T(k\Omega)}\right)$$

Figure 15. PWM frequency vs R_T



The PWM switching frequency is equal to the programmed oscillator frequency.

The PM8800A can work also with a clock reference provided by an external source whose frequency is higher than the one programmed by the R_T resistor. The presence of the external resistor is mandatory also when the reference is provided from outside the IC.

The external source must coupled to the RT with a 100 pF capacitor and have a minimum peak amplitude of 2.8 V. Minimum pulse width of 50 ns has to be assured for proper operation.

When synchronized the PWM frequency is equal to the external clock reference.

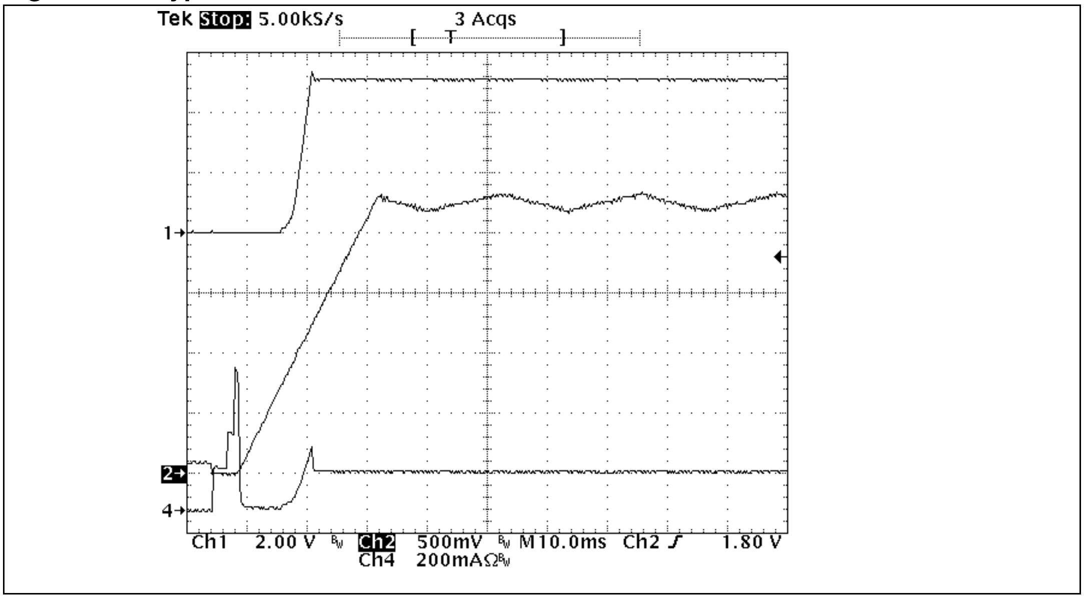
6.3 Soft start

The soft-start feature of the PM8800A allows the load voltage to ramp-up in a safe and controlled manner. This is achieved by a 10 µA internal current source charging an external C_{ss} capacitor connected to the SS pin, which progressively increases the duty cycle of the PWM pulse, since the reference of the error amplifier is clamped with this value. Duration of the start-up time and external capacitor are linked by the following relation:

$$t_{ss}(ms) = 0.23 \cdot C_{SS}(nF)$$

SS voltage is actively kept at 2.3 V by the internal control circuitry, which manages also over-current and fault conditions.

Figure 16. Typical soft start waveform



Ch1 = 5Vout, Ch2 = soft start, Ch4 = I input