



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



## High-efficiency, IEEE 802.3at compliant, integrated PoE-PD interface and PWM controller

Datasheet - production data



### Features

- IEEE 802.3at compliant PD interface
- Works with power supplied from Ethernet LAN cables or from local auxiliary sources
- Successful IEEE802.3at Layer1 classification indicator
- Integrated 100 V, 0.45  $\Omega$ , 1 A hot-swap MOSFET
- Accurate 140 mA typ. inrush current level
- Programmable classification current
- Sleep mode with LED indicator and Maintain Power Signature (MPS)
- Precise DC current limit set at 640 mA typ.
- Integrated high-voltage startup bias regulator
- Thermal shutdown protection
- Current mode pulse width modulator
- Programmable oscillator frequency
- 80% maximum duty cycle with internal slope compensation
- Support for flyback, forward, forward active clamp, flyback with synchronous rectification

### Applications

- VoIP phones, WLAN AP
- WiMAX CPEs
- Security cameras
- PoE/PoE+ Powered device appliances

### Description

The PM8801 integrates a standard compliant Power over Ethernet (PoE) interface and a current mode PWM controller to simplify the design of the power supply sections of all powered devices.

The PoE/PoE+ interface incorporates all the functions required by the IEEE 802.3at including detection, classification, undervoltage lockout (UVLO) and inrush current limitation.

The PM8801 specifically performs IEEE802.3at Layer1 hardware classification, providing an indication of type 2 PSE successful detection to the rest of the system.

The PM8801 has been designed to work with power either from the Ethernet cable connection or from an external power source such as a wall adapter, ensuring prevalence of the auxiliary source with respect to the PoE interface.

The DC/DC section of the PM8801 features a programmable oscillator frequency, an adjustable slope compensation, dual complementary low-side drivers with programmable delay time and internal temperature sensor.

The PM8801 targets high-efficiency conversion at all load conditions supporting flyback, forward, forward active clamp and synchronous rectification.

**Table 1. Device summary**

Part number	Package	Packing
PM8801	HTSSOP24	Tube
PM8801TR		Tape and reel

# Contents

<b>1</b>	<b>Typical application circuit and block diagram</b>	<b>6</b>
1.1	Application circuits	6
1.2	Block diagrams	8
<b>2</b>	<b>Pin descriptions and connection diagram</b>	<b>10</b>
<b>3</b>	<b>Electrical specifications</b>	<b>13</b>
3.1	Absolute maximum ratings	13
3.2	Thermal data	13
3.3	Electrical characteristics	14
<b>4</b>	<b>PD interface</b>	<b>19</b>
4.1	Detection	19
4.2	Classification	19
4.3	Indication of successful 2-event classification	20
4.4	Undervoltage lockout	22
4.5	Inrush and DC current limiting	22
4.6	Sleep mode / MPS mode	23
4.7	LED driving	24
4.8	Wakeup from sleep mode	26
4.9	High-voltage startup regulator	26
4.10	5 V bias regulator	27
<b>5</b>	<b>PWM controller</b>	<b>28</b>
5.1	Oscillator	28
5.2	Delay time control	28
5.3	Soft-start	30
5.4	PWM comparator / slope compensation	30
5.5	Current limit	30
5.6	Thermal protection	31

---

6	Auxiliary sources .....	32
7	HTSSOP24 mechanical data & package dimensions .....	34
8	Revision history .....	36

## List of tables

Table 1.	Device summary . . . . .	1
Table 2.	Pin descriptions . . . . .	10
Table 3.	Absolute maximum ratings . . . . .	13
Table 4.	Thermal data. . . . .	13
Table 5.	Electrical characteristics - interface section . . . . .	14
Table 6.	Electrical characteristics - SMPS section . . . . .	15
Table 7.	Value of the external classification resistor for the different PD classes of power . . . . .	20
Table 8.	LED duty cycle selection. . . . .	24
Table 9.	TSSOP24 mechanical data . . . . .	34
Table 10.	Document revision history . . . . .	36



## List of figures

Figure 1.	Simplified application schematic for powered devices using PM8801 in forward active clamp configuration . . . . .	6
Figure 2.	Simplified application schematic for powered devices using PM8801 in synchronous flyback configuration . . . . .	7
Figure 3.	PM8801 internal block diagram . . . . .	8
Figure 4.	Block diagram of the DC/DC section of the PM8801 . . . . .	9
Figure 5.	Pin connections (top view) . . . . .	10
Figure 6.	PM8801: reference schematic of the PoE classification logic. . . . .	20
Figure 7.	T2P signal when connected to PSE supporting 1-event classification . . . . .	21
Figure 8.	T2P signal when connected to PSE supporting 2-event classification . . . . .	21
Figure 9.	Line transient response . . . . .	23
Figure 10.	Sleep mode with pulsed MPS current. . . . .	24
Figure 11.	LED enabled at startup . . . . .	25
Figure 12.	Wakeup sequence . . . . .	26
Figure 13.	PWM frequency vs. $R_T$ . . . . .	28
Figure 14.	Delay time vs. RDT . . . . .	29
Figure 15.	Timing relationship between output drivers as a function of DT . . . . .	29
Figure 16.	Overload (left) and short-circuit (right) behavior . . . . .	31
Figure 17.	Smooth transition from POE to auxiliary source and vice-versa. . . . .	32
Figure 18.	HTSSOP24 package dimensions . . . . .	35

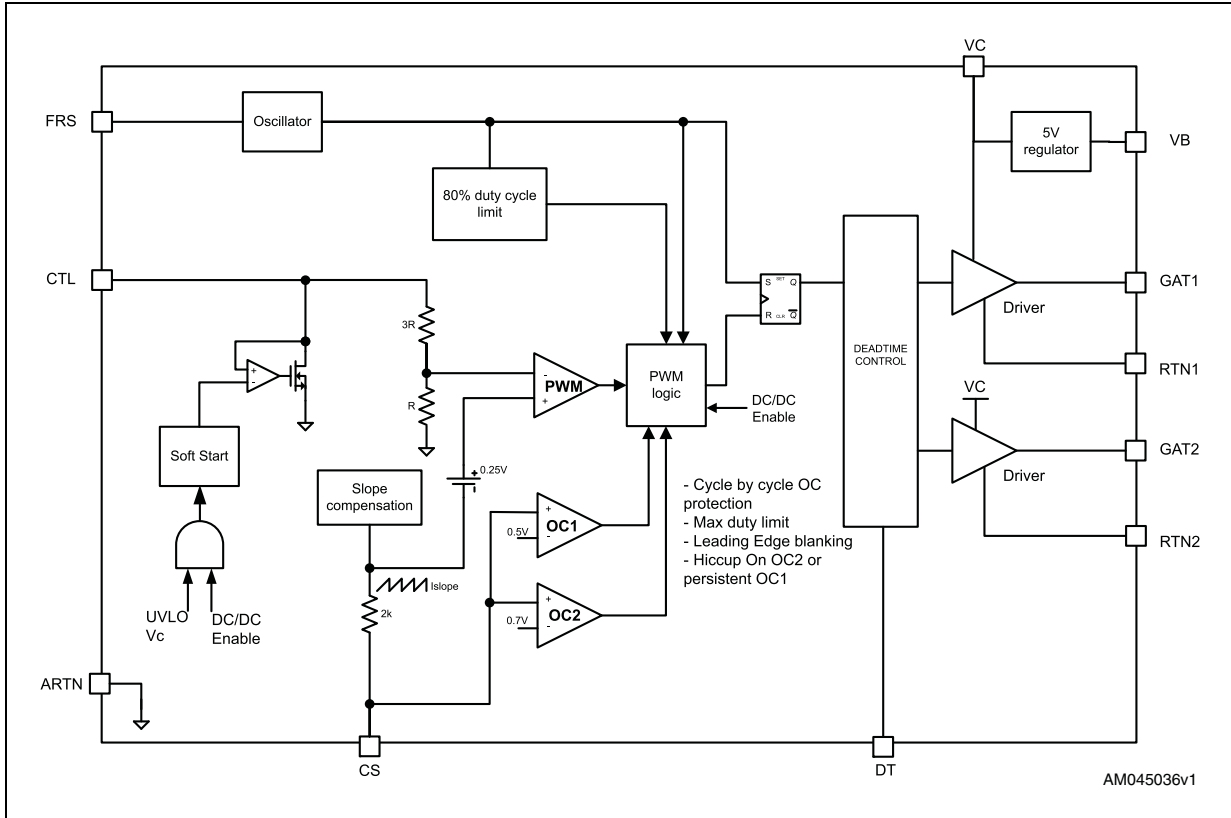






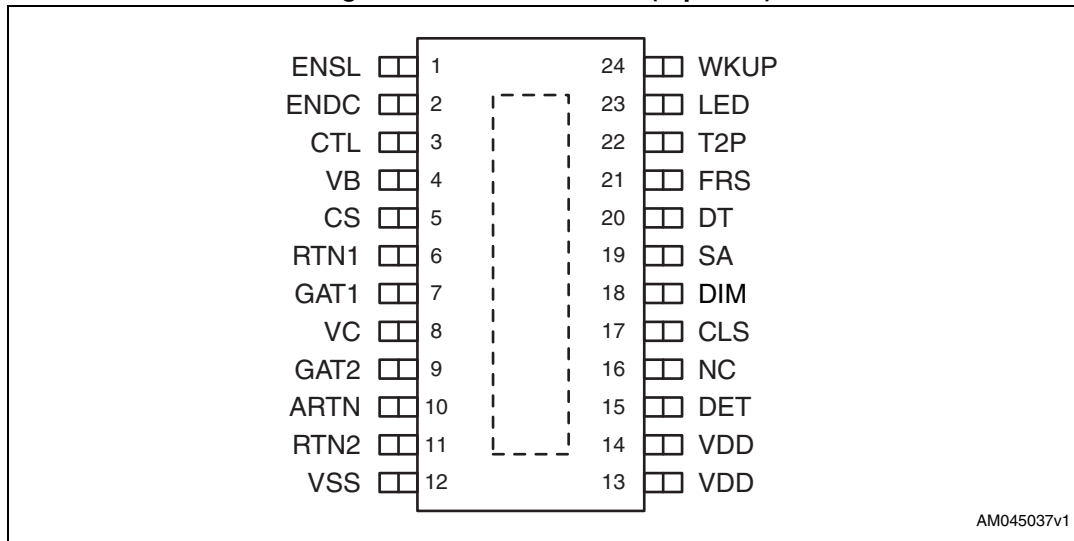


Figure 4. Block diagram of the DC/DC section of the PM8801



## 2 Pin descriptions and connection diagram

Figure 5. Pin connections (top view)



AM045037v1

Table 2. Pin descriptions

Pin#	Name	Function
1	ENSL	Sleep mode input: active-low signal. An optocoupler may be used to force the PM8801 to enter into sleep mode, shutting down its internal DC/DC controller.
2	ENDC	MPS duty cycle / LED enable: active-low signal. Drive this pin low to disable the LED driver during normal operations. Entering sleep mode the host of the PoE-PD may drive this pin through an optocoupler to set the MPS current profile. The signal value is sampled on the ENSL pin during transition to sleep mode. If low the MPS current is pulsed, if high the MPS current is constant.
3	CTL	Input of the pulse width modulator. CTL pull-up to VB is provided by an external resistor which may be used to bias an opto-coupler transistor.
4	VB	5 V, up to 10 mA bias regulator. This reference voltage can be used to bias an opto-coupler transistor. In sleep mode VB regulator is switched off.
5	CS	Current sense input for current mode control and overcurrent protection. Current sensing is accomplished using a dedicated current sense comparator. If the CS pin voltage exceeds 0.5 V, the GAT1 pin switches low for cycle-by-cycle current limiting. CS is internally held low for 60 ns after GAT1 switches high to blank leading edge current spikes.
6	RTN1	Power ground for the GAT1 driver. This pin must be connected to RTN2 and ARTN.

Table 2. Pin descriptions (continued)

Pin#	Name	Function
7	GAT1	Main gate driver output of the PWM controller. DC-DC converter gate driver output with 1A peak sink-source current capability. (5 $\Omega$ typ MOSFETs).
8	VC	Output of the internal high-voltage regulator. When the auxiliary transformer winding (if used) raises the voltage on this pin above the 8 V typ. regulation set point, the internal regulator will shut down, reducing the internal power dissipation. Filter this pin with a 1 $\mu$ F typ connected to ground.
9	GAT2	Secondary gate driver output. AUX gate driver output for active clamp or synchronous rectification designs. 1 A peak sink-source current capability (5 $\Omega$ typ MOSFETs).
10	ARTN	Analog PWM supply ground. RTN for sensitive analog circuitry including the SMPS current limit amplifier.
11	RTN2	Power ground for the secondary gate driver. This pin is also connected to the drain of the internal current-limiting power MOSFET which closes VSS to the return path of the DC-DC converter. This pin must be connected to RTN1 and ARTN.
12	VSS	System low potential input. Diode "OR'd" to the RJ45 connector and PSE's -48 V supply, it is the more negative input potential.
13	VDD	System high potential input. The diode "OR" of several lines entering the PD, it is the most positive input potential.
14	VDD	System high potential input. The diode "OR" of several lines entering the PD, it is the most positive input potential.
15	DET	Detection resistor. Connect the signature resistance between DET pin and VDD. Current will flow through the resistor only during the detection phase. This pin is 100 V rated with negligible resistance with respect to the external 24.9 k $\Omega$ .
16	NC	Not Connected.
17	CLS	Classification resistor. Connect the classification programming resistor from this pin to VSS.
18	DIM	LED dimming set. A resistor between this pin and VSS will set the duty cycle of the PWM current driving the LED connected to pin 23.
19	SA	Auxiliary input startup pin. Pulling up this pin will give high priority to an auxiliary power source like an external wall adapter. Use a resistor voltage divider from the auxiliary voltage to ARTN to connect this low voltage rating pin. Connect this pin to ARTN if not used.

Table 2. Pin descriptions (continued)

Pin#	Name	Function
20	DT	Delay time set. A resistor connected from this pin to ARTN sets the delay time between GAT1 and GAT2. This pin cannot be left open.
21	FRS	Switching frequency set. An external resistor connected from FRS to ARTN sets the oscillator frequency.
22	T2P	Successful 2-event classification indicator. T2P open-drain signal assertion happens when powered by a PSE performing a 2-event classification. T2P is an active-low signal.
23	LED	Sleep mode LED indicator. An LED connected to VSS is driven by a 250 Hz, 12 mA PWM current. The LED brightness can be set through the DIM pin.
24	WKUP	Wake-up signal. Closing the switch from WKUP to VSS, the PM8801 wakes up from sleep mode, enabling the DC/DC controller with a soft-start. The WKUP is an active-low input.
	EP	Exposed Pad. Connect this pad to a pcb copper plane to improve heat dissipation; must be electrically connected to VSS.

## 3 Electrical specifications

### 3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Parameter	Value	Unit
VDD, DET, ARTN to VSS	-0.3 to 100	V
LED to VSS	-0.3 to 5.5	V
CLS, DIM, WKUP to VSS	-0.3 to 3.6	V
VC to ARTN	-0.3 to 16	V
GAT1, GAT2, T2P to ARTN	-0.3 to VC+0.3	V
CTL, VB, DT, ENDC, ENSL to ARTN	-0.3 to 5.5	V
FRS, SA, CS to ARTN	-0.3 to 3.6	V
RTN1, RTN2 to ARTN	-0.3 to 0.3	V
ESD HBM	2	kV
ESD CDM	500	V
Operating junction temperature <sup>(1)</sup>	-40 to 150	°C
Storage temperature	-40 to 150	°C

1. Internally limited to 160 °C typ. with internal overtemperature protection circuit.

*Note:* Absolute maximum ratings are limits beyond which damage to the device may occur.

### 3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R <sub>THJA</sub>	Max thermal resistance junction to ambient <sup>(1)</sup>	40	°C/W
T <sub>MAX</sub>	Maximum junction temperature	150	°C
T <sub>STG</sub>	Storage temperature range	-40 to 150	°C
T <sub>J</sub>	Operative junction temperature range	-40 to 125	°C
T <sub>A</sub>	Operative ambient temperature range	-40 to 85	°C

1. Package mounted on a 4-layer board ( 2 signals + 2 powers ), CU thickness 35 micron, with 6-8 vias on the exposed pad copper area connected to an inner power plane

### 3.3 Electrical characteristics

VDD = 48 V, VC = not loaded, Cvc = 1 μF, VB = not loaded, Cvb = 1 μF,

GAT1 and GAT2 = not loaded, TA = 25 °C unless otherwise specified.

Values in Bolded type apply over the full operating ambient temperature range.

**Table 5. Electrical characteristics - interface section**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
<b>Detection and Classification</b>						
	Signature enable	VDD rising			<b>1.5</b>	V
	Signature pull down resistance	within signature range		150	<b>350</b>	Ω
	Signature disable	VDD rising	<b>10.3</b>	10.8	<b>11.3</b>	V
	Classification enable	VDD rising	<b>11.3</b>	12	12.7	V
	Classification turn-off	VDD rising	<b>21.5</b>	23.0	<b>24.5</b>	V
	Mark event threshold / Classification turn-off	VDD falling	<b>9</b>	10	<b>11</b>	V
	Classification reset threshold	VDD falling	<b>3</b>	4	<b>5</b>	V
	CLS voltage	within classification range with 44 mA load	<b>1.3</b>	1.4	<b>1.5</b>	V
	CLS max current capability	within classification range with CLS pin grounded	<b>50</b>	65	<b>80</b>	mA
<b>Bias current</b>						
I <sub>dd</sub>	VDD supply current during detection	VDD = 8 V			10	μA
	VDD supply current during classification			900	<b>1200</b>	μA
	VDD supply current during mark event		<b>500</b>	800	<b>1100</b>	μA
<b>Undervoltage lockout</b>						
V <sub>UVLO_R</sub>	UVLO release	VIN rising	<b>34</b>	35	<b>36.5</b>	V
V <sub>UVLO_F</sub>	UVLO lockout	VIN falling	<b>30</b>	31	<b>32.5</b>	V
	UVLO hysteresis		<b>3.5</b>	4	<b>4.5</b>	V
<b>Hot-swap MOSFET</b>						
R <sub>DSON</sub>	MOSFET resistance			0.45	<b>1</b>	Ω
	Default inrush current limit		<b>125</b>	140	<b>155</b>	mA
	Default DC current limit		<b>590</b>	640	<b>690</b>	mA



Table 5. Electrical characteristics - interface section (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
<b>Inrush to DC current switchover</b>						
	V <sub>DS</sub> required for inrush to DC switchover	V <sub>DS</sub> falling - hot-swap MOSFET closing	<b>1.35</b>	1.50	<b>1.75</b>	V
	V <sub>GS</sub> required for inrush to DC Switchover	V <sub>DS</sub> falling - hot-swap MOSFET closing. Guaranteed by design.		2		V
	V <sub>DS</sub> required for inrush to DC Switchover	V <sub>DS</sub> rising - hot-swap MOSFET opening	<b>11</b>	12	<b>13</b>	V
<b>LED</b>						
I <sub>LED</sub>	LED PWM current amplitude	Sourced from LED pin	<b>9</b>	12	<b>14</b>	mA
V <sub>fLED_MAX</sub>	LED maximum forward voltage		<b>4.5</b>			V
f <sub>LED</sub>	LED PWM current frequency			250		Hz
<b>Maintain Power Signature</b>						
I <sub>ddMPS</sub>	MPS current	including VDD quiescent current		13		mA
T <sub>MPS</sub>	MPS current draw duration	ENDC = 0 V	<b>75</b>	100		ms
T <sub>MPDO</sub>	MPS current dropout duration	ENDC = 0 V		200	<b>250</b>	ms
<b>Wakeup from sleep mode</b>						
	WKUP threshold	WKUP falling	<b>1.3</b>	1.4	<b>1.5</b>	V
	WKUP pull-up current			450		μA

Table 6. Electrical characteristics - SMPS section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
<b>Oscillator</b>						
F <sub>osc</sub>	Frequency accuracy	In the range 100 to 500 kHz		+/-10		%
	Frequency programmability	R <sub>FRS</sub> = 100 kΩ	<b>220</b>	245	<b>270</b>	kHz
R <sub>FRS</sub> = 47.5 kΩ		<b>445</b>	495	<b>545</b>	kHz	
	Frequency range		100		1000	kHz
	FRS voltage		<b>1.20</b>	1.25	<b>1.30</b>	V
<b>Delay time</b>						
	GAT1 to GAT2 delay time	R <sub>DT</sub> = 20 kΩ, GAT1 and GAT2 open		32		ns
		R <sub>DT</sub> = 200 kΩ, GAT1 and GAT2 open		320		ns
	DT voltage		<b>1.20</b>	1.25	<b>1.30</b>	V

**Table 6. Electrical characteristics - SMPS section (continued)**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
<b>Soft-start</b>						
T <sub>SS</sub>	Soft-start time	Over CTL full range (0 to 3V), at F <sub>osc</sub> = 250 kHz		12.3		ms
<b>Current limit</b>						
	Delay to output	Guaranteed by design		20		ns
	Cycle-by-cycle current limit threshold voltage		<b>0.44</b>	0.50	<b>0.56</b>	V
	Leading edge blanking time		<b>45</b>	60	<b>75</b>	ns
	Slope compensation current	Sourced by CS pin		45		μA
<b>PWM comparator</b>						
	Delay to output	Guaranteed by design		25		ns
	Minimum duty cycle	CTL = 0, CS = 0			0	%
	Maximum duty cycle	CTL = 2 V, CS = 0, F <sub>osc</sub> = 250 kHz	<b>75</b>	80	<b>85</b>	%
	CTL to PWM gain	Guaranteed by design		1: 4		
	CTL operative range		1		3	V
<b>Output driver GAT1</b>						
	Output high	I <sub>GD</sub> = 100 mA		VC-0.25	<b>VC-0.5</b>	V
	Output low	I <sub>GD</sub> = -100 mA		0.25	<b>0.5</b>	V
	Fall time	C <sub>LOAD</sub> = 3.3 nF, VC = 10 V Guaranteed by design		40		ns
	Rise time	C <sub>LOAD</sub> = 3.3 nF, VC = 10 V Guaranteed by design		45		ns
	Peak source current	C <sub>LOAD</sub> = 3.3 nF, VC = 10 V Guaranteed by design		800		mA
	Peak sink current	C <sub>LOAD</sub> = 3.3 nF, VC = 10 V Guaranteed by design		1		A
<b>Output driver GAT2</b>						
	Output high	I <sub>GD</sub> = 100 mA		VC-0.25	VC-0.5	V
	Output low	I <sub>GD</sub> = -100 mA		0.25	0.5	V
	Fall time	C <sub>LOAD</sub> = 3.3 nF, VC = 10 V Guaranteed by design		40		ns
	Rise time	C <sub>LOAD</sub> = 3.3 nF, VC = 10 V Guaranteed by design		45		ns

Table 6. Electrical characteristics - SMPS section (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
	Peak source current	$C_{LOAD} = 3.3 \text{ nF}$ , $V_C = 10 \text{ V}$ Guaranteed by design		800		mA
	Peak sink current	$C_{LOAD} = 3.3 \text{ nF}$ , $V_C = 10 \text{ V}$ Guaranteed by design		1		A
<b>Thermal shutdown</b>						
	Shutdown temp.	Always active; Guaranteed by design		160		°C
	Shutdown hyst.			30		°C
<b>Sleep mode</b>						
	ENSL threshold	ENSL falling	<b>1.7</b>	1.85	<b>1.95</b>	V
	ENSL hysteresis	Guaranteed by design		0.1		V
	ENDC threshold	ENDC falling	<b>1.7</b>	1.85	<b>1.95</b>	V
	ENDC hysteresis			0.1		V
<b>VC regulation</b>						
VC	Internal default		<b>7.7</b>	8.0	<b>8.3</b>	V
	VC current limit	$I_B = 0$ ; GAT1, GAT2 = open	<b>14</b>	20		mA
$V_{C_{UVLO}}$	Internal default UVLO, release	VC rising		VC-0.3		V
	Internal default; UVLO, lockout	VC falling	5.7	6.0	<b>6.3</b>	V
	VC regulator dropout	$I_C = 10 \text{ mA}$ ; GAT1, GAT2 = open		2		V
<b>VB regulation</b>						
VB	Internal default		<b>4.85</b>	5.0	<b>5.15</b>	V
	VB current capability	$I_C = 0$ ; GAT1, GAT2 = open	5		10	mA
	VB sink current capability				<b>1</b>	mA
<b>Auxiliary source detection</b>						
	SA threshold		<b>1.1</b>	1.2	<b>1.3</b>	V
	SA hysteresis			180		mV
	Minimum VDD voltage for aux. operations		13	15		V
<b>T2P flag</b>						
	T2P pull-up current		<b>20</b>	25	<b>30</b>	μA
	T2P pull-down resistance			45	<b>75</b>	Ω

**Table 6. Electrical characteristics - SMPS section (continued)**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
<b>Device current consumption</b>						
I <sub>ddq</sub>	VDD quiescent current	VD > V <sub>UVLO_R</sub> , VC = 12 V, CTL = 0		1.25	<b>1.5</b>	mA
	VC quiescent current	VD > V <sub>UVLO_R</sub> , VC = 12 V, CTL = 0		2	<b>2.5</b>	mA

Note:

- 1) Minimum and maximum limits are guaranteed by test, design, or statistical correlation. Typical values represent the most likely parametric norm at T<sub>A</sub> = 25 °C, and are provided for reference only.
- 2) Device thermal limitations could limit useful operating range.
- 3) he VC regulator is intended for internal use only as the startup supply of the PM8801; any additional external VC current, including the VB regulator current and external MOSFET driving current, has to be limited within the specified max current limit.

## 4 PD interface

### 4.1 Detection

In Power over Ethernet systems, the Power Sourcing Equipment (PSE) senses the Ethernet connection to detect whether the Powered Device (PD) is plugged to the cable termination by applying a small voltage (2.7 to 10 V) on the Ethernet cable and measuring the equivalent resistance in at least two successive steps. During this phase, the PD must present a resistance between 23.75 k $\Omega$  and 26.25 k $\Omega$ .

The signature resistor must be connected between the DET and VDD pins. This resistor is in-series to a pass transistor (see [Figure 3](#)) enabled only during the detection phase. No current is flowing through the signature resistor for the rest of the operative phases (classification and turn-on).

The value of the detection resistance has to be selected also taking into account the typical drop in voltage of the diode bridges. The typical value that can be used in most cases is 24.9 k $\Omega$ .

During detection, most of the circuits inside the PM8801 are disabled to minimize the offset current.

### 4.2 Classification

The classification phase in a PoE network is the feature that allows PSE to plan and allocate the available power to the appliances connected to various Ethernet ports.

PM8801 complies with both IEEE802.3at 1-event and 2-event classification schemes. 1-event classification in IEEE802.3at is the same as specified in the IEEE 802.3af standard, which divides the power levels below 12.95 W into 5 classes (Class 0 to Class 4).

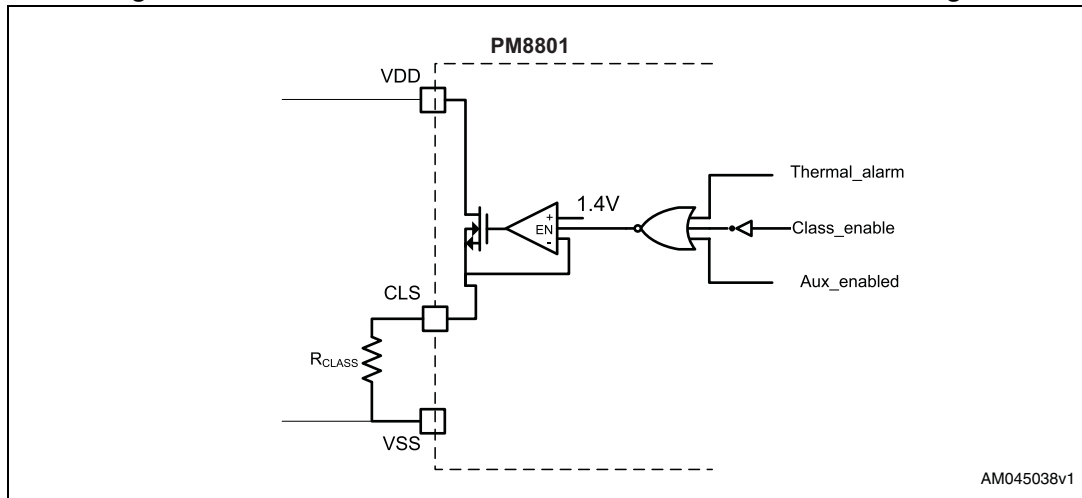
While Class 4 was reserved in IEEE802.3af, in IEEE802.3at Class 4 identifies Type2 PDs requiring up to 25.5 W.

A Type2 PD is a PD that provides a Class 4 signature during Physical Layer classification, understands 2-event classification and is capable of Data Link Layer classification.

[Figure 8](#) represents the voltage at the input of the PD when connected to a PSE performing 2-event classification. A Type2 PD will present in both classification events a Class 4 current, while during the so called "mark-event", between the 2 classification fingers, the PD will present an invalid signature resistance.

To support the classification function, an equivalent programmable constant current generator has been implemented. [Figure 6](#) depicts the primary schematic of the classification circuit. Following the successful completion of the detection phase, the voltage of the CLS pin is set to the 1.4 V voltage reference and a pass transistor connects the VIN pin to the CLS pin.

Figure 6. PM8801: reference schematic of the PoE classification logic



The classification resistor can be disconnected for the following reasons:

- the classification has been successfully completed
- an auxiliary power source has been connected
- the device is in thermal protection.

Designers can set the current by changing the value of the external resistor according to the following table.

Table 7. Value of the external classification resistor for the different PD classes of power

Class	PD max average power (W)	R <sub>CLS</sub> (Ω)
0	13	2 k
1	3.84	150
2	6.49	80.6
3	13	51.1
4	25.5	35.6

### 4.3 Indication of successful 2-event classification

PM8801 is capable of recognizing whether it is connected to a PSE performing physical layer classification by asserting the T2P signal.

T2P is an open-drain, active-low signal which is pulled down in case a successful 2-event classification event is completed.

T2P will be asserted as soon as the high-voltage startup regulator output is stable (see [Figure 7](#) and [Figure 8](#) for timing sequences). If PM8801 sees a 1-event classification or no classification, T2P is pulled up and the main circuit in the PD can try to establish an LLDP connection to negotiate the power. No LLDP response from the PSE means that the PD is connected to a Type1 PSE, and only 13 W input power will be available.

A low T2P signal after the turn-on phase of the PD means that the device is connected to a Type2, 2-event physical layer classification PSE which may allocate power either through further LLDP negotiation or directly feeding the PD with the required power.

In isolated applications, the main circuits and the PM8801 are at both sides of the galvanic isolation. The T2P signal is normally connected to an optocoupler to pass the Type 2, 2-event PSE detection information to the main circuit in the PD system.

Figure 7. T2P signal when connected to PSE supporting 1-event classification

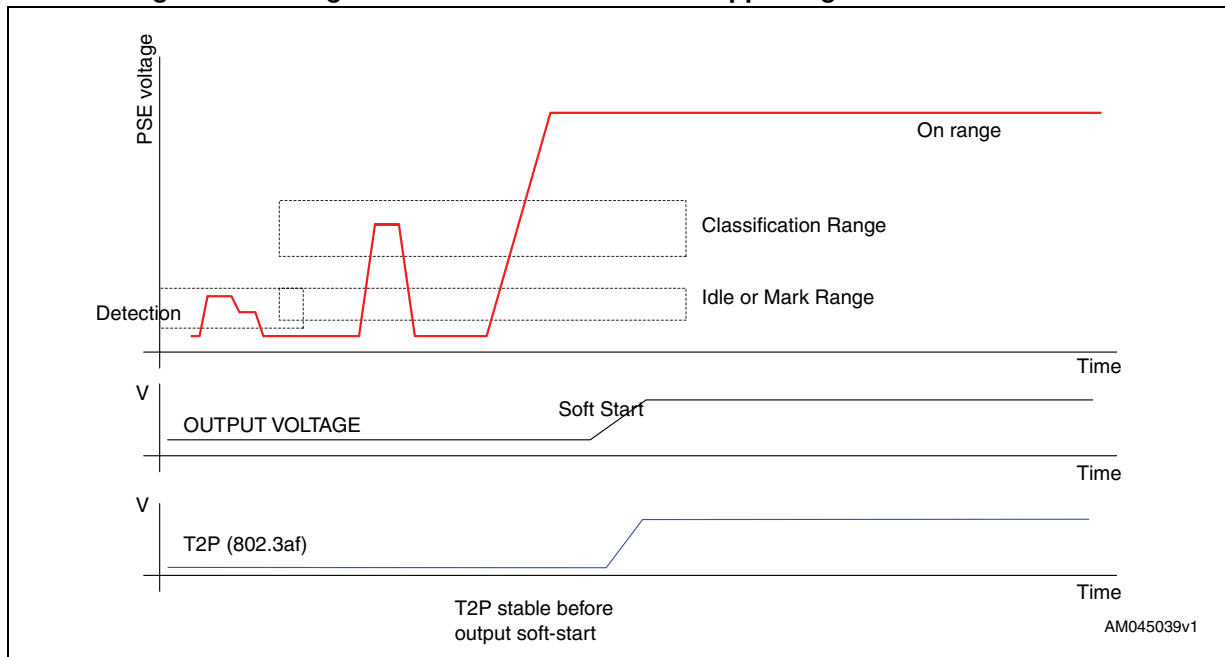
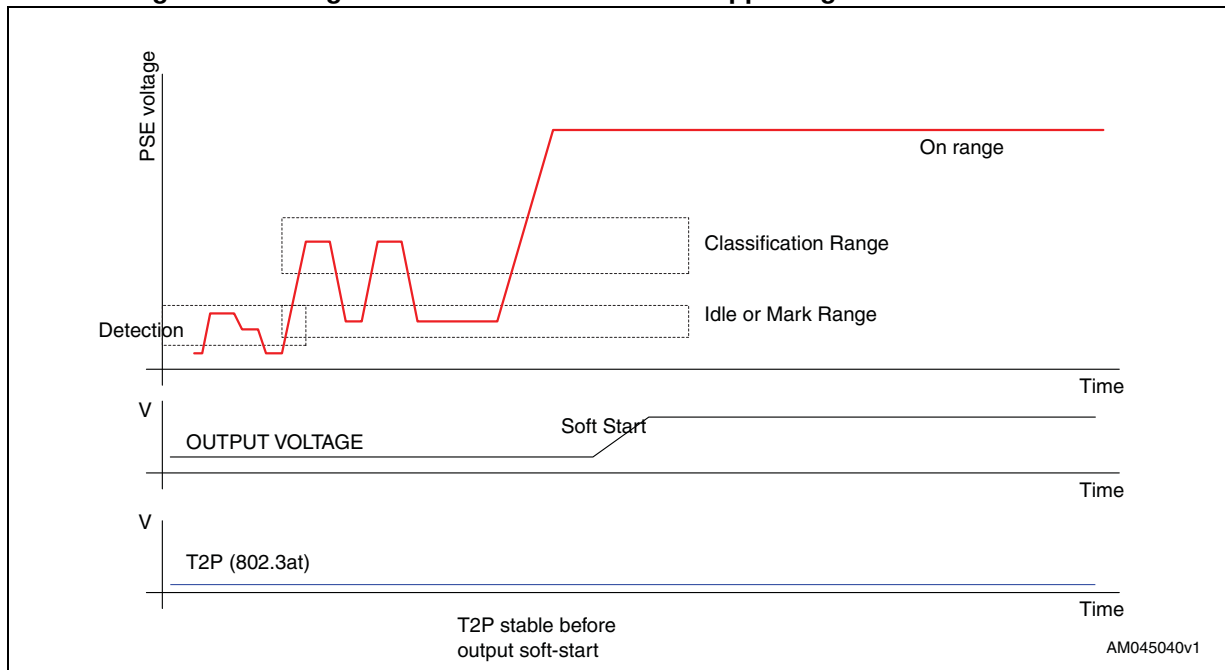


Figure 8. T2P signal when connected to PSE supporting 2-event classification





## 4.4 Undervoltage lockout

After classification is completed, the PSE raises the voltage to provide the Powered Device with the negotiated power. During the transition from low to operating voltage, the internal UVLO is released and the hot-swap MOSFET is activated, initiating the inrush sequence.

PM8801 implements the UVLO mechanism by setting 2 internal thresholds on the voltage across the VDD-VSS pins. One is to activate the hot-swap ( $V_{UVLO\_R}$ ), while the other is to switch off the hot-swap MOSFET upon detection of a supply voltage drop ( $V_{UVLO\_F}$ ) from normal operating conditions.

No additional external components are required to comply with the IEEE requirements. The thermal protection alarm overrides the gate driving of the MOS, immediately switching off the MOS itself in case of device overheating. The hot-swap is bypassed also in auxiliary source topology, supplying directly the PWM section of the PM8801 and bypassing the hot-swap MOSFET.

## 4.5 Inrush and DC current limiting

Once the detection and classification phases have been successfully completed, the PSE raises the voltage across the Ethernet cable. When the voltage difference between VIN and VSS is greater than the  $V_{UVLO\_R}$  threshold, the internal hot-swap MOSFET is switched on and the DC/DC input capacitance is charged in a controlled manner.

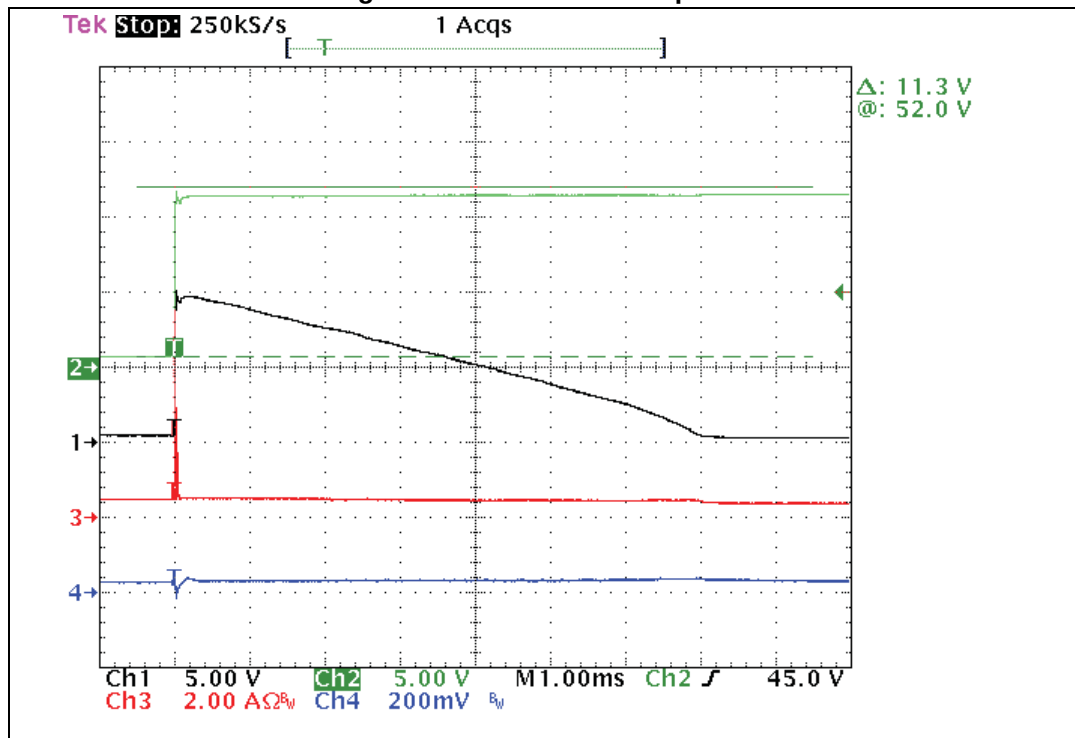
During the inrush phase the current is limited to 140 mA.

When the RTN voltage falls below 1.5 V, an internal signal (PGOOD in [Figure 3](#)) is asserted to activate the DC/DC section.

This feature is active only when working from an input voltage with a "frontal" connection, that must use the hot-swap MOSFET; this voltage could be from the PoE interface or from an external auxiliary adapter connected before the internal hot-swap MOSFET. If the auxiliary source is connected after the hot-swap MOSFET, it will be opened and this feature is disabled, allowing the converter to work with a low-voltage auxiliary source. The PGOOD comparator includes hysteresis to allow the PM8801 to operate near the current limit point without inadvertently disabling it. The MOSFET voltage must increase to 12 V before PGOOD is deasserted. This feature will also allow withstanding positive line transients of up to 12 V without stopping DC/DC normal operations as shown in [Figure 9](#). The line transient is managed by the PWM section, adjusting its operating parameters accordingly without shutting down the output voltage. The input current during the transient is controlled by the hot-swap MOSFET at the DC current limit.

After PGOOD assertion, a comparator on the gate of the hot-swap MOSFET controls the transition between the 140 mA to the 640mA DC current limit, with a 2 V threshold. The comparator is needed to ensure that the charge of the DC/DC input capacitor is completed, avoiding current spikes on the last portion of the charge.

Figure 9. Line transient response



Ch1: RTN - VSS, Ch2: VDD - VSS, Ch3: I input, Ch4: 5Vout (with offset)

## 4.6 Sleep mode / MPS mode

It is possible to put the PM8801 in sleep mode for applications connected to either a PoE network or auxiliary sources. In both cases the DC/DC converter is turned off. The device draws a minimum current and the LED is activated (see [Section 4.7](#) for details).

The sleep mode is activated by pulling ENSL below its internal threshold. The ENSL pin is a logic level active-low input. The ENSL pin may be connected to a system microcontroller through an optocoupler.

When working from a PoE network or from a frontal auxiliary source, the internal hot-swap MOSFET is opened and the DC/DC section shuts down. In this condition the PD consumption is very low and for this reason it may be disconnected by the PSE.

To avoid this disconnection the PM8801 features a Maintain Power Signature (MPS) current control. The device will keep on drawing a current whose profile is determined by sampling the level of ENDC when entering sleep mode. The ENDC pin is designed to receive the signal from a system microcontroller connected through an optocoupler.

According to the IEEE802.3at standard, continuous or pulsed MPS profiles are available.

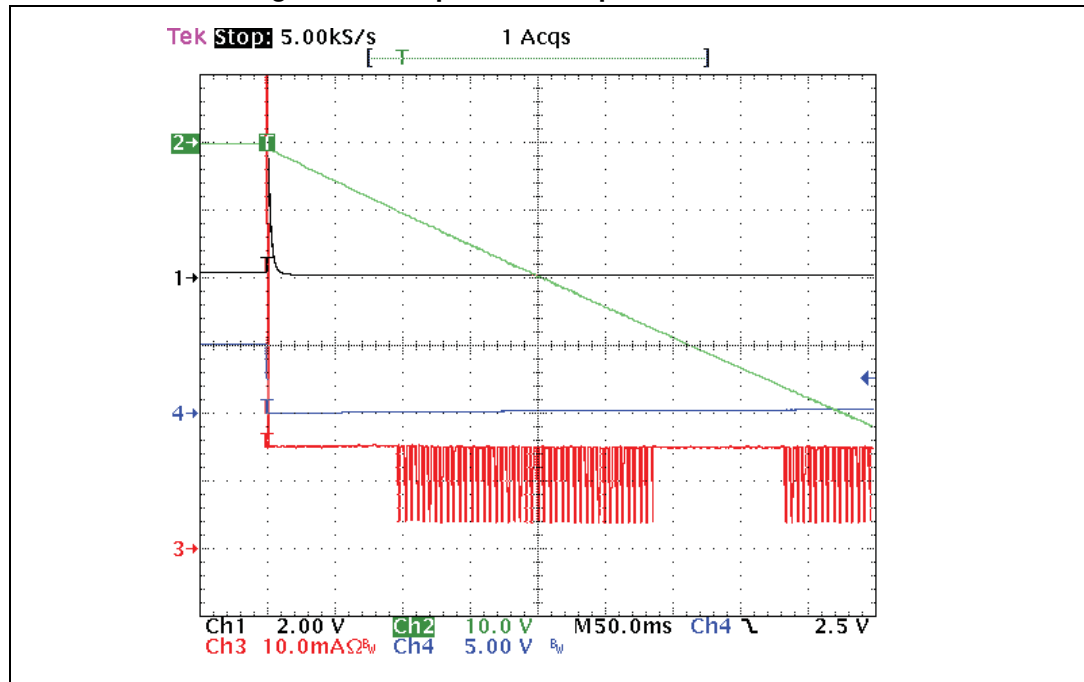
Pulsed MPS is obtained by 100 ms pulses of 12 mA current, followed by 200 ms of MPS dropout as shown in [Figure 10](#). This profile is obtained with ENDC = low when entering sleep mode.

Constant current MPS is a 12 mA constant current drawn during the entire duration of the sleep mode. This profile is obtained with ENDC = high when entering sleep mode.

In case of thermal shutdown, MPS is released, making sure that current consumption is below the threshold and allowing the PSE to detach the PD.

When the PM8801 is powered by an auxiliary source (see [Section 6](#)), the MPS current is not activated.

**Figure 10. Sleep mode with pulsed MPS current**



Ch1: ENSL, Ch2: VSS-RTN. Ch3: Iinput, Ch4: 5Vout

## 4.7 LED driving

The PM8801 features a current-driven LED output. The LED is enabled when the ENDC pin is driven high, or automatically enabled in sleep mode.

The LED driver sources a PWM current at 250 Hz frequency and 12 mA typical amplitude.

The LED brightness is adjustable connecting a resistor  $R_{DC}$  at 1% accuracy between DIM and VSS. The correspondence between duty-cycle and resistor values are shown in the following [Table 8](#).

**Table 8. LED duty cycle selection**

LED duty cycle D	$R_D [\Omega]$
0	>1 M
15%	453 k
33%	243 k
47%	162 k
75%	110 k

To minimize current consumption during sleep mode, the MPS current is obtained by:

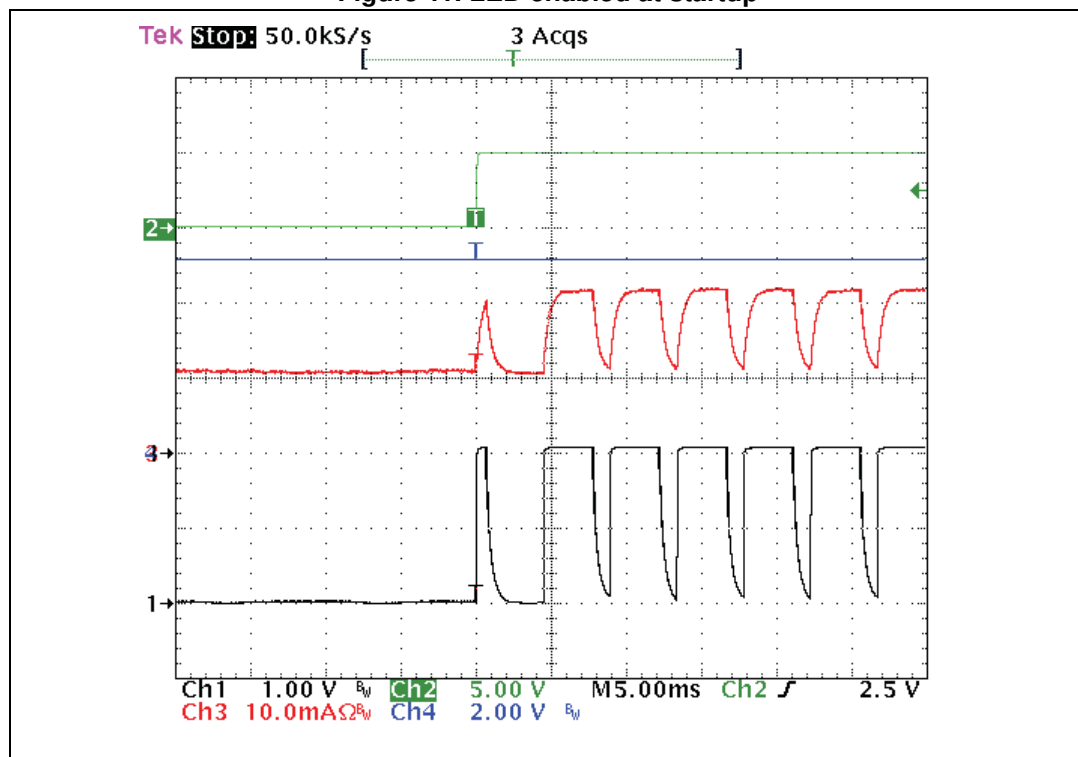
- the 12 mA driving LED current when the LED is on
- an internal 12 mA sink when the LED is off

This behavior ensures a 12 mA constant MPS current shape when the MPS is on.

During MPS dropout the consumption is due only to the quiescent current and the average LED driving current.

$$I_{MPDO} = I_{ddq} + D \cdot I_{LED}$$

Figure 11. LED enabled at startup



Ch1: LED, Ch2: ENDC, Ch3: Iinput, Ch4: 5Vout

LED signal will be present also in the case an auxiliary source is used in place of PoE.

If both PoE and auxiliary source are connected, the PoE interface is not providing power to the DC/DC section, but still provides current to the LED.

When working from an auxiliary source, if the system requires disconnection from the PSE, it is suggested to turn off the LED for at least 400 msec after insertion of the auxiliary power jack.