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PMBFJ111; PMBFJ112; PMBFJ113

N-channel junction FETs

Rev. 4 — 20 September 2011 Product data sheet

1. Product profile

1.1 General description

Symmetrical N-channel junction FETs in a SOT23 package.

1.2 Features and benefits

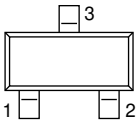
- High-speed switching
- Interchangeability of drain and source connections
- Low R_{DSon} at zero gate voltage (< 30 Ω for PMBFJ111).

1.3 Applications

- Analog switches
- Choppers
- Commutators
- Multiplexers
- Thin and thick film hybrids.

2. Pinning information

Table 1. Pinning

Pin	Description[1]	Simplified outline	Symbol
1	drain		
2	source		
3	gate		

sym053

[1] Drain and source are interchangeable.

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PMBFJ111	-	plastic surface mounted package; 3 leads	SOT23
PMBFJ112			
PMBFJ113			

4. Marking

Table 3. Marking

Type number	Marking code[1]
PMBFJ111	41*
PMBFJ112	42*
PMBFJ113	47*

[1] * = p: Made in Hong Kong
* = t: Made in Malaysia
* = W: Made in China

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage (DC)			-	±40	V
V_{GSO}	gate-source voltage			-	–40	V
V_{GDO}	gate-drain voltage			-	–40	V
I_G	forward gate current (DC)			-	50	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C	[1]	-	300	mW
T_{stg}	storage temperature			–65	+150	°C
T_j	junction temperature			-	150	°C

[1] Mounted on a ceramic substrate, 8 mm × 10 mm × 0.7 mm.

6. Thermal characteristics

Table 5. Thermal characteristics

$T_j = P\ (R_{th(j-t)} + R_{th(t-s)} + R_{th(s-a)}) + T_{amb}$.

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	430	K/W
	thermal resistance from junction to ambient		[2]	500	K/W

[1] Mounted on a ceramic substrate, 8 mm × 10 mm × 0.7 mm.

[2] Mounted on printed circuit board.

7. Static characteristics

Table 6. Static characteristics

T_j = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{GSS}	gate-source leakage current	V_{GS} = −15 V; V_{DS} = 0 V	-	-	−1	nA
I_{DSS}	drain-source leakage current					
	PMBFJ111	V_{GS} = 0 V; V_{DS} = 15 V	20	-	-	mA
	PMBFJ112	V_{GS} = 0 V; V_{DS} = 15 V	5	-	-	mA
	PMBFJ113	V_{GS} = 0 V; V_{DS} = 15 V	2	-	-	mA
$V_{(BR)GSS}$	gate-source breakdown voltage	I_G = −1 μA; V_{DS} = 0 V	−40	-	-	V
V_{GSoff}	gate-source cut-off voltage					
	PMBFJ111	I_D = 1 μA; V_{DS} = 5 V	−10	-	−3	V
	PMBFJ112	I_D = 1 μA; V_{DS} = 5 V	−5	-	−1	V
	PMBFJ113	I_D = 1 μA; V_{DS} = 5 V	−3	-	−0.5	V
R_{DSon}	drain-source on-state resistance					
	PMBFJ111	V_{GS} = 0 V; V_{DS} = 0.1 V	-	-	30	Ω
	PMBFJ112	V_{GS} = 0 V; V_{DS} = 0.1 V	-	-	50	Ω
	PMBFJ113	V_{GS} = 0 V; V_{DS} = 0.1 V	-	-	100	Ω

8. Dynamic characteristics

Table 7. Dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_{iss}	input capacitance	V_{DS} = 0 V; V_{GS} = −10 V; f = 1 MHz		-	6	-	pF
		V_{DS} = 0 V; V_{GS} = 0 V; f = 1 MHz; T_{amb} = 25 °C		-	22	28	pF
C_{rss}	feedback capacitance			-	3	-	pF
Switching times; see Figure 2							
t_r	rise time		[1]	-	6	-	ns
t_{on}	turn-on time		[1]	-	13	-	ns
t_f	fall time		[1]	-	15	-	ns
t_{off}	turn-off time		[1]	-	35	-	ns

[1] Test conditions for switching times are as follows:
V_{DD} = 10 V, V_{GS} = 0 V to V_{GSoff} (all types);
V_{GSoff} = −12 V, R_L = 750 Ω (PMBFJ111);
V_{GSoff} = −7 V, R_L = 1550 Ω (PMBFJ112);
V_{GSoff} = −5 V, R_L = 3150 Ω (PMBFJ113).

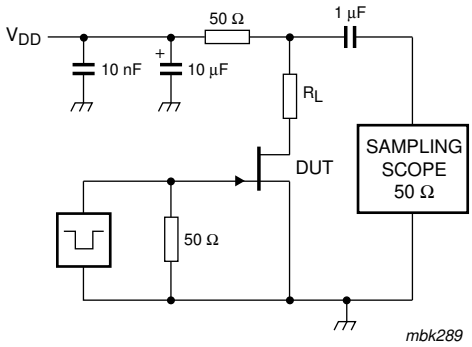


Fig 1. Switching circuit.

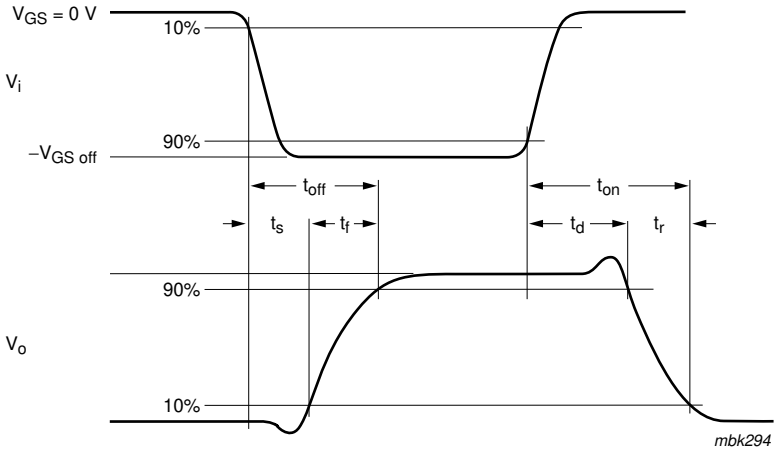
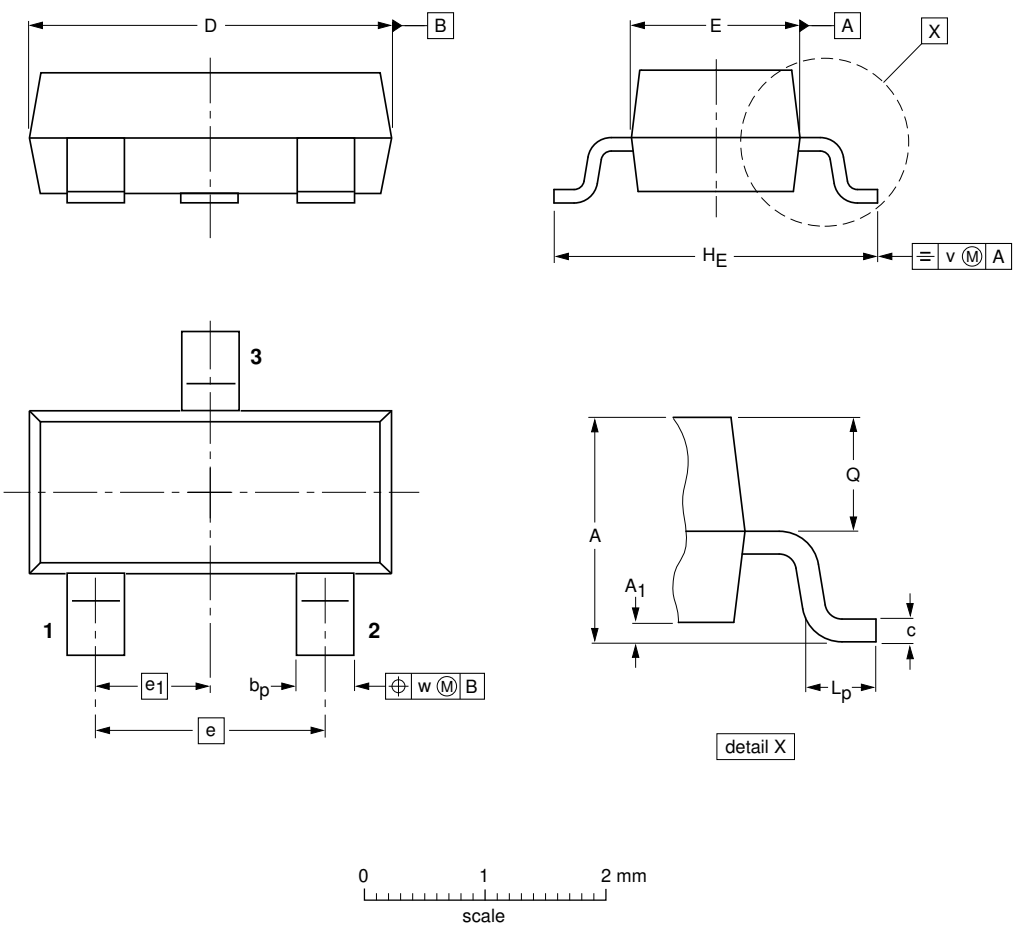


Fig 2. Input and output waveforms.

9. Package outline

Plastic surface-mounted package; 3 leads **SOT23**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT23		TO-236AB				~~04-11-04~~ 06-03-16

Fig 3. Package outline.

10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMBFJ111_112_113 v.4	20110920	Product data sheet	-	PMBFJ111_112_113 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Package outline drawings have been updated to the latest version.			
PMBFJ111_112_113 v.3 (9397 750 13402)	20040804	Product data sheet	-	PMBFJ111_112_113_CNV v.2
PMBFJ111_112_113_CNV v.2	19971201	Product specification	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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13. Contents

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