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Team Nexperia

# PMK50XP

## P-channel TrenchMOS extremely low level FET

Rev. 02 — 28 April 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Extremely low level P-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance

### 1.3 Applications

- Battery management
- Load switching

### 1.4 Quick reference data

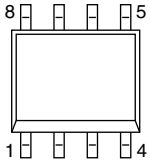
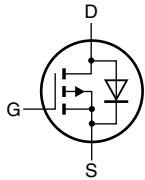
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	-20	V
$I_D$	drain current	$T_{sp} = 25\text{ °C}$ ; $V_{GS} = -4.5\text{ V}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	-	-7.9	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	5	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}$ ; $I_D = -2.8\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	40	50	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = -4.5\text{ V}$ ; $I_D = -4.7\text{ A}$ ; $V_{DS} = -10\text{ V}$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	1.3	-	nC



## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>SOT96-1 (SO8)</b></p>	 <p>003aaa671</p>
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

## 3. Ordering information

**Table 3. Ordering information**

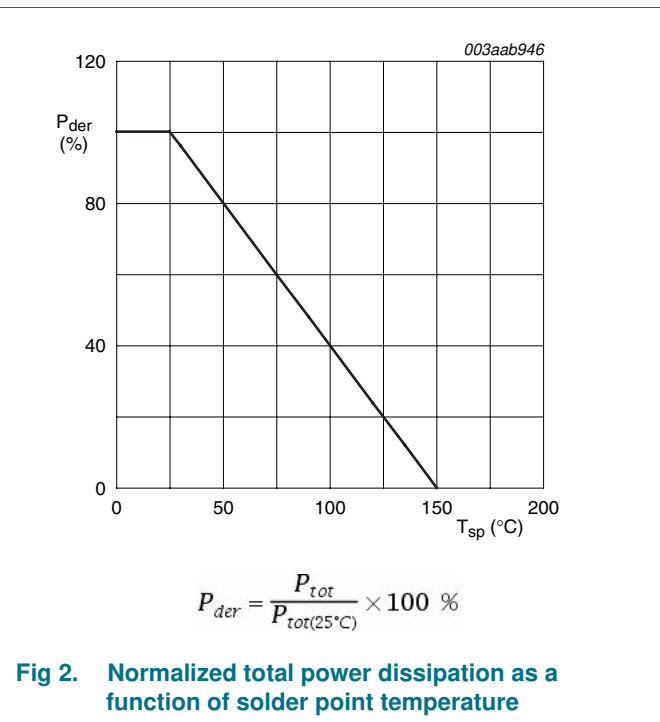
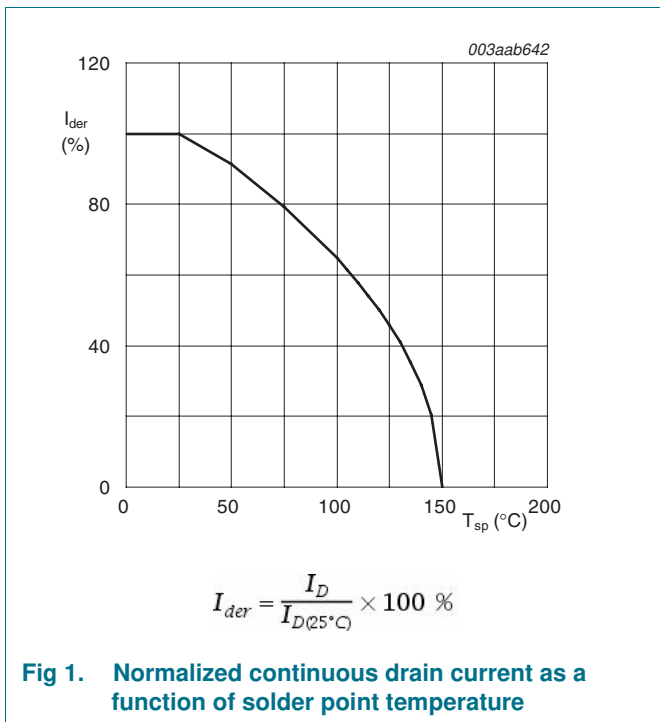
Type number	Package		Version
	Name	Description	
PMK50XP	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

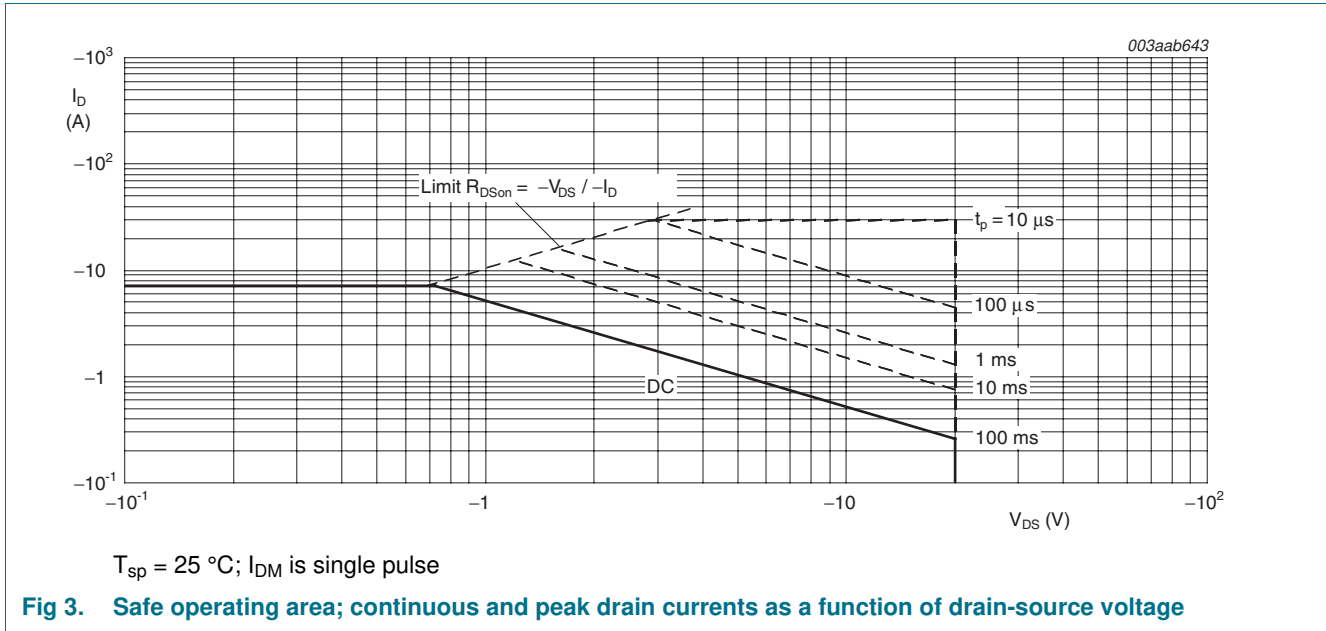
### 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 150 °C	-	-	-20	V
V <sub>DGR</sub>	drain-gate voltage	25 °C ≤ T <sub>j</sub> ≤ 150 °C; R <sub>GS</sub> = 20 kΩ	-	-	-20	V
V <sub>GS</sub>	gate-source voltage		-12	-	12	V
I <sub>D</sub>	drain current	T <sub>sp</sub> = 25 °C; V <sub>GS</sub> = -4.5 V; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	-	-7.9	A
		T <sub>sp</sub> = 100 °C; V <sub>GS</sub> = -4.5 V; see <a href="#">Figure 1</a>	-	-	-5	A
I <sub>DM</sub>	peak drain current	T <sub>sp</sub> = 25 °C; t <sub>p</sub> ≤ 10 μs; pulsed; see <a href="#">Figure 3</a>	-	-	-31.6	A
P <sub>tot</sub>	total power dissipation	T <sub>sp</sub> = 25 °C; see <a href="#">Figure 2</a>	-	-	5	W
T <sub>stg</sub>	storage temperature		-55	-	150	°C
T <sub>j</sub>	junction temperature		-55	-	150	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>sp</sub> = 25 °C	-	-	-4.1	A
I <sub>SM</sub>	peak source current	T <sub>sp</sub> = 25 °C; t <sub>p</sub> ≤ 10 μs; pulsed	-	-	-16.4	A

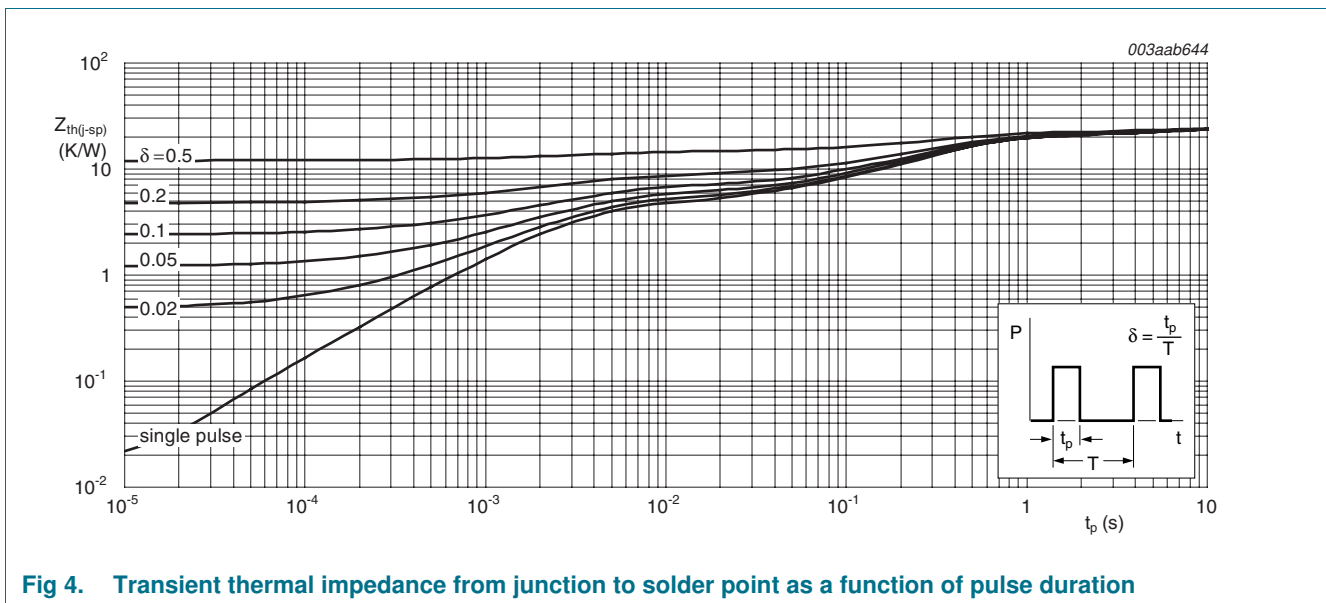




### 5. Thermal characteristics

Table 5. Thermal characteristics

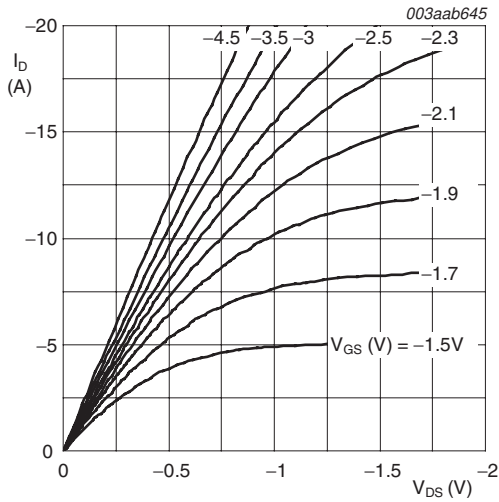
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see <a href="#">Figure 4</a>	-	-	25	K/W



## 6. Characteristics

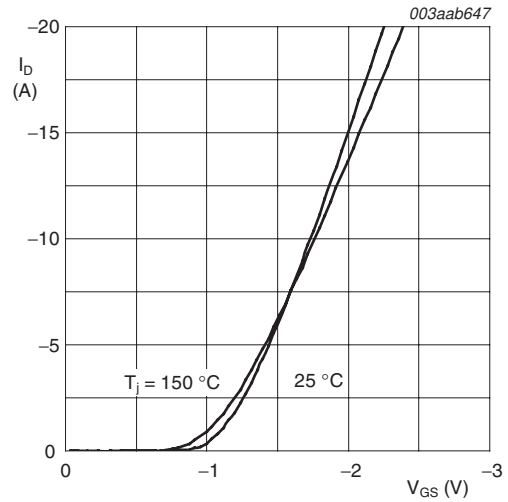
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	-18	-	-	V
		$I_D = -250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-20	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = -250 \mu\text{A}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-	-	-1.1	V
		$I_D = -250 \mu\text{A}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-0.35	-	-	V
		$I_D = -250 \mu\text{A}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-0.55	-0.75	-0.95	V
$I_{DSS}$	drain leakage current	$V_{DS} = -20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	$\mu\text{A}$
		$V_{DS} = -20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 70 \text{ }^\circ\text{C}$	-	-	-5	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 12 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-10	-100	nA
		$V_{GS} = -12 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-10	-100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -2.5 \text{ V}; I_D = -2.3 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	56	70	m $\Omega$
		$V_{GS} = -4.5 \text{ V}; I_D = -2.8 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	64	80	m $\Omega$
		$V_{GS} = -4.5 \text{ V}; I_D = -2.8 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	40	50	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = -4.7 \text{ A}; V_{DS} = -10 \text{ V}; V_{GS} = -4.5 \text{ V};$ see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	10	-	nC
$Q_{GS}$	gate-source charge		-	2.2	-	nC
$Q_{GD}$	gate-drain charge		-	1.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = -4.7 \text{ A}; V_{DS} = -10 \text{ V};$ see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	-1.6	-	V
$C_{iss}$	input capacitance	$V_{DS} = -20 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a>	-	1020	-	pF
$C_{oss}$	output capacitance		-	140	-	pF
$C_{rss}$	reverse transfer capacitance		-	100	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 \text{ V}; R_L = 10 \text{ } \Omega; V_{GS} = -4.5 \text{ V};$ $R_{G(ext)} = 6 \text{ } \Omega$	-	8.5	-	ns
$t_r$	rise time		-	7.5	-	ns
$t_{d(off)}$	turn-off delay time		-	82	-	ns
$t_f$	fall time		-	35	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = -1.7 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 14</a>	-	-0.77	-1.2	V



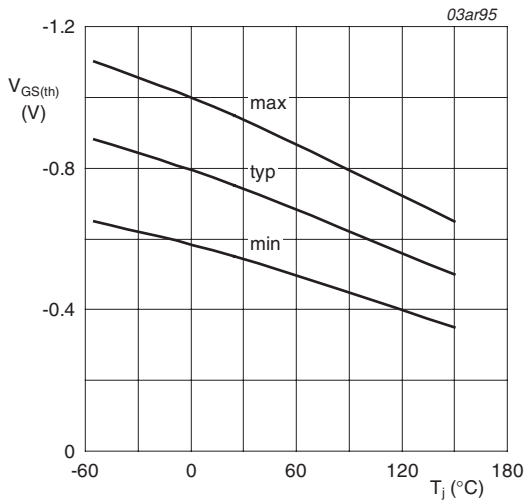
$T_j = 25\text{ }^\circ\text{C}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



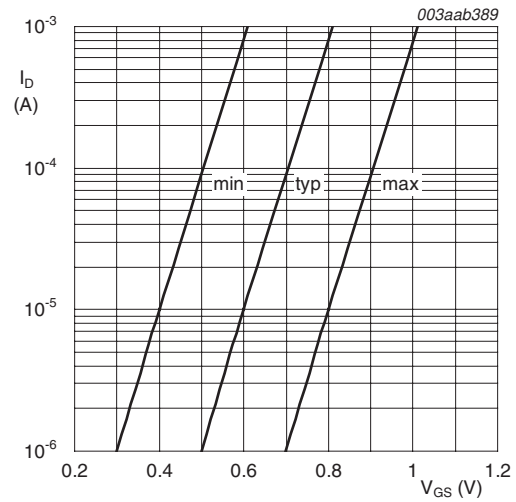
$V_{DS} > I_D \times R_{DS(on)}$

**Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



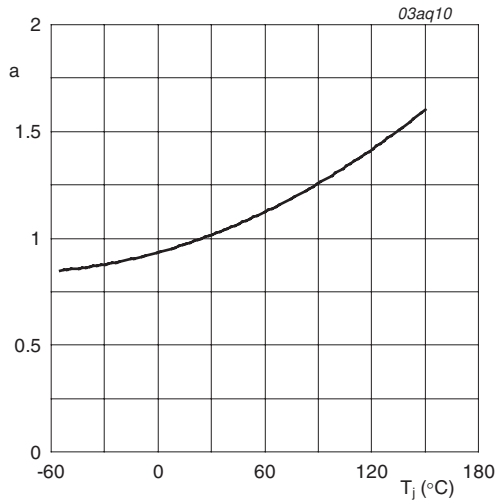
$I_D = -0.25\text{ mA}; V_{DS} = V_{GS}$

**Fig 7. Gate-source threshold voltage as a function of junction temperature**



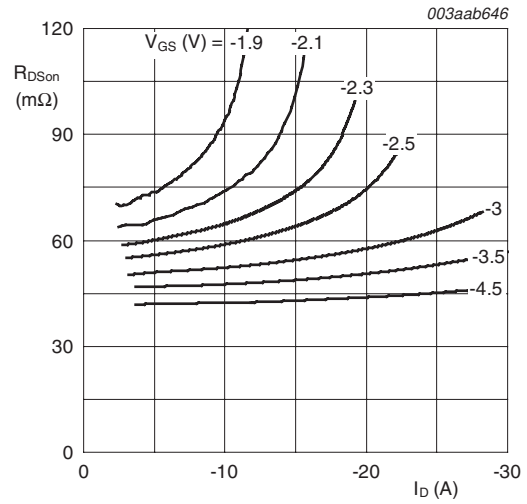
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = -5\text{ V}$

**Fig 8. Sub-threshold drain current as a function of gate-source voltage**



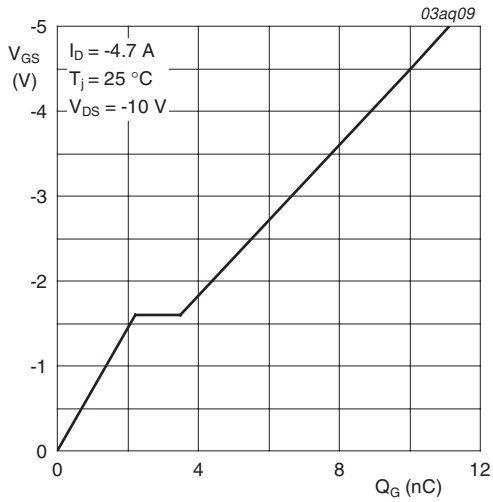
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature



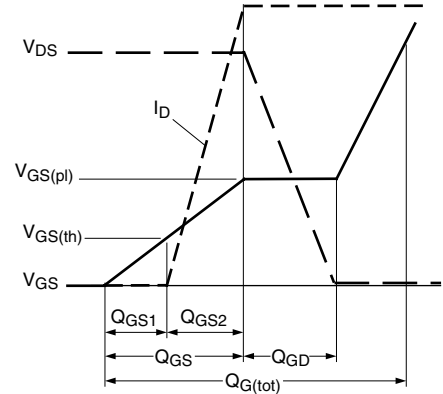
$T_j = 25^{\circ}C$

Fig 10. Drain-source on-state resistance as a function of drain current; typical values



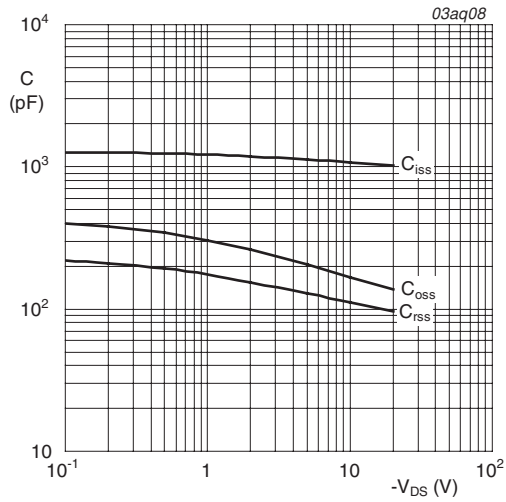
$I_D = -4.7 A; T_j = 25^{\circ}C; V_{DS} = -10 V$

Fig 11. Gate-source voltage as a function of gate charge; typical values



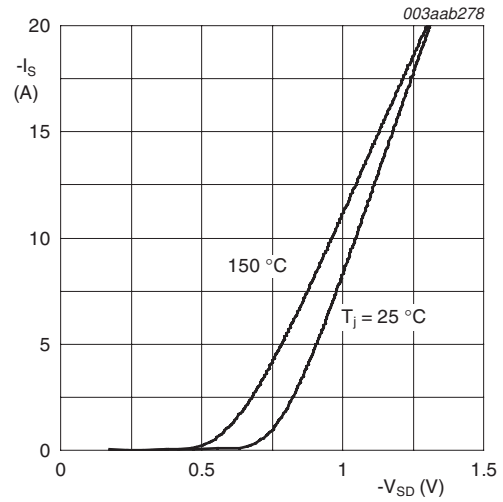
003aaa508

Fig 12. Gate charge waveform definitions



V<sub>GS</sub> = 0 V; f = 1 MHz

**Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



V<sub>GS</sub> = 0 V

**Fig 14. Source current as a function of source-drain voltage; typical values**

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

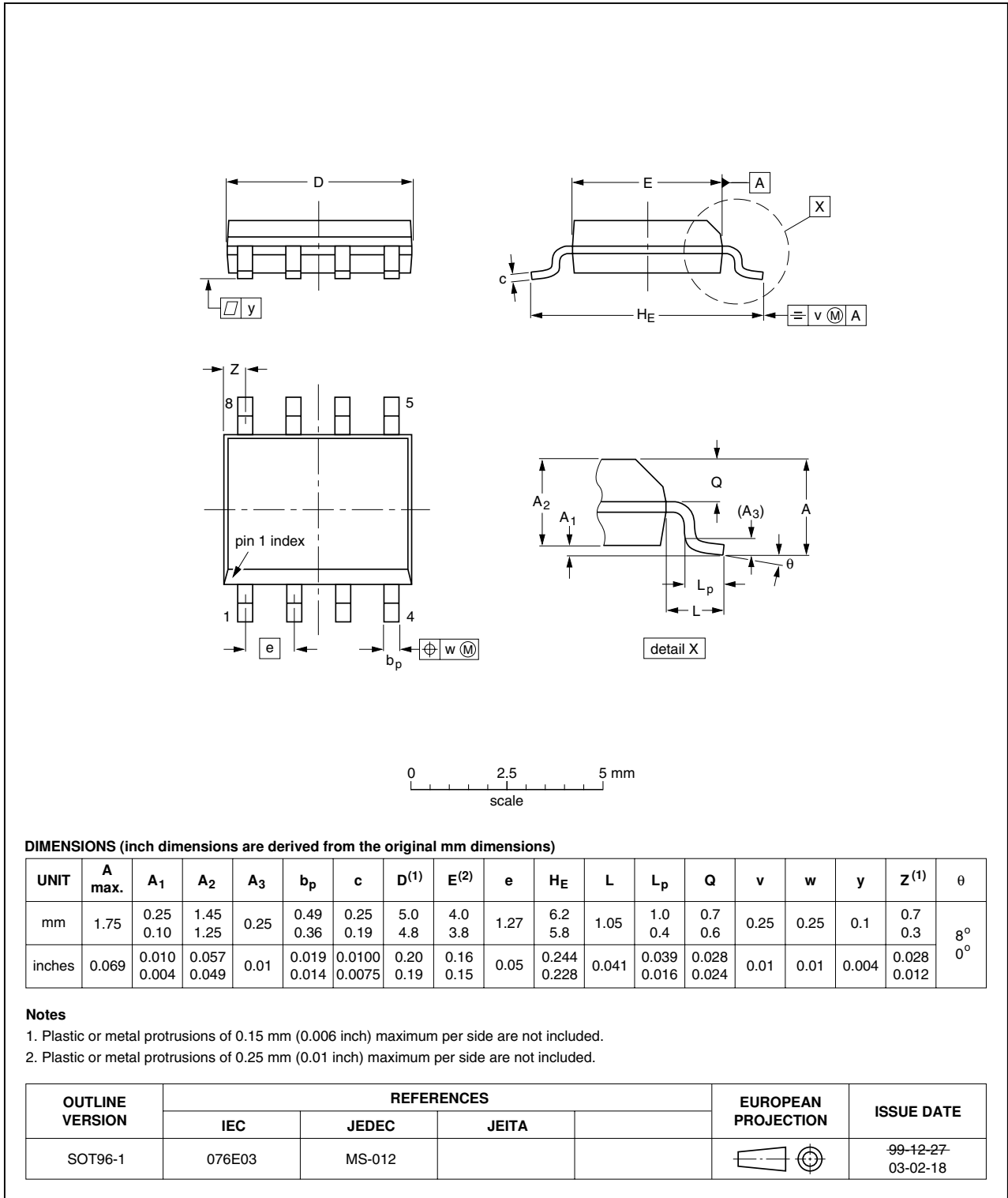


Fig 15. Package outline SOT96-1 (SO8)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMK50XP_2	20100428	Product data sheet	-	PMK50XP_1
Modifications:	• Various changes to content.			
PMK50XP_1	20070917	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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