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Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- · Logic-level compatible
- · Very fast switching
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

3. Applications

- · Relay driver
- · High-speed line driver
- · Low-side loadswitch
- · Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j = 25 °C		-	-	60	V
V_{GS}	gate-source voltage			-20	-	20	V
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-	3.1	Α
Static characte	Static characteristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 2.4 \text{ A}; T_j = 25 \text{ °C}$		-	96	123	mΩ

^[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain		D
2	D	drain		
3	G	gate	0 1 1 2 13	G. A. T. A.
4	S	source	TSOP6 (SOT457)	
5	D	drain		
6	D	drain		8
				017aaa255

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PMN120ENE	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457			

7. Marking

Table 4. Marking codes

Type number	Marking code
PMN120ENE	3K

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _j = 25 °C		-	60	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	3.1	Α
		V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	2.4	Α
		V _{GS} = 10 V; T _{amb} = 100 °C	[1]	-	1.5	Α
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \mu s$		-	10	Α
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	570	mW
			[1]	-	1.4	W
		T _{sp} = 25 °C		-	6.25	W
Tj	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain	n diode					
I _S	source current	T _{amb} = 25 °C	[1]	-	1.4	Α

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

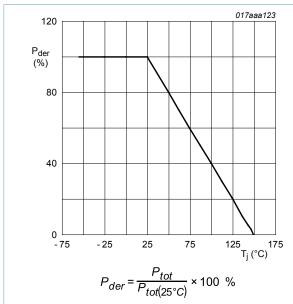


Fig. 1. Normalized total power dissipation as a function of junction temperature

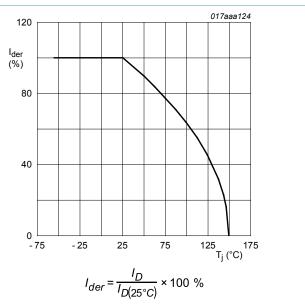


Fig. 2. Normalized continuous drain current as a function of junction temperature

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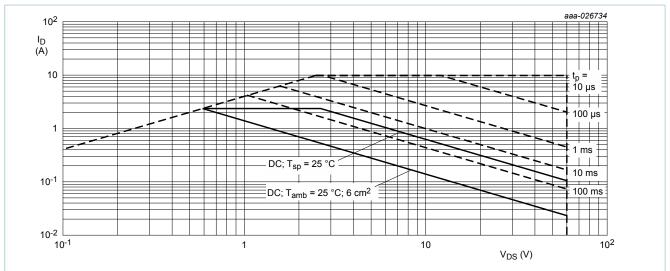


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drainsource voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient		[1]	-	190	220	K/W
			[2]	-	78	90	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	15	20	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm²

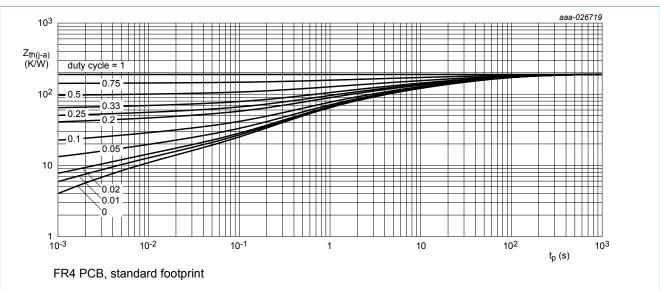
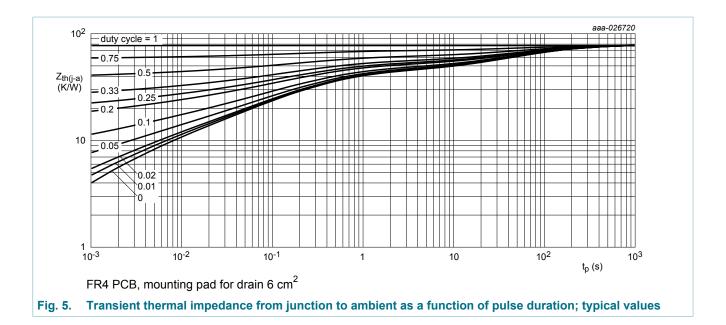


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara				.) P	inax	J.I.I.
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	60	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \ \mu A; \ V_{DS} = V_{GS}; \ T_j = 25 \ ^{\circ}C$	1.3	1.7	2.7	V
I _{DSS}	drain leakage current	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 25 °C	-	-	1	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	10	μΑ
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-10	μA
		V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C	-	-	1	μA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-1	μA
R _{DSon}	drain-source on-state	V_{GS} = 10 V; I_D = 2.4 A; T_j = 25 °C	-	96	123	mΩ
	resistance	V _{GS} = 10 V; I _D = 2.4 A; T _j = 150 °C	-	192	246	mΩ
		V_{GS} = 4.5 V; I_D = 2.2 A; T_j = 25 °C	-	108	146	mΩ
g _{fs}	forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 0.9 \text{ A}; T_j = 25 \text{ °C}$	-	10.2	-	S
R _G	gate resistance	f = 1 MHz	-	10	-	Ω
Dynamic ch	naracteristics					
Q _{G(tot)}	total gate charge	$V_{DS} = 30 \text{ V}; I_D = 2.1 \text{ A}; V_{GS} = 10 \text{ V};$	-	5.9	7.4	nC
Q _{GS}	gate-source charge	T _j = 25 °C	-	0.6	-	nC
Q _{GD}	gate-drain charge		-	1.1	-	nC
C _{iss}	input capacitance	V _{DS} = 30 V; f = 1 MHz; V _{GS} = 0 V;	-	275	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	24	-	pF
C _{rss}	reverse transfer capacitance		-	17	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 30 \text{ V}; I_D = 2.1 \text{ A}; V_{GS} = 10 \text{ V};$	-	6	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 ^{\circ}C$	-	9	-	ns
t _{d(off)}	turn-off delay time	_	-	16	-	ns
t _f	fall time	_	-	6	-	ns
Source-drai	in diode		1			,
V_{SD}	source-drain voltage	I _S = 1.4 A; V _{GS} = 0 V; T _i = 25 °C	_	0.8	1.2	V

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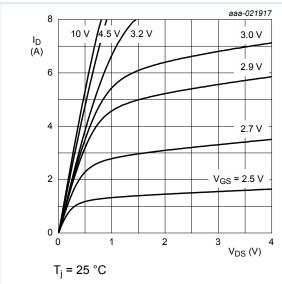


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

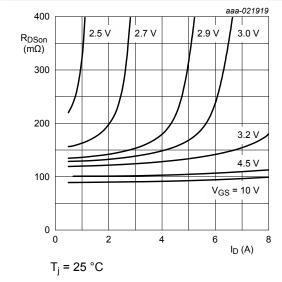


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

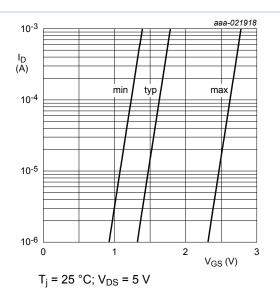


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

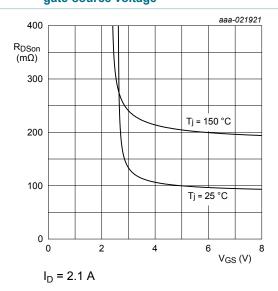


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

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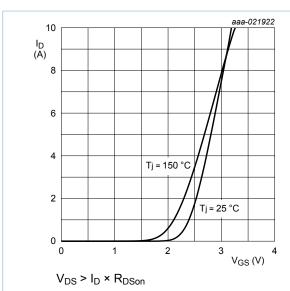


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

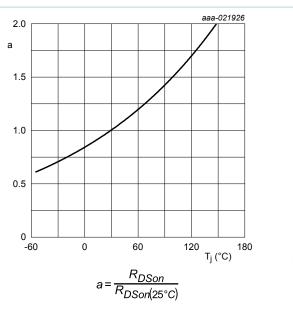


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

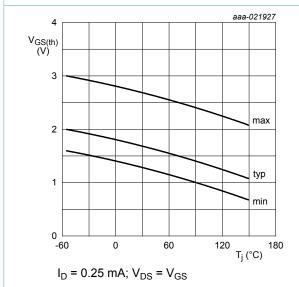
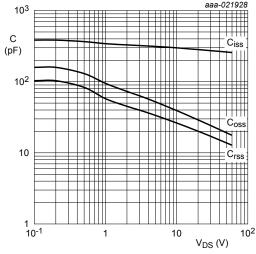


Fig. 12. Gate-source threshold voltage as a function of junction temperature



 $f = 1 MHz; V_{GS} = 0 V$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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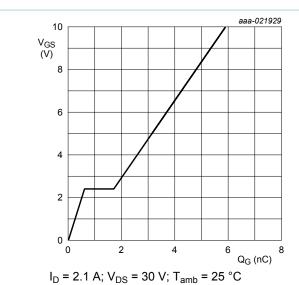


Fig. 14. Gate-source voltage as a function of gate charge; typical values

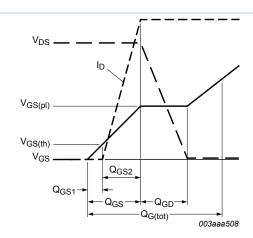


Fig. 15. Gate charge waveform definitions

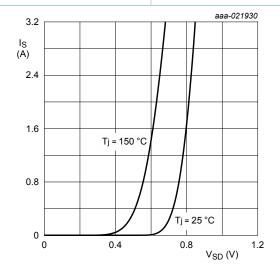
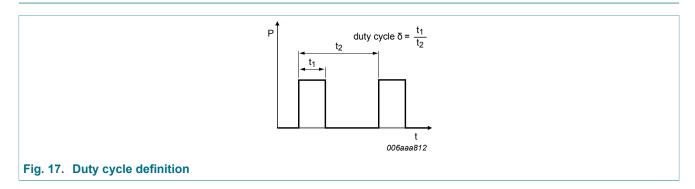


Fig. 16. Source current as a function of source-drain voltage; typical values

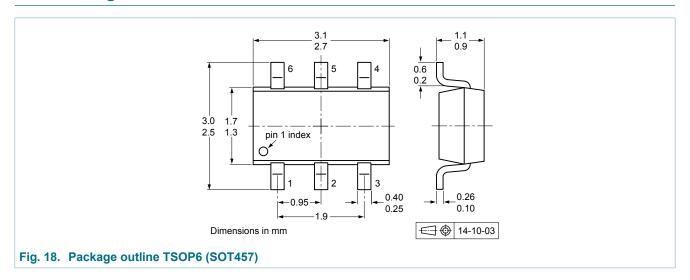
 $V_{GS} = 0 V$

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11. Test information



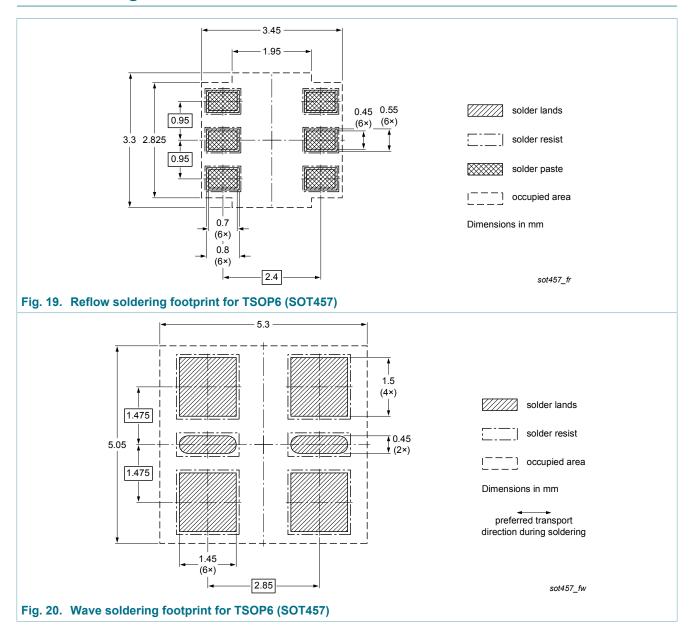
12. Package outline



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13. Soldering



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14. Revision history

Table 8. Revision history

	· y						
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes			
PMN120ENE v.2	20171214	Product data sheet	-	PMN120ENE v.1			
Modifications:	Characteristics, temperature condition removed from gate resistance.						
PMN120ENE v.1	20171127	Product data sheet	-	-			

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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