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PMN40ENE

30 V, N-channel Trench MOSFET

24 May 2016

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Logic-level compatible
- Very fast switching
- Enhanced power dissipation capability of 1240 mW
- ElectroStatic Discharge (ESD) protection > 1 kV HBM

3. Applications

- LED driver
- Power management
- Low-side loadswitch
- Switching circuits

4. Quick reference data

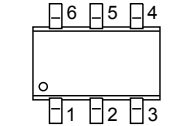
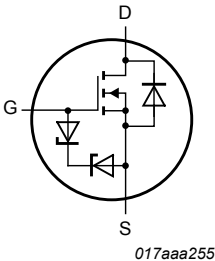
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	-	30	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-	5.7	A
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 4.5\text{ A}; T_j = 25\text{ °C}$		-	30	38	mΩ

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 TSOP6 (SOT457)	 017aaa255
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMN40ENE	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457

7. Marking

Table 4. Marking codes

Type number	Marking code
PMN40ENE	H4

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	30	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	5.7	A
		V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	4.5	A
		V _{GS} = 10 V; T _{amb} = 100 °C	[1]	-	2.9	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	18	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	530	mW
			[1]	-	1.24	W
		T _{sp} = 25 °C		-	4.46	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	1.2	A

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

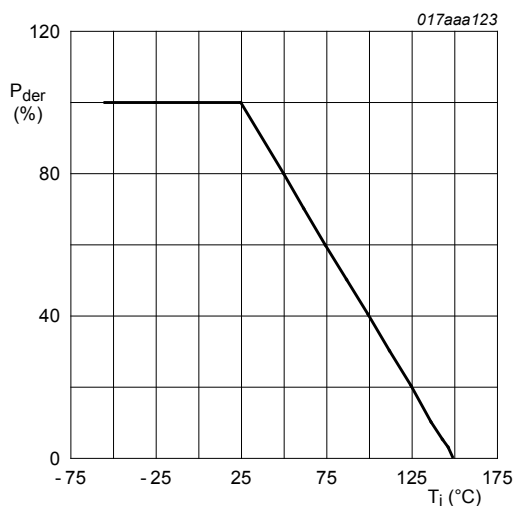


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

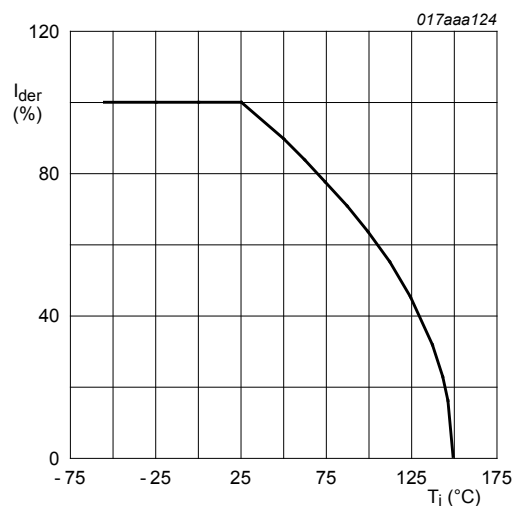
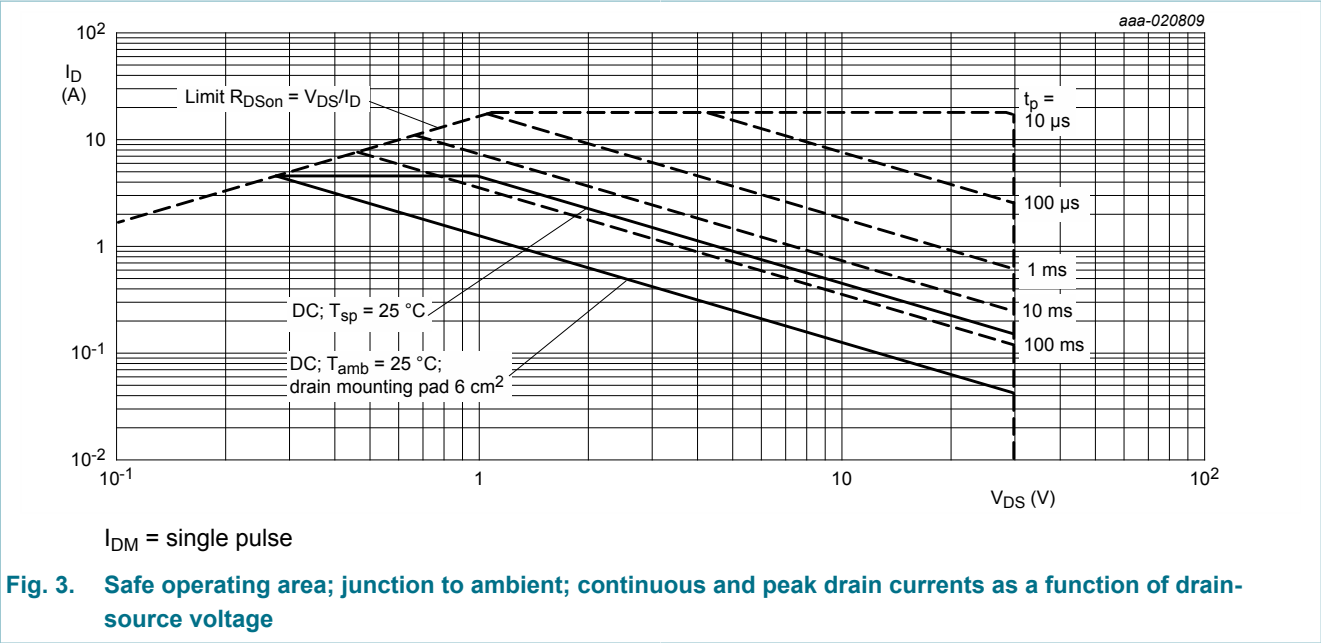


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$

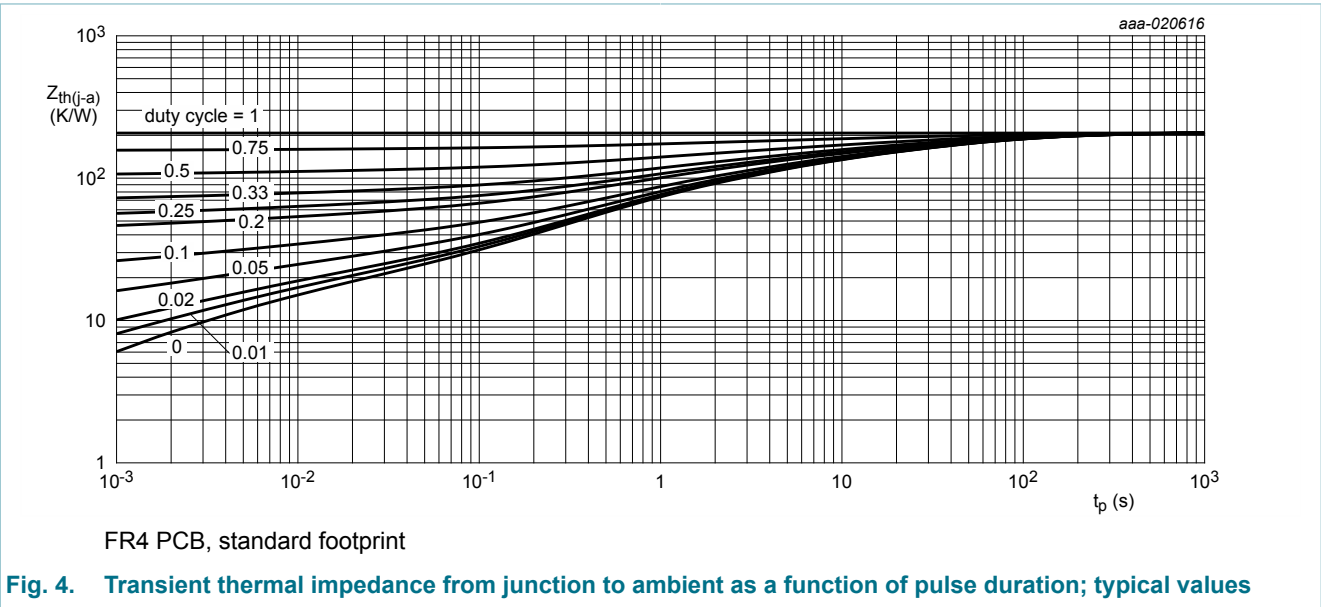


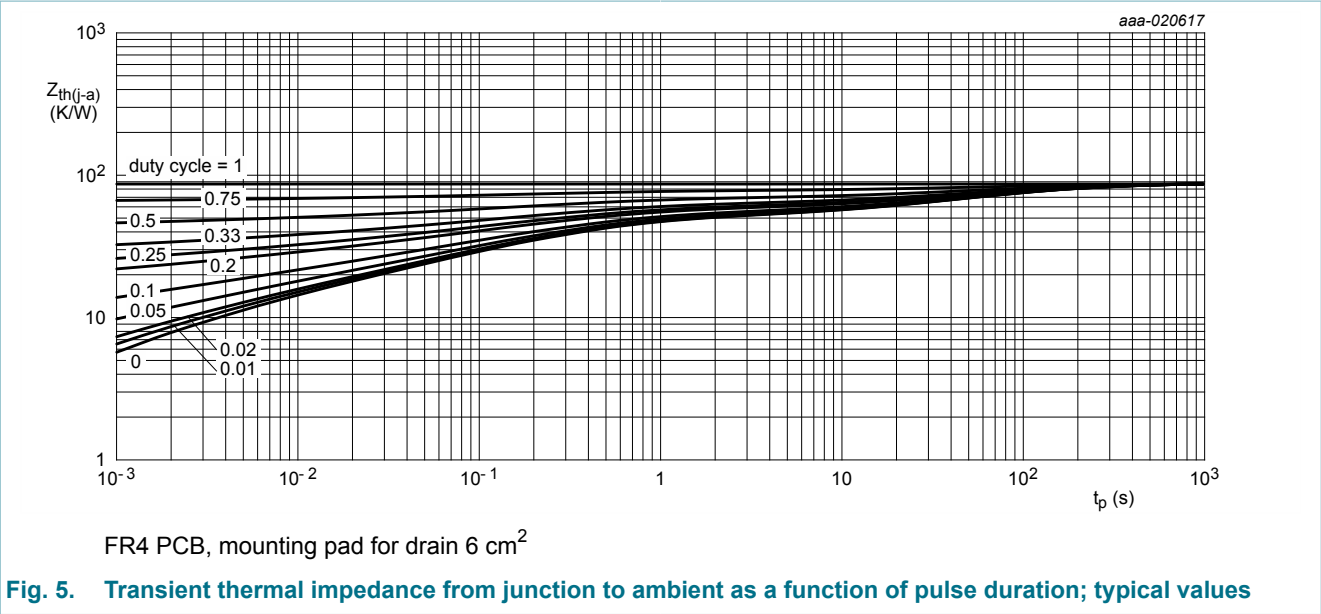
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	205	235	K/W
			[2]	-	88	101	K/W
		in free air; $t \leq 5$ s	[2]	-	55	63	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	24	28	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².





10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		30	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = 250 μA; V _{DS} =V _{GS} ; T _j = 25 °C		1	1.4	2	V
I _{DSS}	drain leakage current	V _{DS} = 30 V; V _{GS} = 0 V; T _j = 25 °C		-	-	1	μA
I _{GSS}	gate leakage current	V _{GS} = 16 V; V _{DS} = 0 V; T _j = 25 °C		-	-	10	μA
		V _{GS} = -16 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-10	μA
		V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	1	μA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-1	μA
		V _{GS} = 4.5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	200	nA
		V _{GS} = -4.5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-200	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 4.5 A; T _j = 25 °C		-	30	38	mΩ
		V _{GS} = 10 V; I _D = 4.5 A; T _j = 150 °C		-	47	60	mΩ
		V _{GS} = 4.5 V; I _D = 3.3 A; T _j = 25 °C		-	44	70	mΩ
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 2 A; T _j = 25 °C		-	10.7	-	S
R _G	gate resistance	T _j = 25 °C; f = 1 MHz		-	0.5	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = 15 V; I _D = 3.2 A; V _{GS} = 10 V; T _j = 25 °C		-	5.6	11	nC
Q _{GS}	gate-source charge			-	0.76	-	nC
Q _{GD}	gate-drain charge			-	1.1	-	nC
C _{iss}	input capacitance	V _{DS} = 15 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	294	-	pF
C _{oss}	output capacitance			-	42	-	pF
C _{rss}	reverse transfer capacitance			-	33	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 15 V; I _D = 3.2 A; V _{GS} = 10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	4.6	-	ns
t _r	rise time			-	14.7	-	ns
t _{d(off)}	turn-off delay time			-	9.1	-	ns
t _f	fall time			-	3	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 1.2 A; V _{GS} = 0 V; T _j = 25 °C		-	0.8	1.2	V

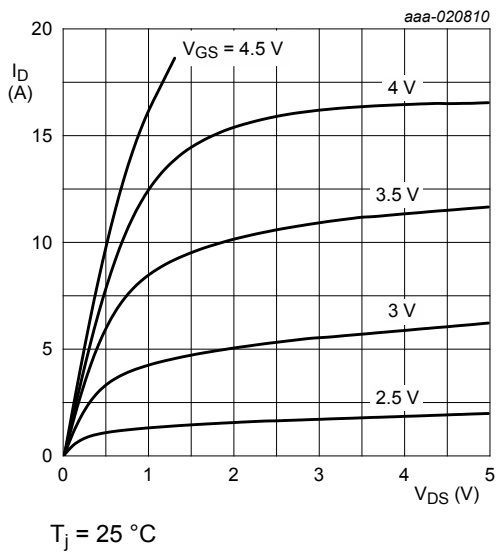


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

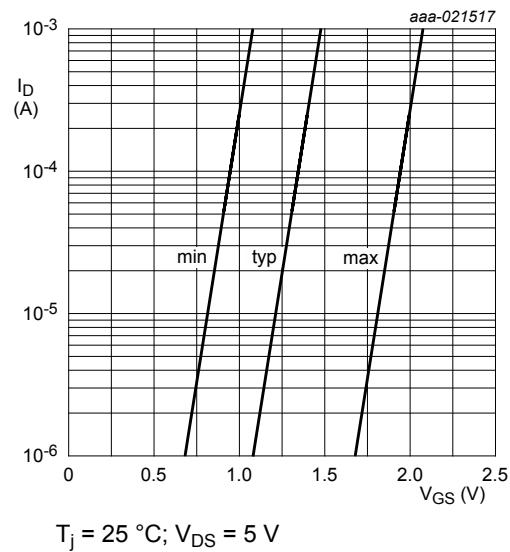


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

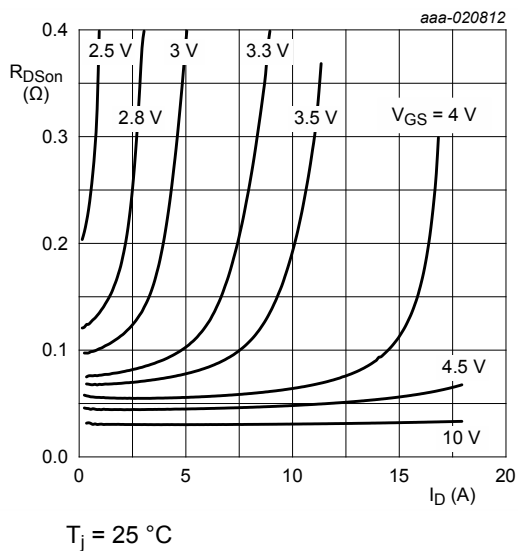


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

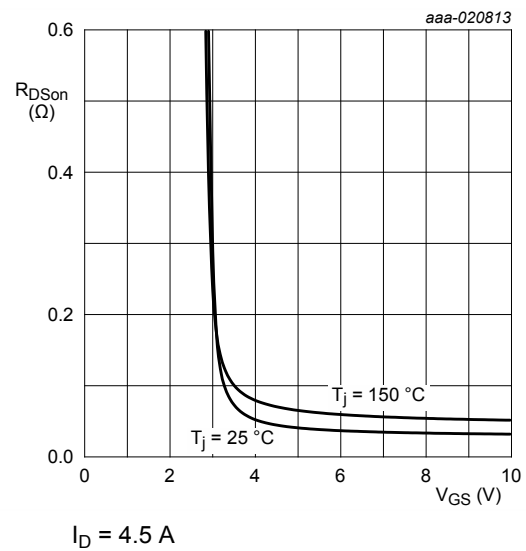


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

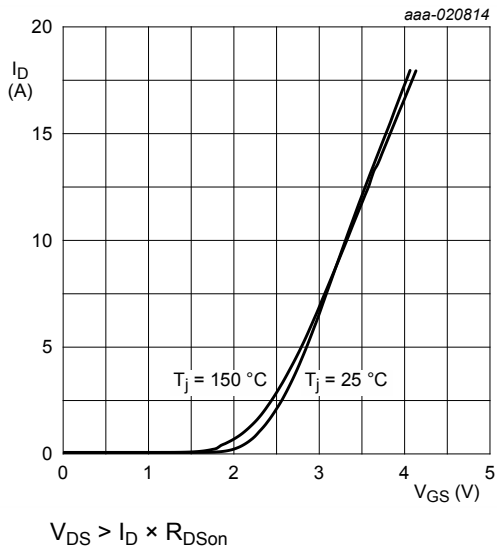


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

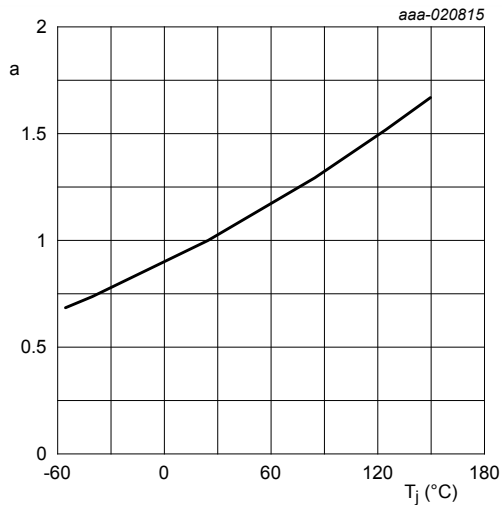


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

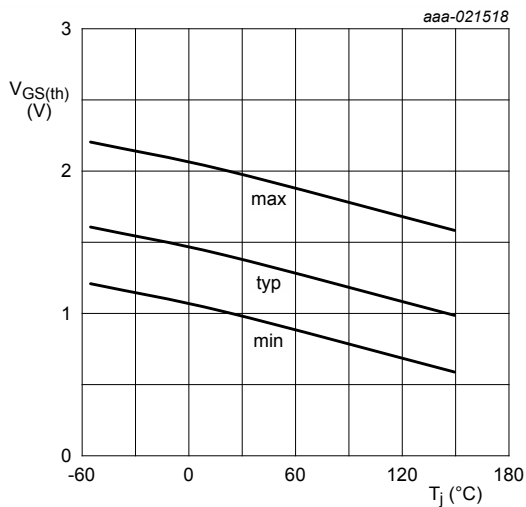


Fig. 12. Gate-source threshold voltage as a function of junction temperature

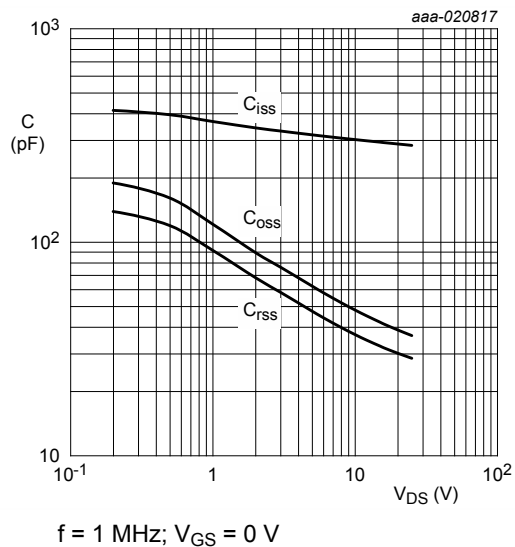


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

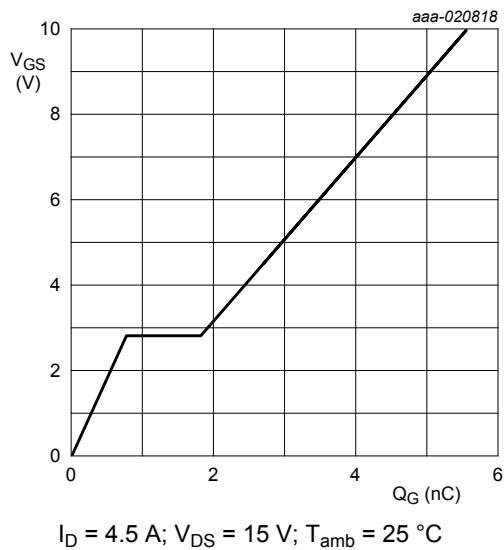


Fig. 14. Gate-source voltage as a function of gate charge; typical values

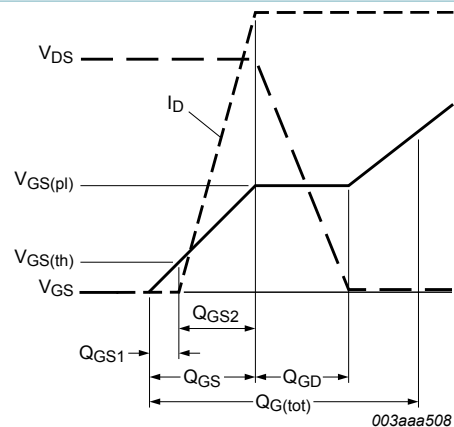


Fig. 15. MOSFET transistor: Gate charge waveform definitions

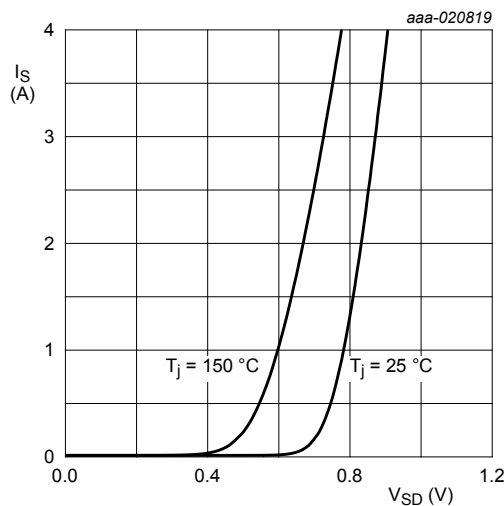


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

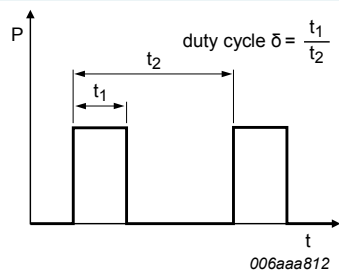
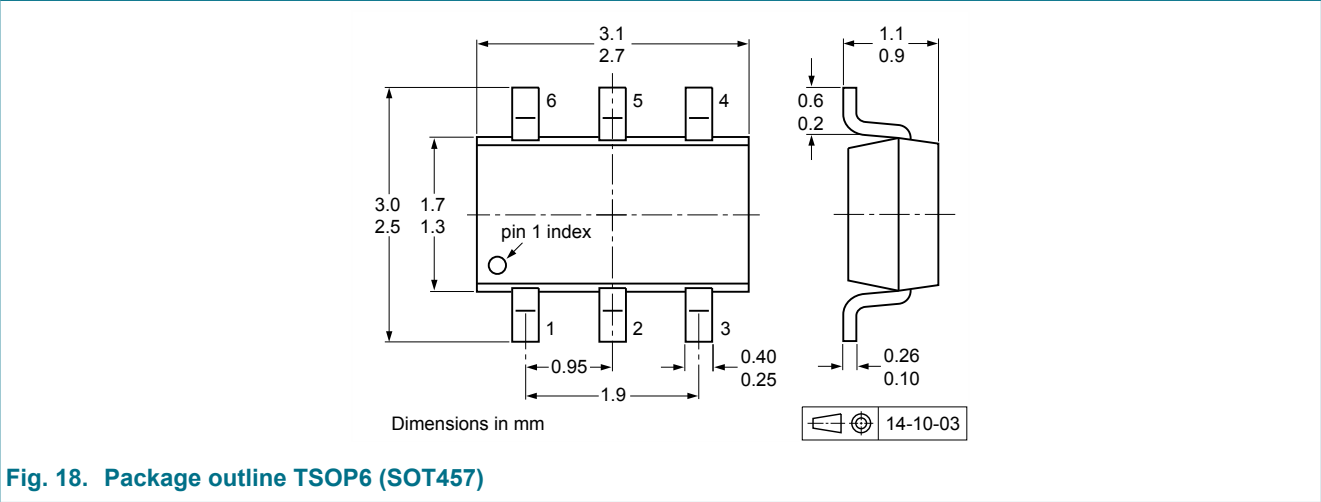
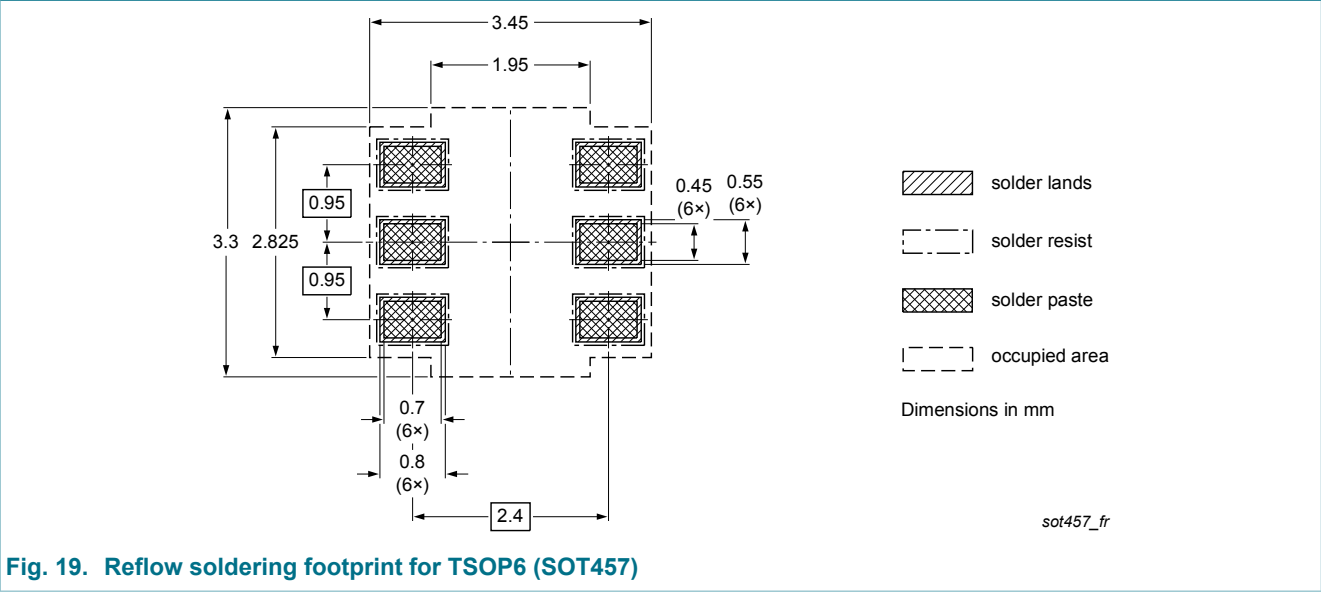


Fig. 17. Duty cycle definition

12. Package outline



13. Soldering



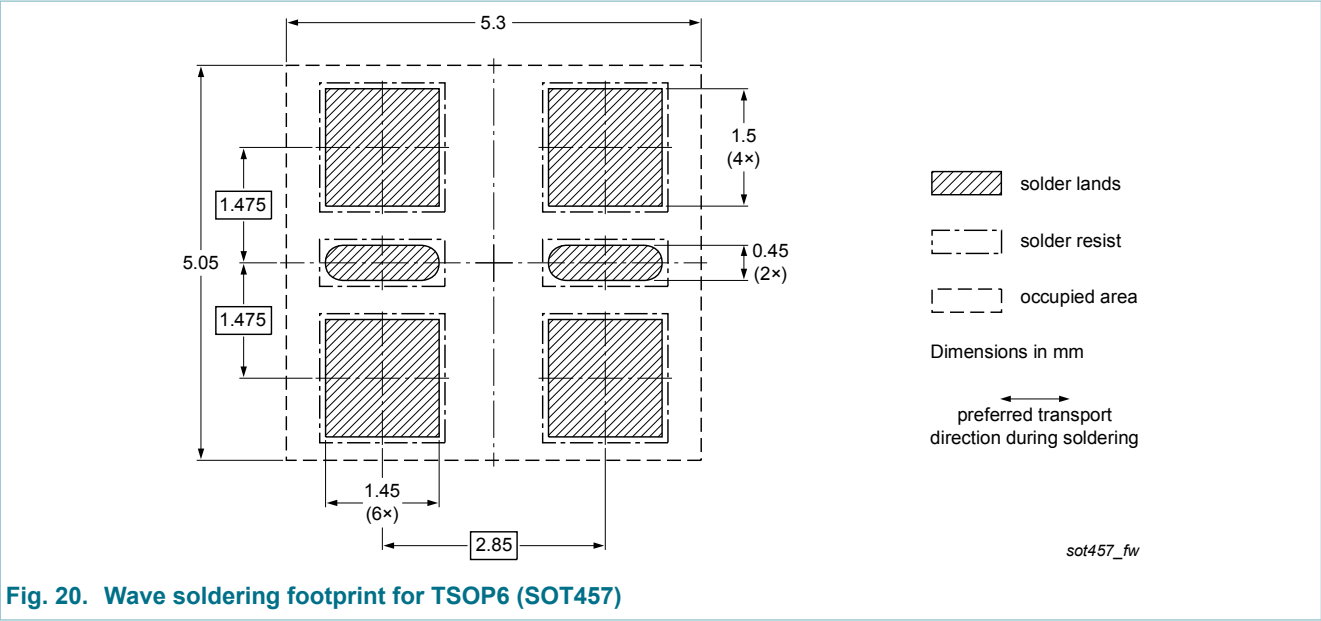


Fig. 20. Wave soldering footprint for TSOP6 (SOT457)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMN40ENE v.1	20160526	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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