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Kind regards,

Team Nexperia



# PMPB20EN

30 V N-channel Trench MOSFET

14 January 2014

Product data sheet

## 1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Trench MOSFET technology
- Very fast switching
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction
- Tin-plated 100 % solderable side pads for optical solder inspection

## 3. Applications

- Charging switch for portable devices
- DC-to-DC converters
- Power management in battery-driven portables
- Hard disk and computing power management

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$		-	-	30	V
$V_{GS}$	gate-source voltage			-20	-	20	V
$I_D$	drain current	$V_{GS} = 10 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}; t \leq 5 \text{ s}$	[1]	-	-	10.4	A
<b>Static characteristics</b>							
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 7 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$		-	16.5	19.5	$\text{m}\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6  $\text{cm}^2$ .



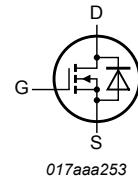
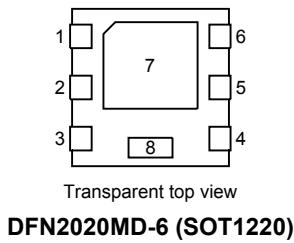
Scan or click this QR code to view the latest information for this product



## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain		
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		



## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMPB20EN	DFN2020MD-6	DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1220

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PMPB20EN	1B

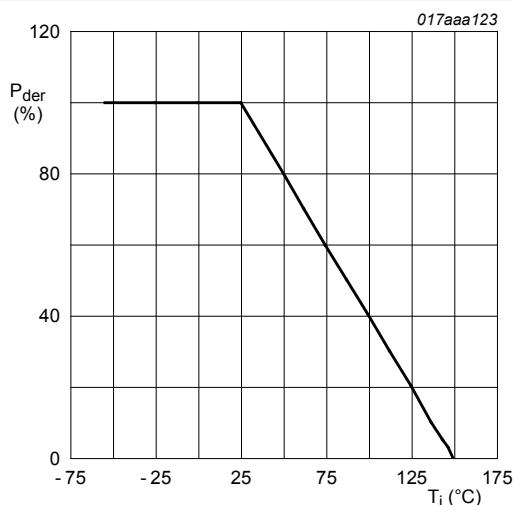
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

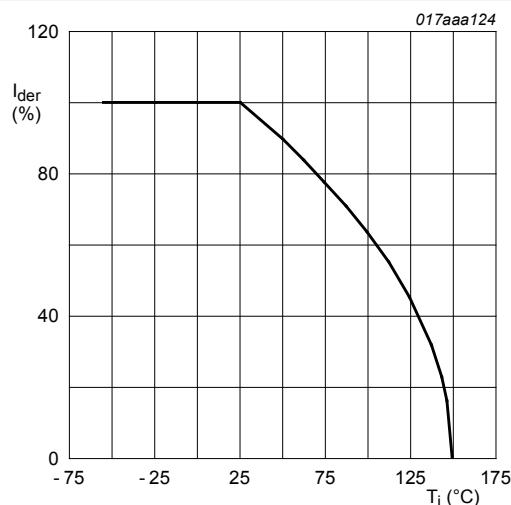
Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25^\circ\text{C}$		-	30	V
$V_{GS}$	gate-source voltage			-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25^\circ\text{C}; t \leq 5\text{ s}$	[1]	-	10.4	A
		$V_{GS} = 10\text{ V}; T_{amb} = 25^\circ\text{C}$	[1]	-	7.2	A
		$V_{GS} = 10\text{ V}; T_{amb} = 100^\circ\text{C}$	[1]	-	4.6	A
$I_{DM}$	peak drain current	$T_{amb} = 25^\circ\text{C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	30	A
$P_{tot}$	total power dissipation	$T_{amb} = 25^\circ\text{C}$	[1]	-	1.7	W
		$T_{amb} = 25^\circ\text{C}; t \leq 5\text{ s}$	[1]	-	3.5	W
		$T_{sp} = 25^\circ\text{C}$		-	12.5	W
$T_j$	junction temperature			-55	150	°C
$T_{amb}$	ambient temperature			-55	150	°C
$T_{stg}$	storage temperature			-65	150	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{amb} = 25^\circ\text{C}$	[1]	-	2.2	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain  $6\text{ cm}^2$ .



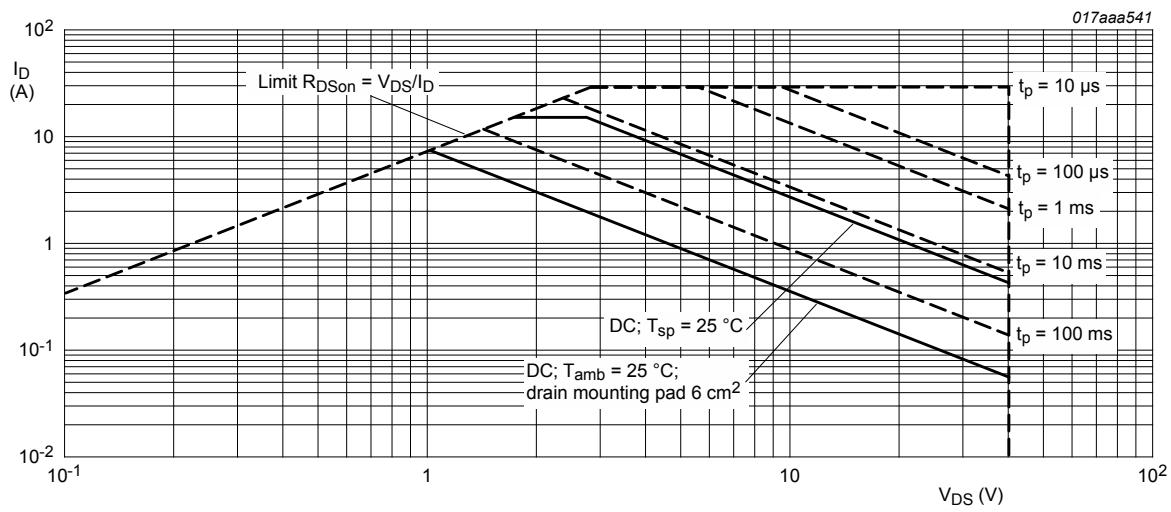
**Fig. 1. Normalized total power dissipation as a function of junction temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot}(25^\circ\text{C})} \times 100 \%$$



**Fig. 2. Normalized continuous drain current as a function of junction temperature**

$$I_{der} = \frac{I_D}{I_D(25^\circ\text{C})} \times 100 \%$$



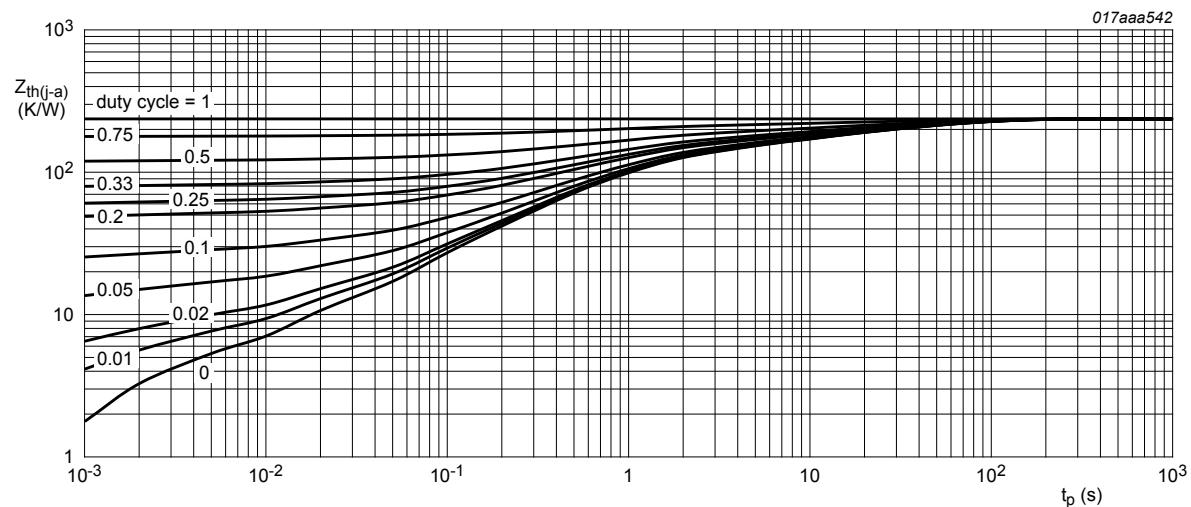
**Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage**

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

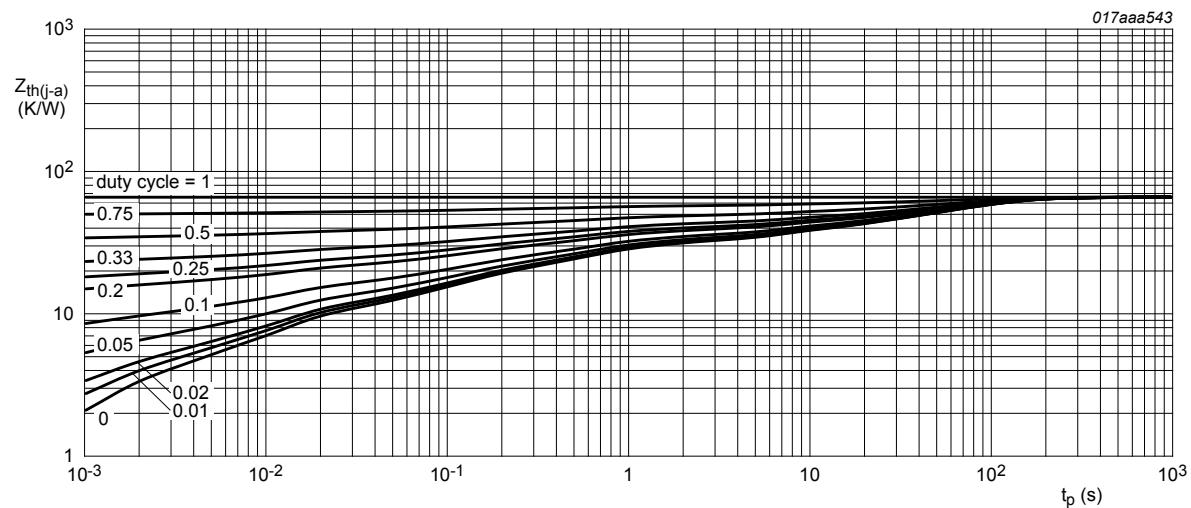
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	235	270	K/W
			[2]	-	67	74	K/W
			[3]	-	33	36	K/W
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point			-	5	10	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>, t ≤ 5 s



FR4 PCB, standard footprint

**Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



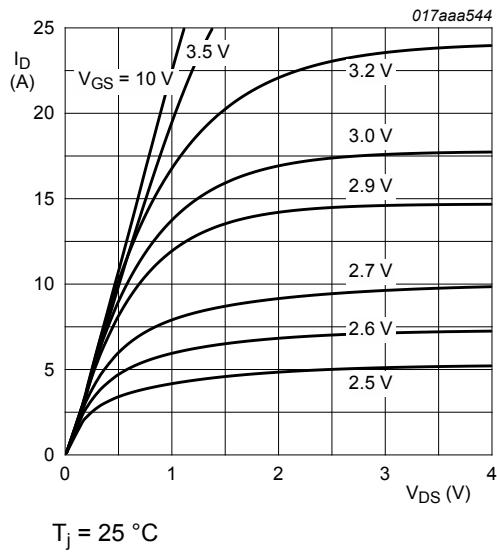
FR4 PCB, mounting pad for drain 6 cm<sup>2</sup>

**Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

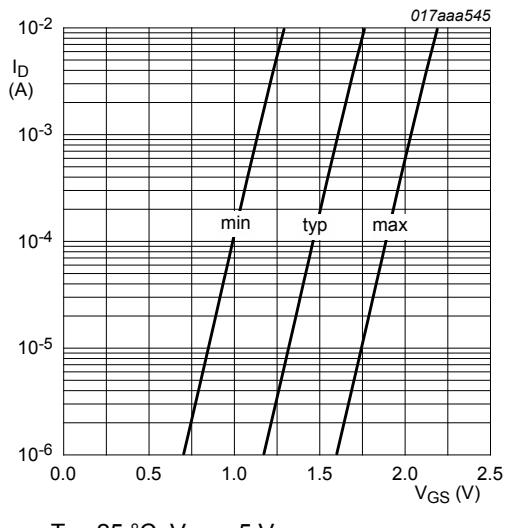
## 10. Characteristics

Table 7. Characteristics

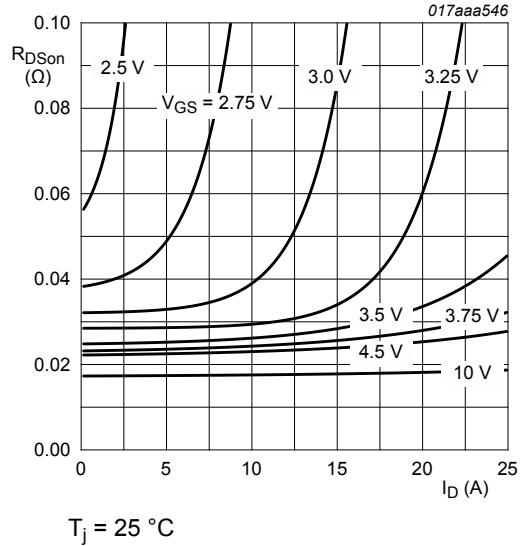
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Static characteristics</b>							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25^\circ C$		30	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu A$ ; $V_{DS} = V_{GS}$ ; $T_j = 25^\circ C$		1	1.5	2	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 V$ ; $V_{GS} = 0 V$ ; $T_j = 25^\circ C$		-	-	1	$\mu A$
		$V_{DS} = 30 V$ ; $V_{GS} = 0 V$ ; $T_j = 150^\circ C$		-	-	20	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 V$ ; $V_{DS} = 0 V$ ; $T_j = 25^\circ C$		-	-	100	nA
		$V_{GS} = -20 V$ ; $V_{DS} = 0 V$ ; $T_j = 25^\circ C$		-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 V$ ; $I_D = 7 A$ ; $T_j = 25^\circ C$		-	16.5	19.5	$m\Omega$
		$V_{GS} = 10 V$ ; $I_D = 7 A$ ; $T_j = 150^\circ C$		-	27	32	$m\Omega$
		$V_{GS} = 4.5 V$ ; $I_D = 7 A$ ; $T_j = 25^\circ C$		-	20.5	24.5	$m\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = 10 V$ ; $I_D = 7 A$ ; $T_j = 25^\circ C$		-	8	-	S
$R_G$	gate resistance	$f = 1 MHz$		-	1.7	-	$\Omega$
<b>Dynamic characteristics</b>							
$Q_{G(tot)}$	total gate charge	$V_{DS} = 15 V$ ; $I_D = 5 A$ ; $V_{GS} = 10 V$ ; $T_j = 25^\circ C$		-	7.2	10.8	nC
$Q_{GS}$	gate-source charge			-	1	-	nC
$Q_{GD}$	gate-drain charge			-	0.67	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 15 V$ ; $f = 1 MHz$ ; $V_{GS} = 0 V$ ; $T_j = 25^\circ C$		-	435	-	pF
$C_{oss}$	output capacitance			-	90	-	pF
$C_{rss}$	reverse transfer capacitance			-	35	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 V$ ; $I_D = 5 A$ ; $V_{GS} = 4.5 V$ ; $R_{G(ext)} = 1.7 \Omega$ ; $T_j = 25^\circ C$		-	9	-	ns
$t_r$	rise time			-	17	-	ns
$t_{d(off)}$	turn-off delay time			-	9	-	ns
$t_f$	fall time			-	8	-	ns
<b>Source-drain diode</b>							
$V_{SD}$	source-drain voltage	$I_S = 2.2 A$ ; $V_{GS} = 0 V$ ; $T_j = 25^\circ C$		-	0.8	1.2	V



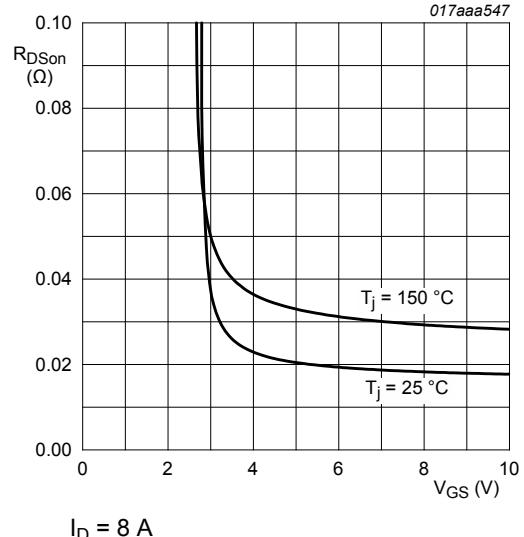
**Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



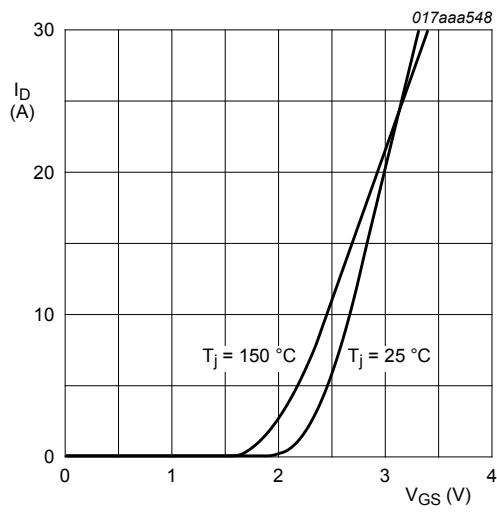
**Fig. 7. Sub-threshold drain current as a function of gate-source voltage**



**Fig. 8. Drain-source on-state resistance as a function of drain current; typical values**

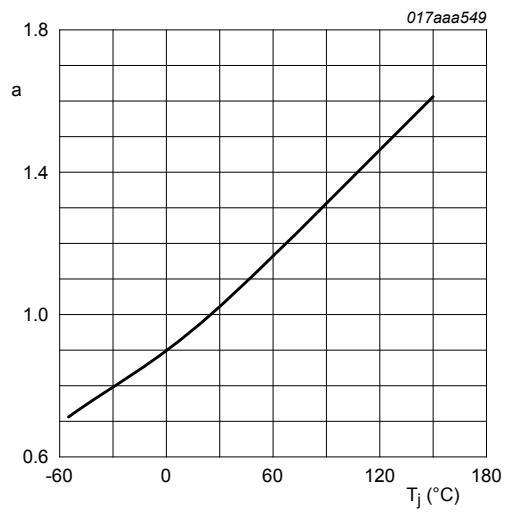


**Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**



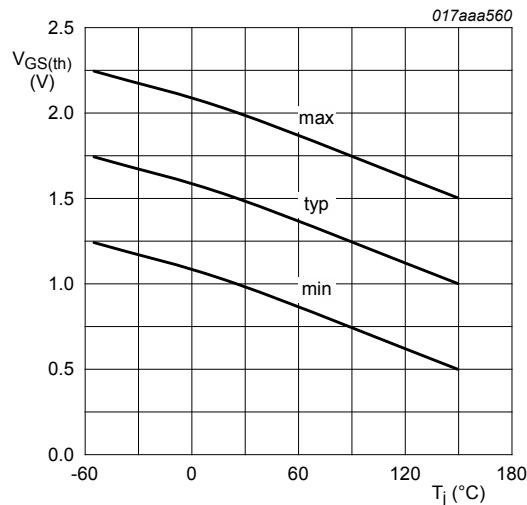
$V_{DS} > I_D \times R_{DSon}$

**Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



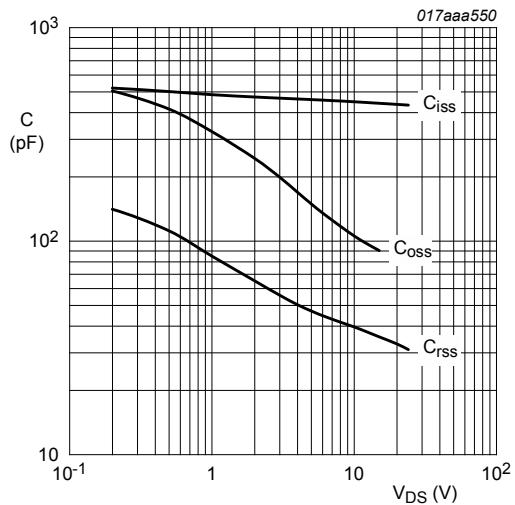
**Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values**

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$



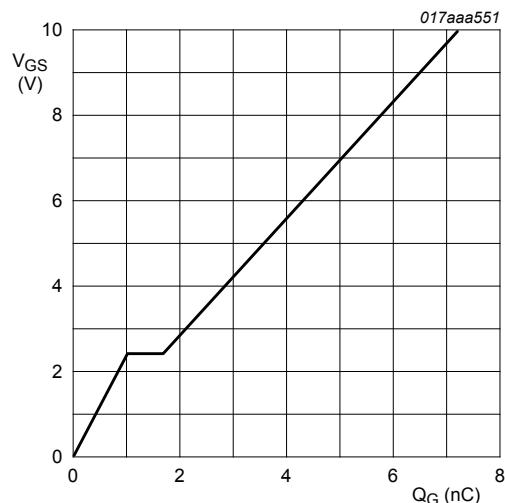
$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$

**Fig. 12. Gate-source threshold voltage as a function of junction temperature**



$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$

**Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$I_D = 5$  A;  $V_{DS} = 15$  V;  $T_{amb} = 25$  °C

Fig. 14. Gate-source voltage as a function of gate charge; typical values

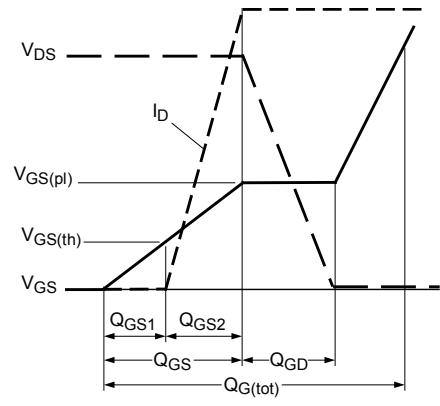
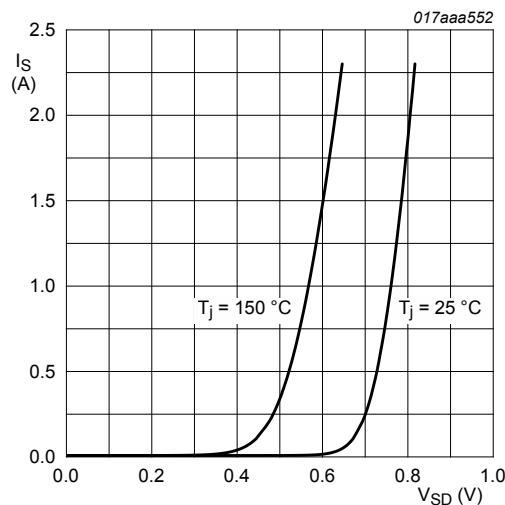


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0$  V

Fig. 16. Source current as a function of source-drain voltage; typical values

## 11. Test information

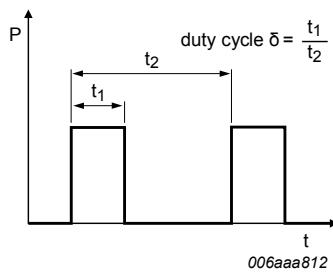


Fig. 17. Duty cycle definition

## 12. Package outline

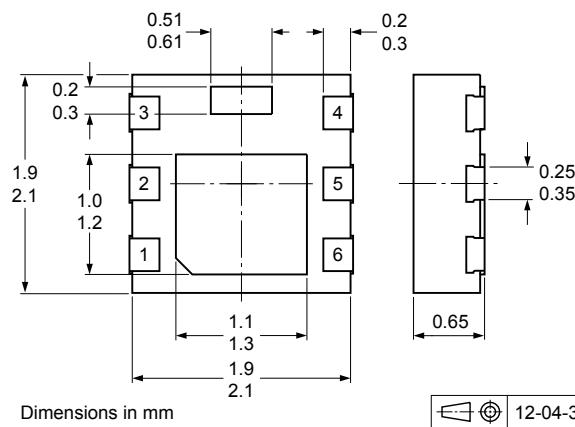
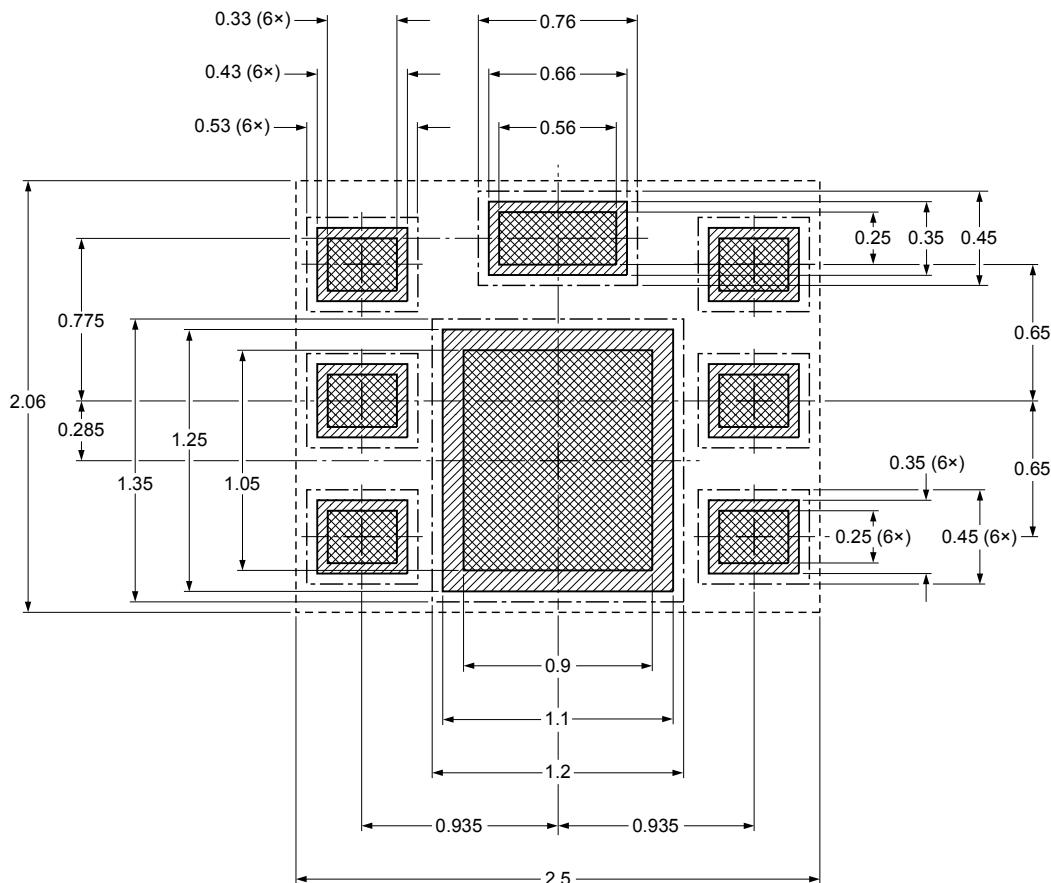


Fig. 18. Package outline DFN2020MD-6 (SOT1220)

## 13. Soldering

Footprint information for reflow soldering of DFN2020MD-6 package

SOT1220



solder land



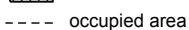
solder land plus solder paste



solder paste deposit



solder resist



--- occupied area

Dimensions in mm

sot1220\_fr

Fig. 19. Reflow soldering footprint for DFN2020MD-6 (SOT1220)

## 14. Revision history

**Table 8. Revision history**

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB20EN v.2	20140114	Product data sheet	-	PMPB20EN v.1
Modifications:	<ul style="list-style-type: none"><li>Table 7: parameter value of <math>V_{DS}</math> corrected from 10 V to 15 V in capacitance condition.</li><li>Figure 16: <math>V_{SD}</math> parameter corrected.</li></ul>			
PMPB20EN v.1	20120516	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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