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PMPB95ENEA

80 V, single N-channel Trench MOSFET

17 December 2013

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction
- Tin-plated 100 % solderable side pads for optical solder inspection
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_J = 25\text{ }^{\circ}\text{C}$		-	-	80	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t \leq 5\text{ s}$	[1]	-	-	4.1	A
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 2.8\text{ A}$; $T_J = 25\text{ }^{\circ}\text{C}$		-	80	105	m Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

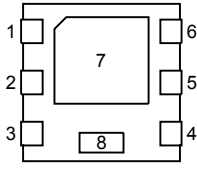
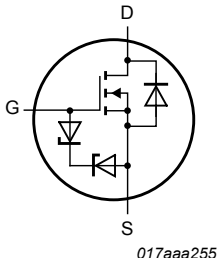


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>Transparent top view DFN2020MD-6 (SOT1220)</p>	
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMPB95ENEA	DFN2020MD-6	DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1220

7. Marking

Table 4. Marking codes

Type number	Marking code
PMPB95ENEA	2A

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	80	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}; t \leq 5\text{ s}$	[1]	-	4.1	A
		$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	2.8	A
		$V_{GS} = 10\text{ V}; T_{amb} = 100\text{ }^{\circ}\text{C}$	[1]	-	1.8	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ }^{\circ}\text{C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	11.2	A

Symbol	Parameter	Conditions		Min	Max	Unit
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $I_D = 0.46\text{ A}$; DUT in avalanche (unclamped)		-	19.3	mJ
P_{tot}	total power dissipation	$T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$	[1]	-	1.6	W
		$T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; $t \leq 5\text{ s}$	[1]	-	3.3	W
		$T_{\text{sp}} = 25\text{ }^{\circ}\text{C}$		-	15.6	W
T_j	junction temperature			-55	150	$^{\circ}\text{C}$
T_{amb}	ambient temperature			-55	150	$^{\circ}\text{C}$
T_{stg}	storage temperature			-65	150	$^{\circ}\text{C}$
Source-drain diode						
I_S	source current	$T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$	[1]	-	1.2	A
ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[2]	-	2000	V

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .

[2] Measured between all pins.

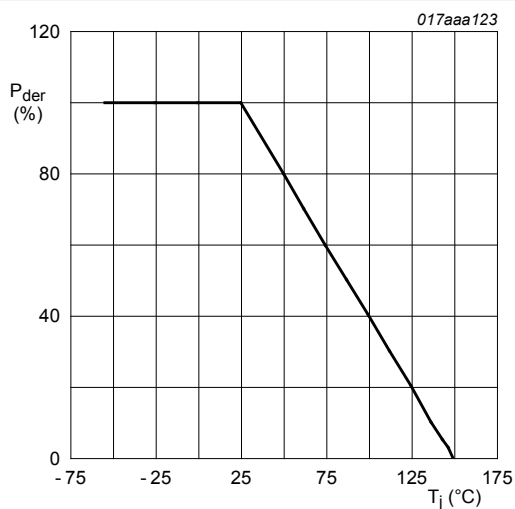


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{\text{der}} = \frac{P_{\text{tot}}}{P_{\text{tot}(25^{\circ}\text{C})}} \times 100\%$$

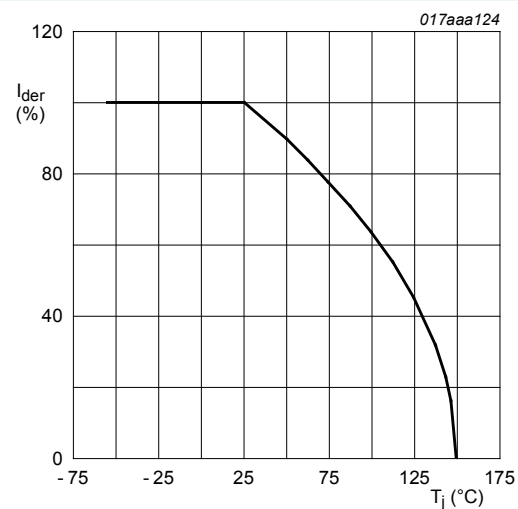
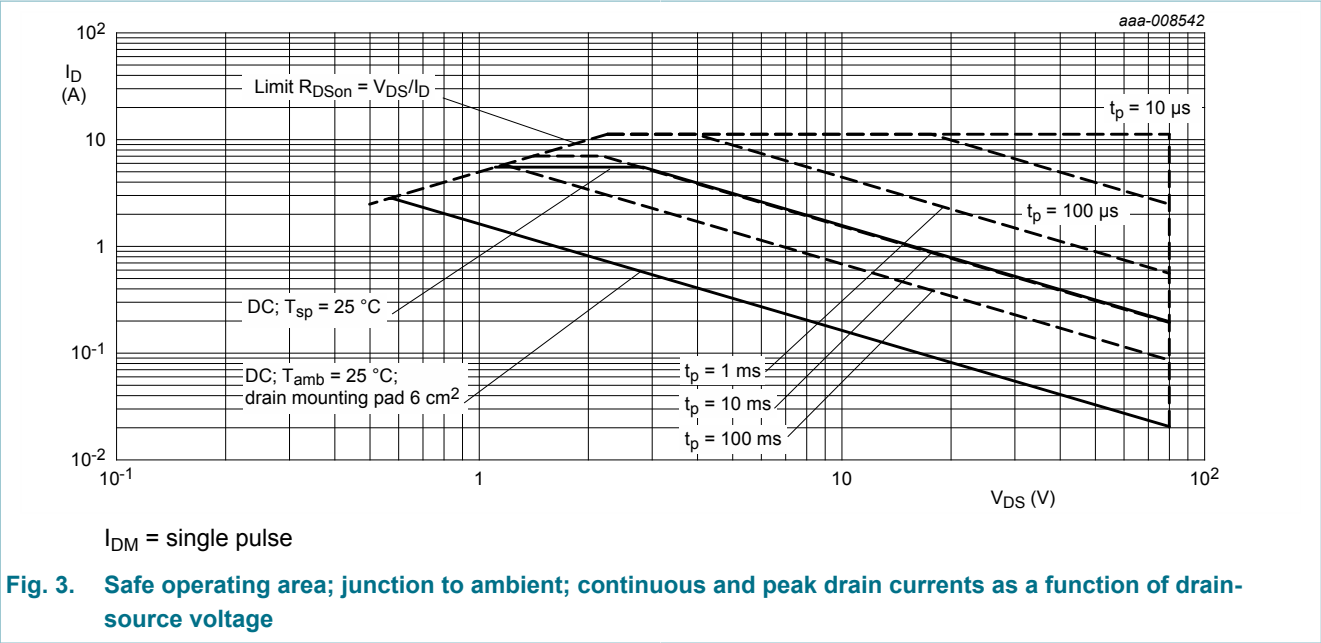


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{\text{der}} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

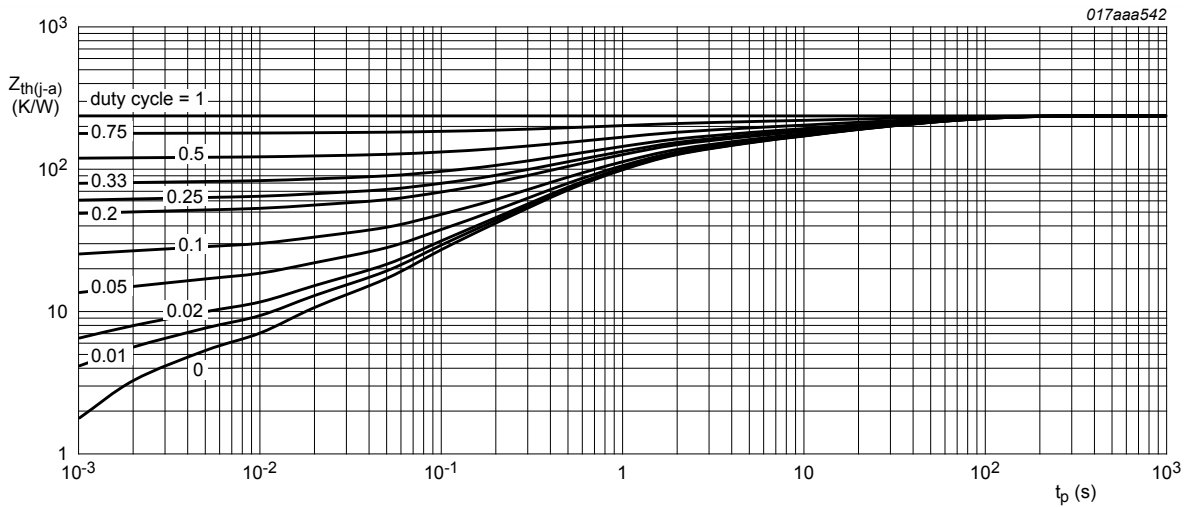


9. Thermal characteristics

Table 6. Thermal characteristics

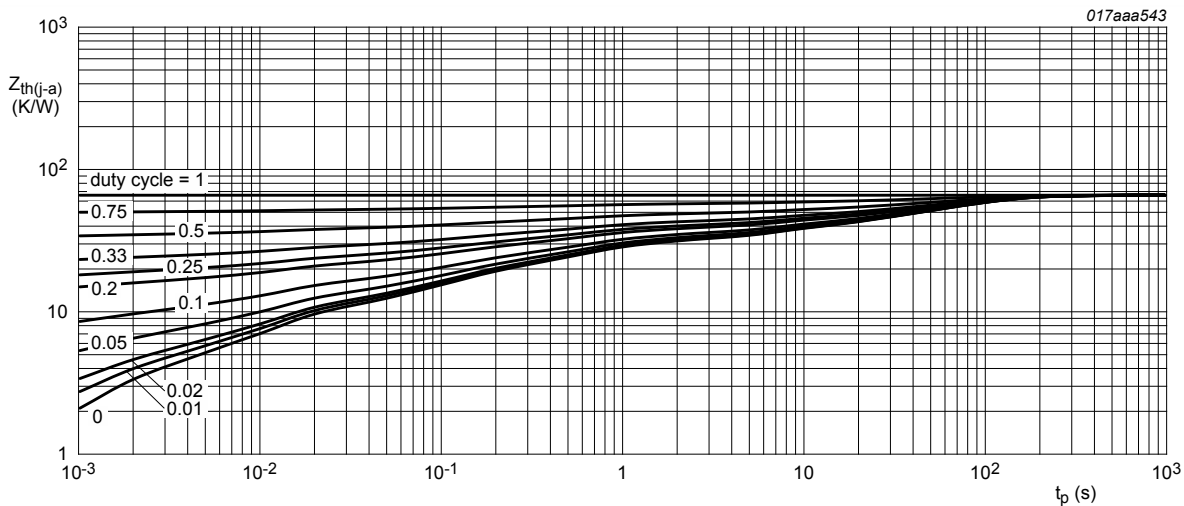
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	239	275	K/W
			[2]	-	67	77	K/W
		in free air; $t \leq 5\ s$	[2]	-	33	38	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	4	8	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain $6\ cm^2$.



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm²

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		80	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = 250 μA; V _{DS} = V _{GS} ; T _j = 25 °C		1.3	1.7	2.7	V
I _{DSS}	drain leakage current	V _{DS} = 80 V; V _{GS} = 0 V; T _j = 25 °C		-	-	1	μA
		V _{DS} = 80 V; V _{GS} = 0 V; T _j = 150 °C		-	-	10	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	10	μA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-10	μA
		V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	1	μA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-1	μA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 2.8 A; T _j = 25 °C		-	80	105	mΩ
		V _{GS} = 10 V; I _D = 2.8 A; T _j = 150 °C		-	154	202	mΩ
		V _{GS} = 4.5 V; I _D = 2.6 A; T _j = 25 °C		-	92	120	mΩ
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 2.8 A; T _j = 25 °C		-	13.3	-	S
R _G	gate resistance	f = 1 MHz		-	4.7	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = 40 V; I _D = 2.8 A; V _{GS} = 10 V; T _j = 25 °C		-	9.9	14.9	nC
Q _{GS}	gate-source charge			-	1.2	-	nC
Q _{GD}	gate-drain charge			-	1.8	-	nC
C _{iss}	input capacitance	V _{DS} = 40 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	504	-	pF
C _{oss}	output capacitance			-	43	-	pF
C _{rss}	reverse transfer capacitance			-	26	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 40 V; I _D = 2.8 A; V _{GS} = 10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	5	-	ns
t _r	rise time			-	4	-	ns
t _{d(off)}	turn-off delay time			-	15	-	ns
t _f	fall time			-	7	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 1.2 A; V _{GS} = 0 V; T _j = 25 °C		-	0.8	1.2	V

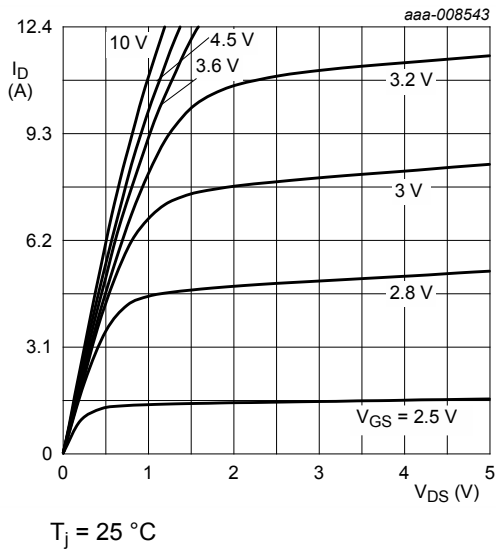


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

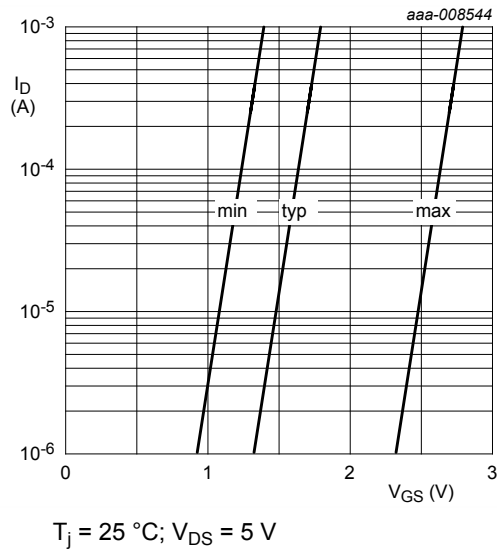


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

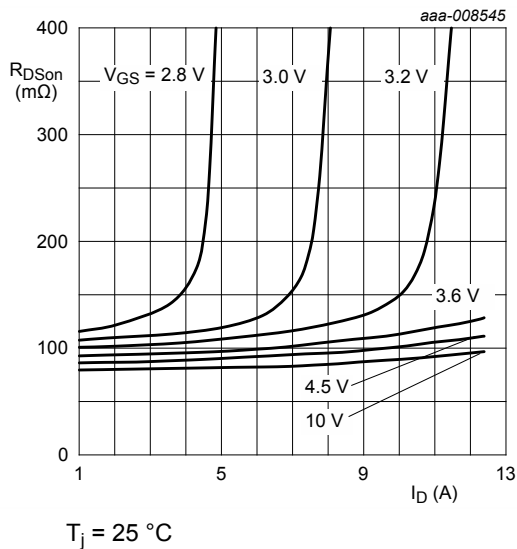


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

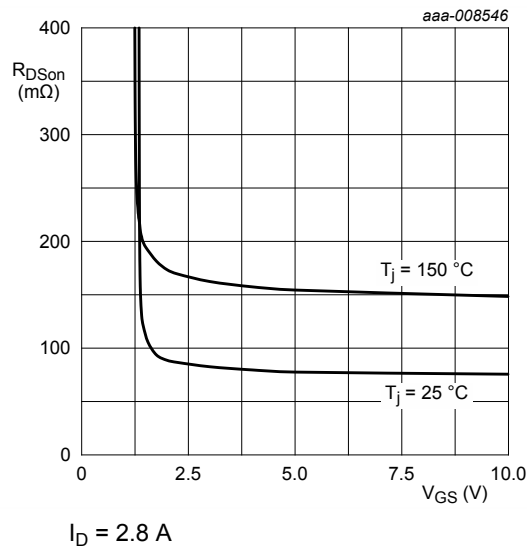


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

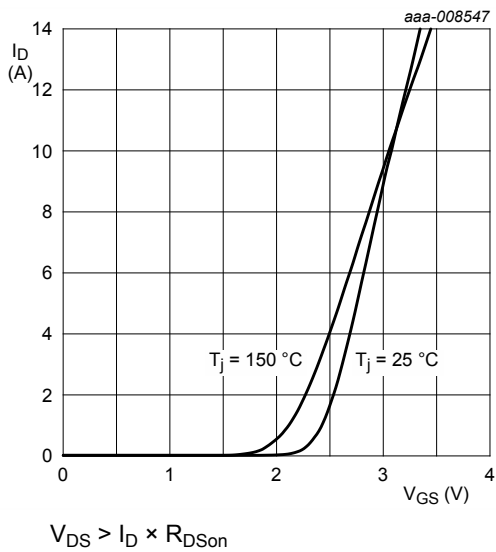


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

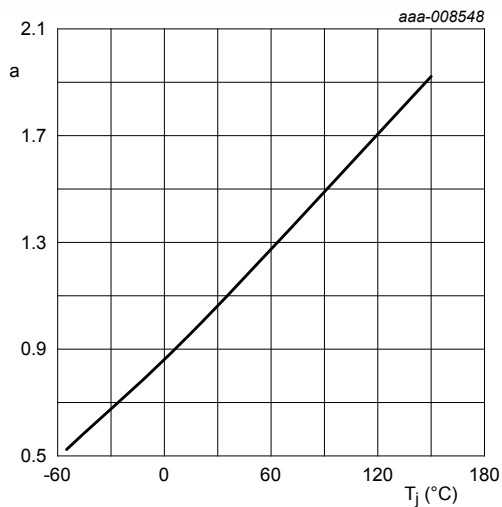


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

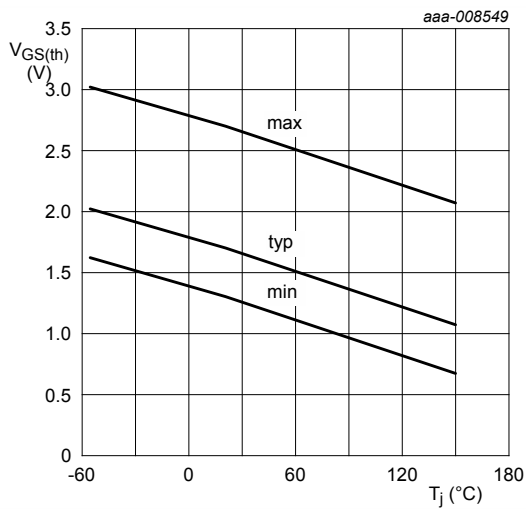


Fig. 12. Gate-source threshold voltage as a function of junction temperature

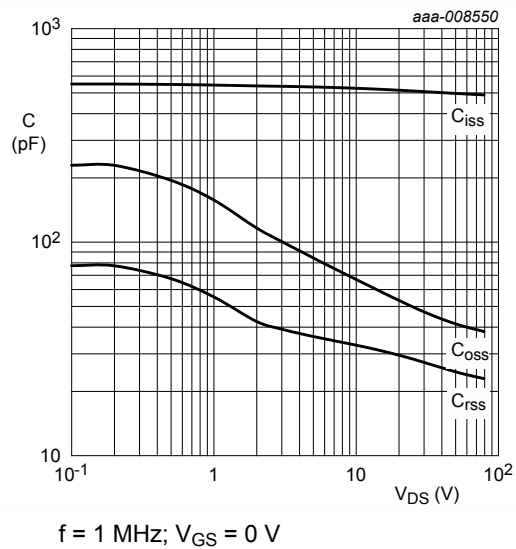


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

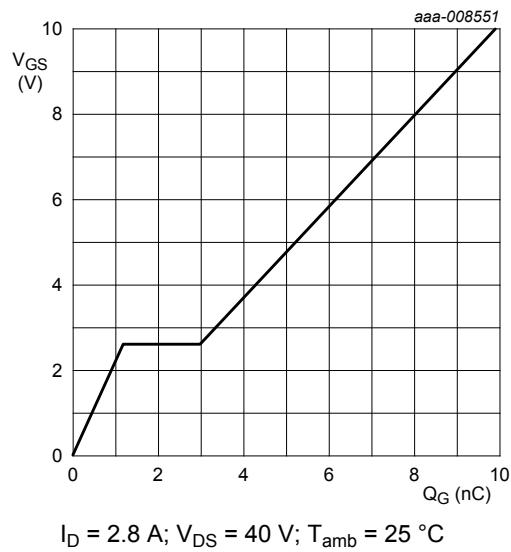


Fig. 14. Gate-source voltage as a function of gate charge; typical values

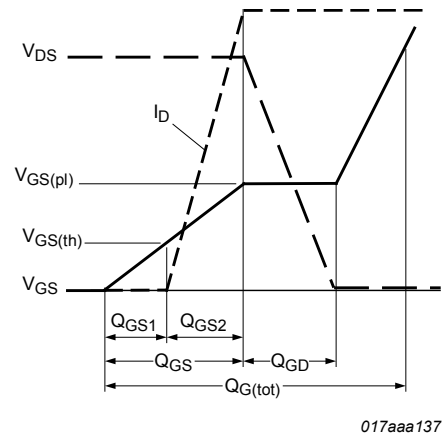
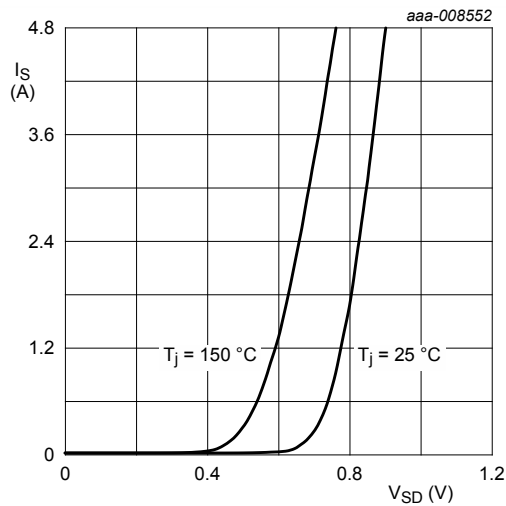


Fig. 15. MOSFET transistor: Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

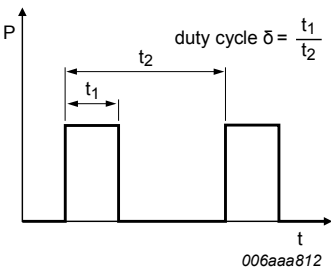


Fig. 17. Duty cycle definition

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline

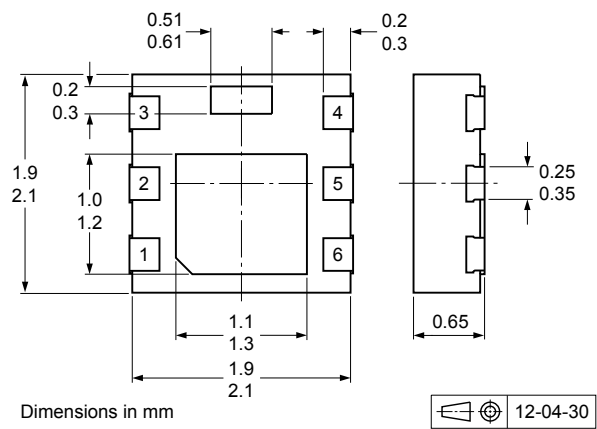
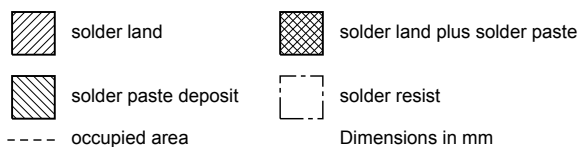
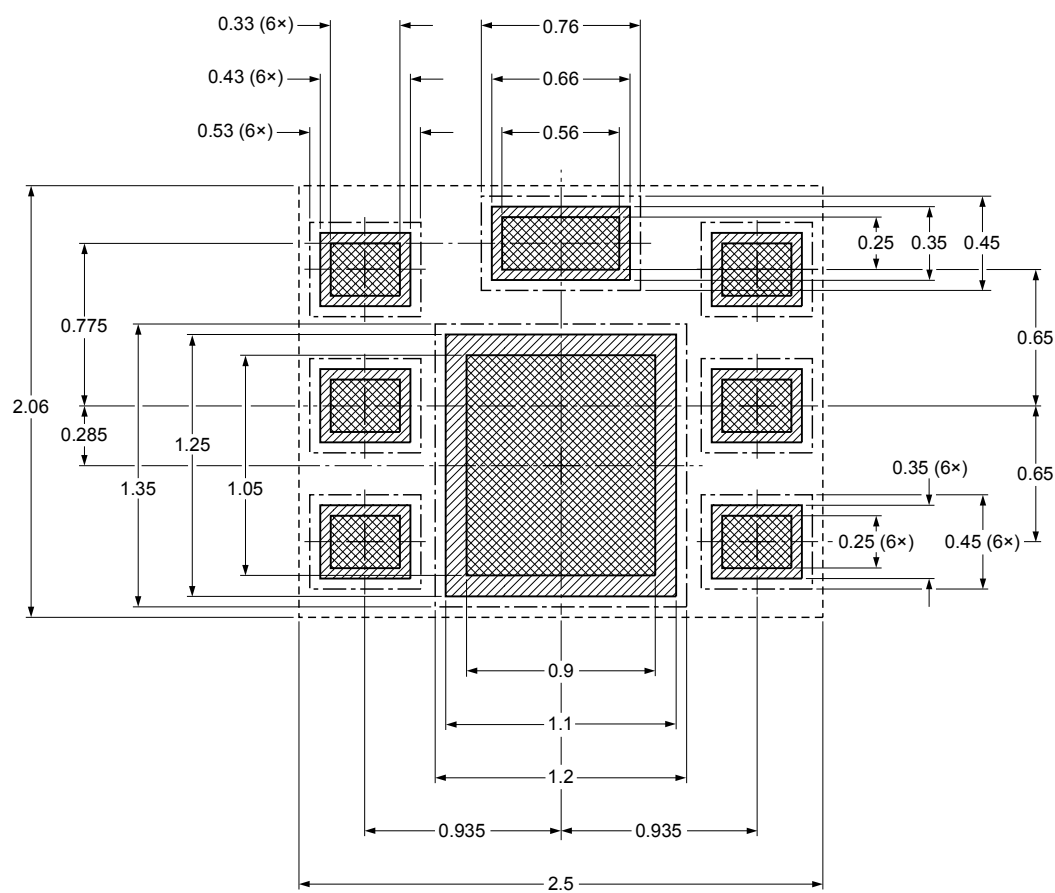


Fig. 18. Package outline DFN2020MD-6 (SOT1220)

13. Soldering

Footprint information for reflow soldering of DFN2020MD-6 package

SOT1220



sot1220_fr

Fig. 19. Reflow soldering footprint for DFN2020MD-6 (SOT1220)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB95ENEA v.2	20131217	Product data sheet	-	PMPB95ENEA v.1
Modifications:	<ul style="list-style-type: none">Product status changed			
PMPB95ENEA v.1	20130218	Objective data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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