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Kind regards,

Team Nexperia



# PMV30XPEA

20 V, P-channel Trench MOSFET

30 October 2015

Product data sheet

## 1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Trench MOSFET technology
- Very fast switching
- Enhanced power dissipation capability:  $P_{tot} = 980 \text{ mW}$
- ElectroStatic Discharge (ESD) protection  $> 2 \text{ kV HBM}$
- AEC-Q101 qualified

## 3. Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$	-	-	-20	V
$V_{GS}$	gate-source voltage		-12	-	12	V
$I_D$	drain current	$V_{GS} = -4.5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}; t \leq 5 \text{ s}$	[1]	-	-5.3	A
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -3 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	28	34	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain  $6 \text{ cm}^2$ .

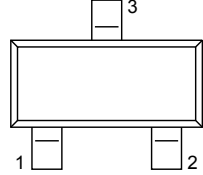
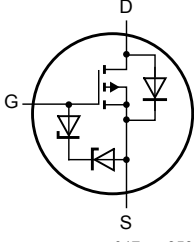


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## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>TO-236AB (SOT23)</p>	 <p>017aaa259</p>
2	S	source		
3	D	drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMV30XPEA	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PMV30XPEA	DM% [1]

[1] % = placeholder for manufacturing site code

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	-20	V
V <sub>GS</sub>	gate-source voltage			-12	12	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	-5.3	A
		V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 25 °C	[1]	-	-4.5	A
		V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 100 °C	[1]	-	-2.8	A
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs		-	-18	A
E <sub>DS(AL)R</sub>	repetitive drain-source avalanche energy	I <sub>D</sub> = -1.3 A; T <sub>j(initial)</sub> = 25 °C; DUT in avalanche (unclamped)		-	13	mJ
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	490	mW
			[1]	-	980	mW
		T <sub>sp</sub> = 25 °C		-	5435	mW
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	-0.89	A
<b>ESD maximum rating</b>						
V <sub>ESD</sub>	electrostatic discharge voltage	HBM	[3]	-	2000	V

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.

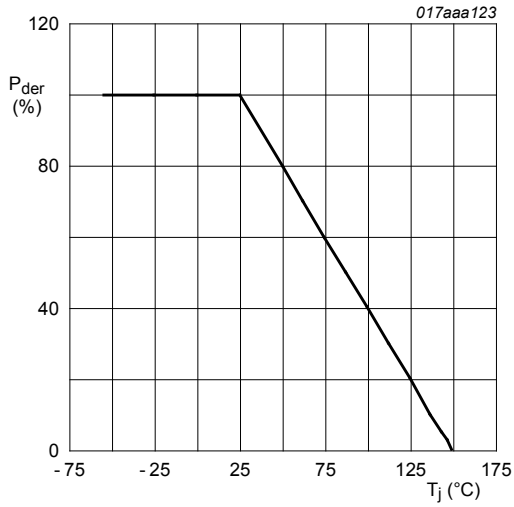


Fig. 1. MOSFET transistor: Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

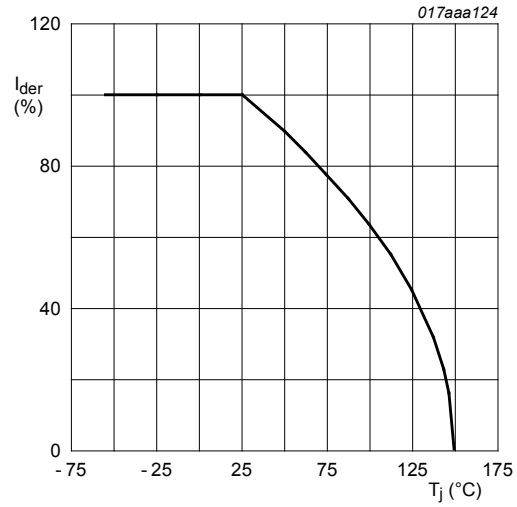
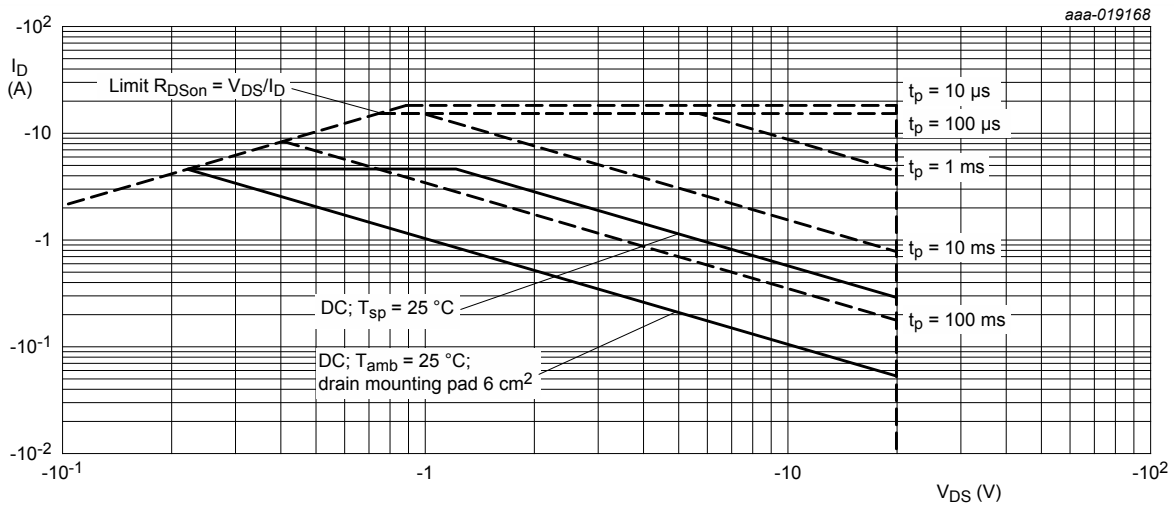


Fig. 2. MOSFET transistor: Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$



I<sub>DM</sub> = single pulse

Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	220	255	K/W
			[2]	110	130	K/W
		in free air; t ≤ 5 s	[2]	80	90	K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	20	25	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

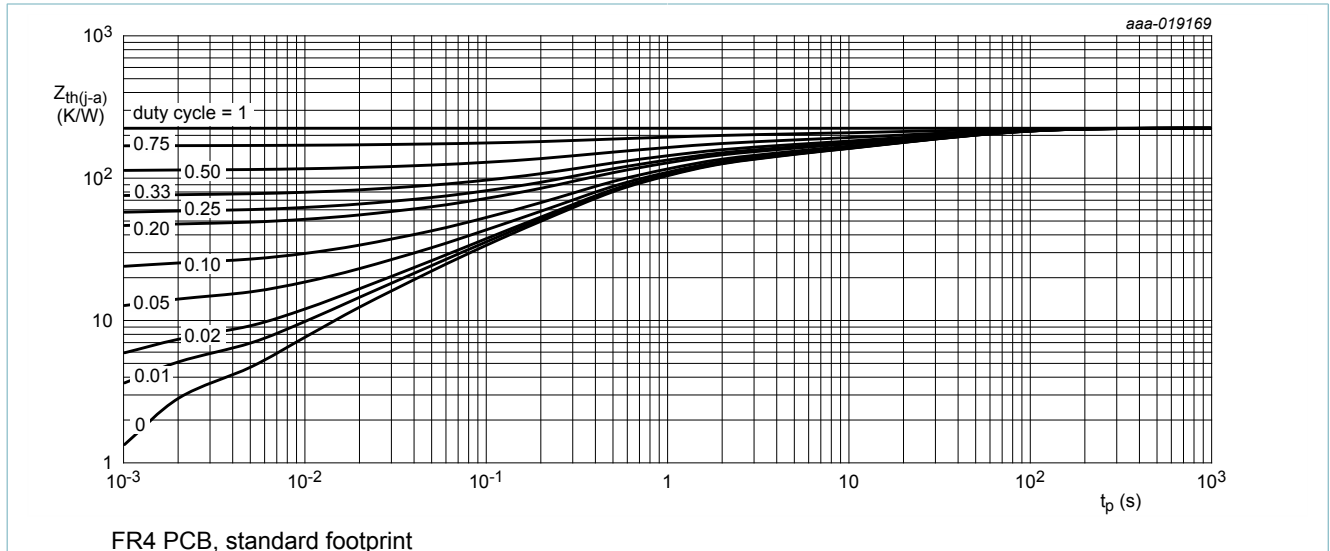


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

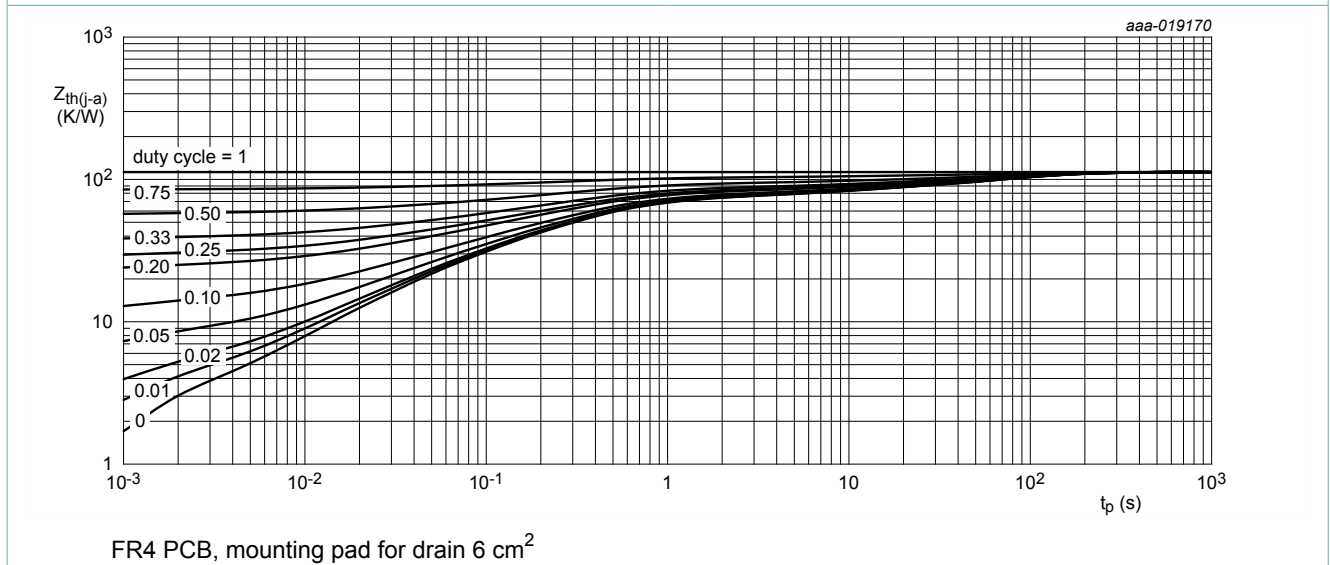


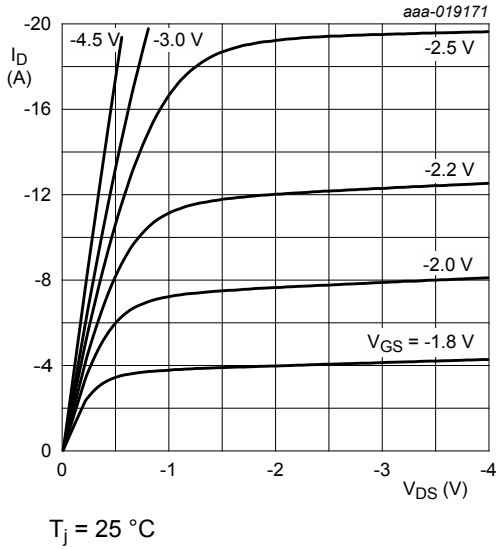
Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

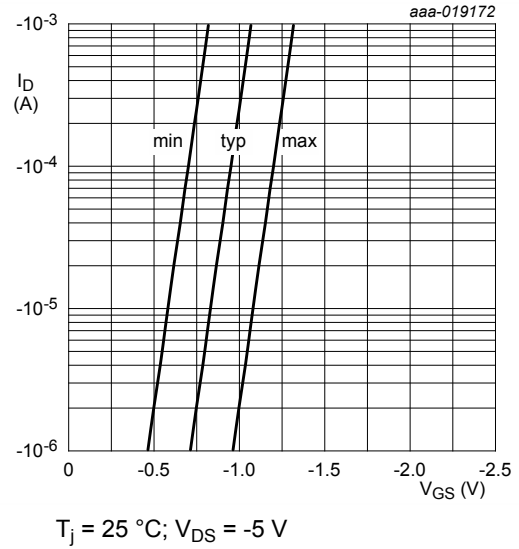
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	-0.75	-1	-1.25	V
$I_{DSS}$	drain leakage current	$V_{DS} = -20 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 12 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	10	$\mu A$
		$V_{GS} = -12 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-10	$\mu A$
		$V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	5	$\mu A$
		$V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-5	$\mu A$
		$V_{GS} = 2.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -2.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 V; I_D = -3 A; T_j = 25 \text{ }^\circ C$	-	28	34	m $\Omega$
		$V_{GS} = -4.5 V; I_D = -3 A; T_j = 150 \text{ }^\circ C$	-	42	49	m $\Omega$
		$V_{GS} = -2.5 V; I_D = -3 A; T_j = 25 \text{ }^\circ C$	-	42	57	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -10 V; I_D = -2 A; T_j = 25 \text{ }^\circ C$	-	13	-	S
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	10.4	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 V; I_D = -3 A; V_{GS} = -4.5 V; T_j = 25 \text{ }^\circ C$	-	11	17	nC
$Q_{GS}$	gate-source charge		-	3.2	-	nC
$Q_{GD}$	gate-drain charge		-	2	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -10 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	1465	-	pF
$C_{oss}$	output capacitance		-	193	-	pF
$C_{rss}$	reverse transfer capacitance		-	133	-	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = -10 V; I_D = -3 A; V_{GS} = -4.5 V; R_{G(ext)} = 6 \Omega; T_j = 25 \text{ }^\circ C$	-	7.9	-
$t_r$	rise time	-		42	-	ns
$t_{d(off)}$	turn-off delay time	-		59	-	ns
$t_f$	fall time	-		27.5	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = -0.89 A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-0.7	-1.2	V

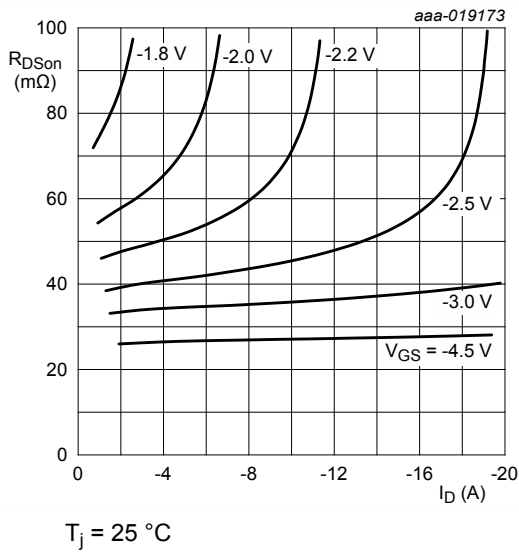




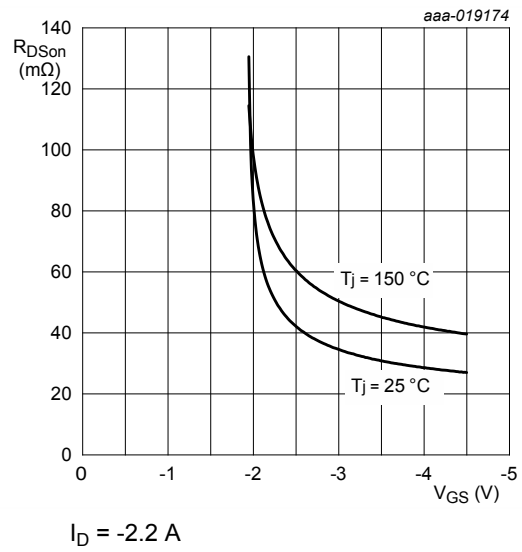
**Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



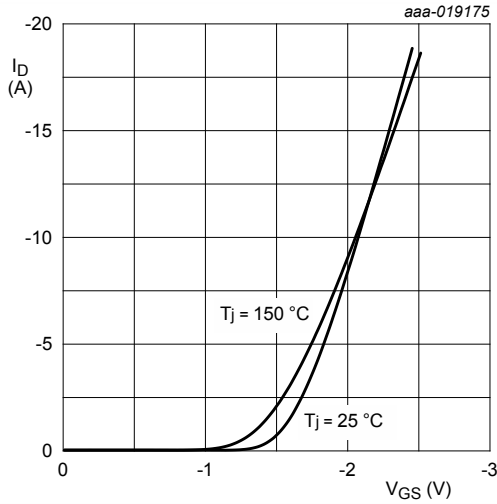
**Fig. 7. Sub-threshold drain current as a function of gate-source voltage**



**Fig. 8. Drain-source on-state resistance as a function of drain current; typical values**



**Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**



$$V_{DS} > I_D \times R_{DSon}$$

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

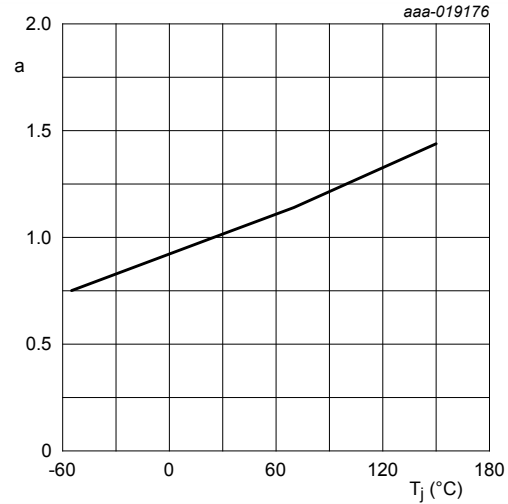
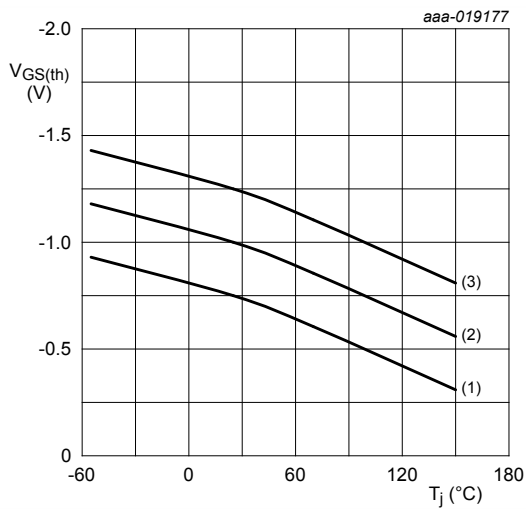


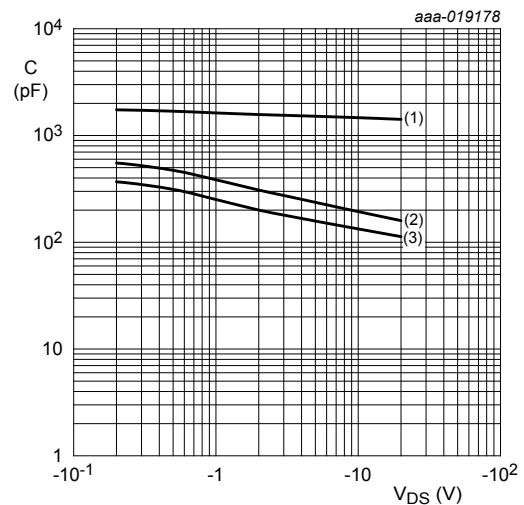
Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$



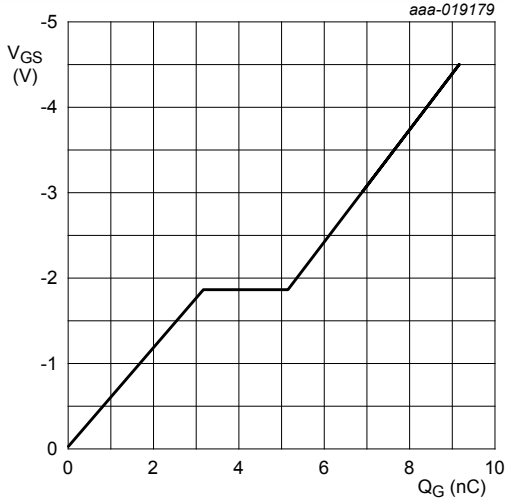
$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}$   
 (1) minimum values  
 (2) typical values  
 (3) maximum values

Fig. 12. Gate-source threshold voltage as a function of junction temperature



$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$   
 (1)  $C_{iss}$   
 (2)  $C_{oss}$   
 (3)  $C_{rss}$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = -3$  A;  $V_{DS} = -10$  V;  $T_{amb} = 25$  °C

Fig. 14. Gate-source voltage as a function of gate charge; typical values

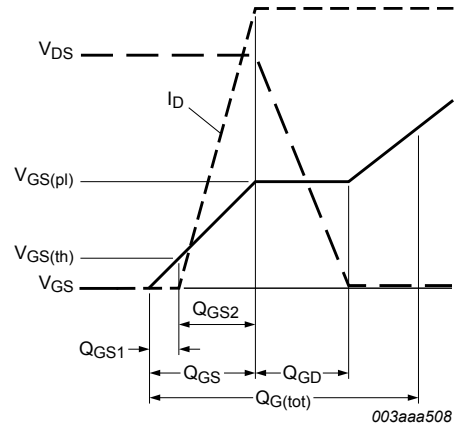
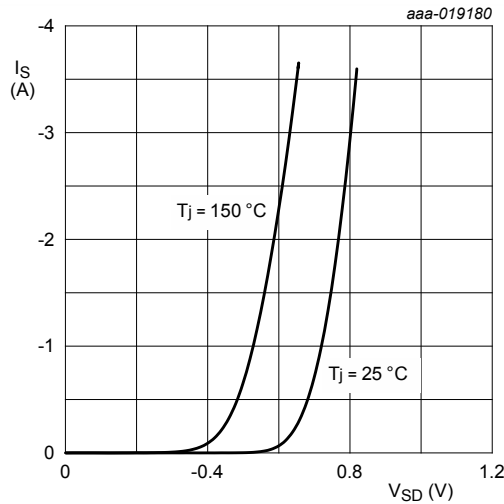


Fig. 15. MOSFET transistor: Gate charge waveform definitions



$V_{GS} = 0$  V

Fig. 16. Source current as a function of source-drain voltage; typical values

## 11. Test information

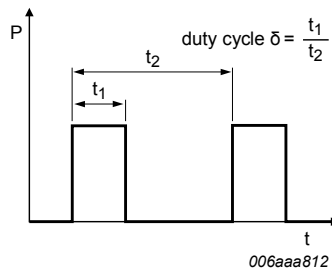


Fig. 17. Duty cycle definition

### 11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

## 12. Package outline

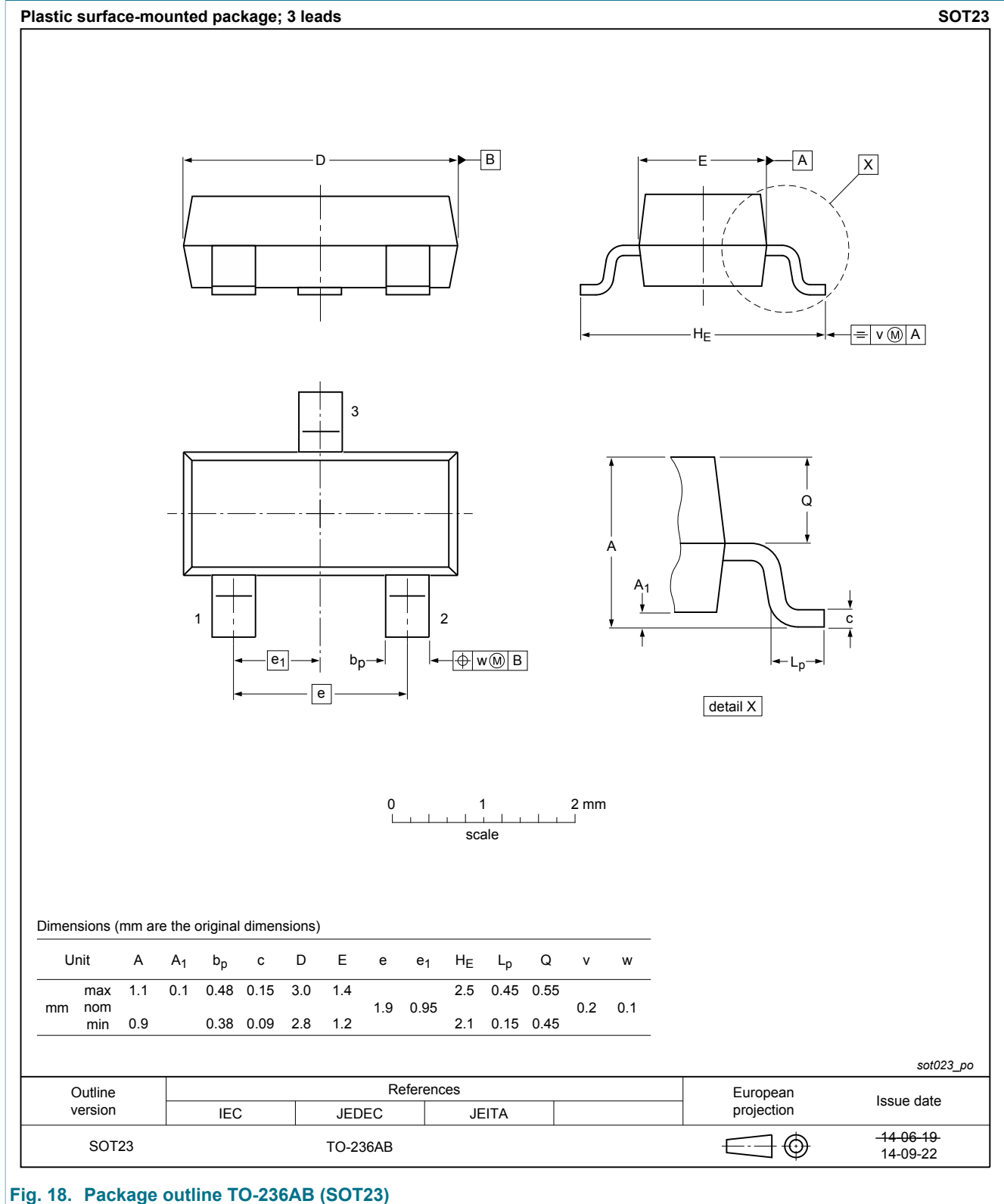


Fig. 18. Package outline TO-236AB (SOT23)

### 13. Soldering

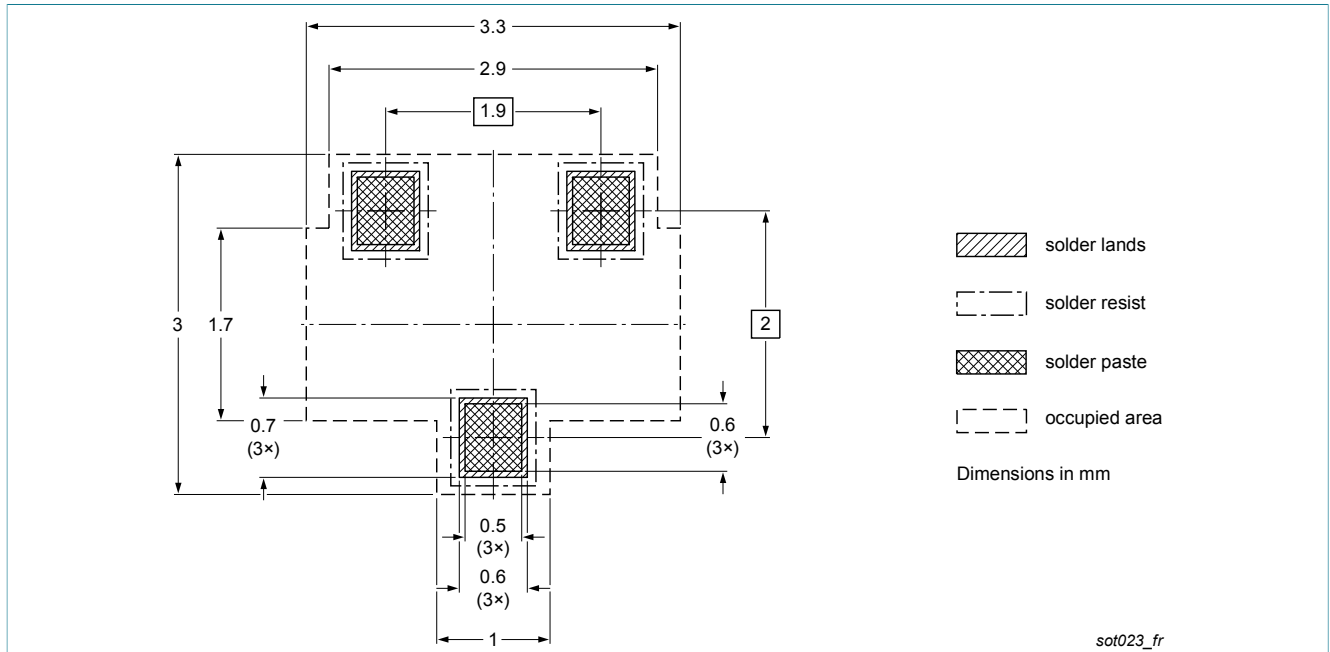


Fig. 19. Reflow soldering footprint for TO-236AB (SOT23)

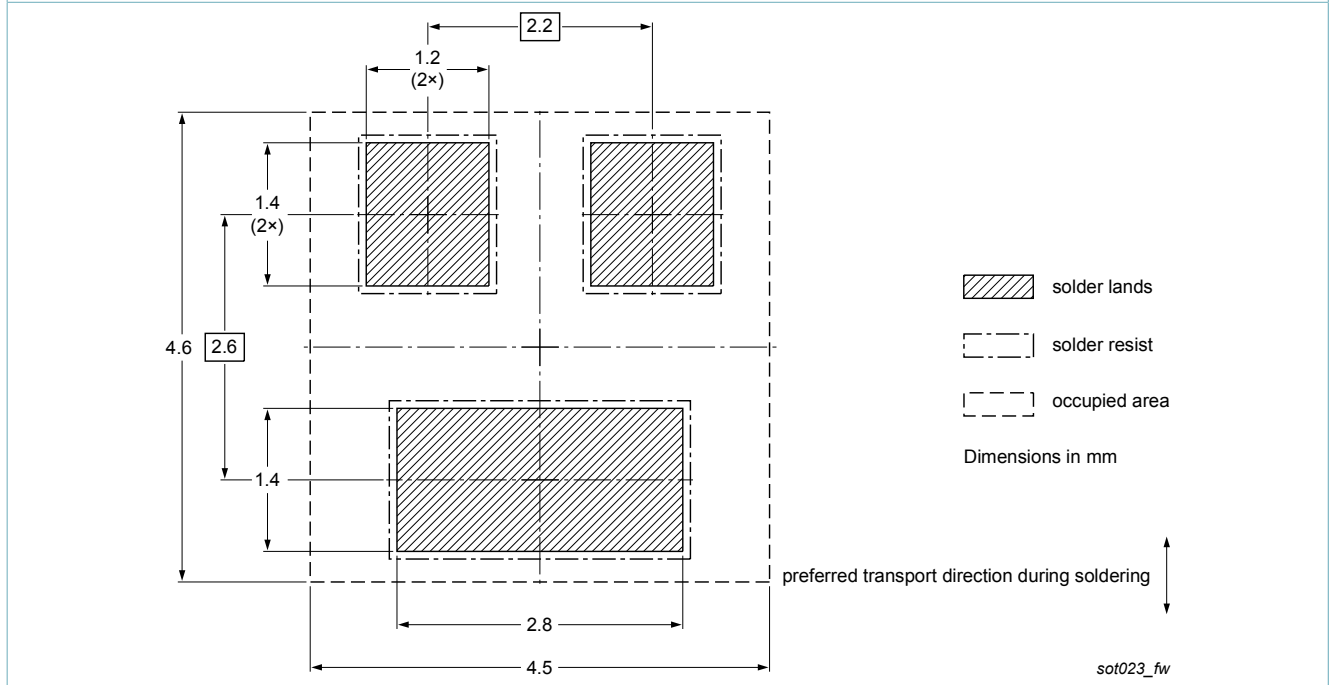


Fig. 20. Wave soldering footprint for TO-236AB (SOT23)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMV30XPEA v.1	20151030	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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