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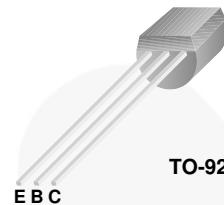
July 2014

# PN222A

## NPN General-Purpose Amplifier

### Features

- This device is for use as a medium power amplifier and switch requiring collector currents up to 500mA.



### Ordering Information

Part Number	Top Mark	Package	Packing Method
PN2222ABU	PN2222A	TO-92 3L	Bulk
PN2222ATA	PN2222A	TO-92 3L	Ammo
PN2222ATF	PN2222A	TO-92 3L	Tape and Reel
PN2222ATFR	PN2222A	TO-92 3L	Tape and Reel

### Absolute Maximum Ratings<sup>(1), (2)</sup>

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Unit
$V_{CEO}$	Collector-Emitter Voltage	40	V
$V_{CBO}$	Collector-Base Voltage	75	V
$V_{EBO}$	Emitter-Base Voltage	6.0	V
$I_C$	Collector Current	1.0	A
$T_{STG}$	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$

#### Note:

1. These rating are based on a maximum junction temperature of  $150^\circ\text{C}$ .
2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty-cycle operation.

**Thermal Characteristics<sup>(3)</sup>**

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Max.	Unit
$P_D$	Total Device Dissipation	625	mW
	Derate Above $25^\circ\text{C}$	5.0	mW/ $^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	$^\circ\text{C}/\text{W}$

**Note:**

3. PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

## Electrical Characteristics

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

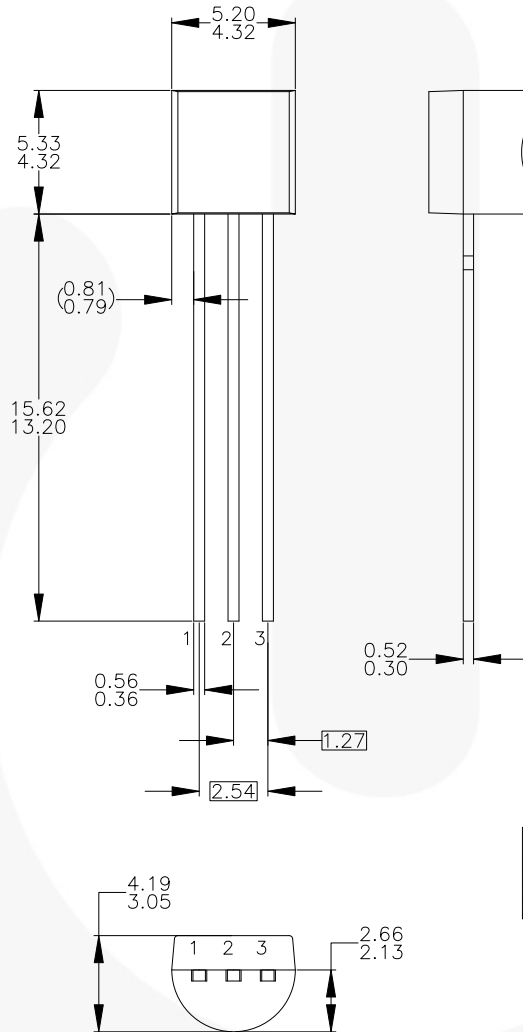
Symbol	Parameter	Conditions	Min.	Max.	Unit
<b>Off Characteristics</b>					
$BV_{(BR)CEO}$	Collector-Emitter Breakdown Voltage <sup>(4)</sup>	$I_C = 10\text{ mA}, I_B = 0$	40		V
$BV_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 10\text{ }\mu\text{A}, I_E = 0$	75		V
$BV_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = 10\text{ }\mu\text{A}, I_C = 0$	6.0		V
$I_{CEX}$	Collector Cut-Off Current	$V_{CE} = 60\text{ V}, V_{EB(off)} = 3.0\text{ V}$		10	nA
$I_{CBO}$	Collector Cut-Off Current	$V_{CB} = 60\text{ V}, I_E = 0$		0.01	$\mu\text{A}$
		$V_{CB} = 60\text{ V}, I_E = 0, T_A = 125^\circ\text{C}$		10	
$I_{EBO}$	Emitter Cut-Off Current	$V_{EB} = 3.0\text{ V}, I_C = 0$		10	nA
$I_{BL}$	Base Cut-Off Current	$V_{CE} = 60\text{ V}, V_{EB(off)} = 3.0\text{ V}$		20	nA
<b>On Characteristics</b>					
$h_{FE}$	DC Current Gain	$I_C = 0.1\text{ mA}, V_{CE} = 10\text{ V}$	35		
		$I_C = 1.0\text{ mA}, V_{CE} = 10\text{ V}$	50		
		$I_C = 10\text{ mA}, V_{CE} = 10\text{ V}$	75		
		$I_C = 10\text{ mA}, V_{CE} = 10\text{ V}, T_A = -55^\circ\text{C}$	35		
		$I_C = 150\text{ mA}, V_{CE} = 10\text{ V}^{(4)}$	100	300	
		$I_C = 150\text{ mA}, V_{CE} = 1\text{ V}^{(4)}$	50		
		$I_C = 500\text{ mA}, V_{CE} = 10\text{ V}^{(4)}$	40		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage <sup>(4)</sup>	$I_C = 150\text{ mA}, I_B = 15\text{ mA}$		0.3	V
		$I_C = 500\text{ mA}, I_B = 50\text{ mA}$		1.0	
$V_{BE(sat)}$	Base-Emitter Saturation Voltage <sup>(4)</sup>	$I_C = 150\text{ mA}, I_B = 15\text{ mA}$	0.6	1.2	V
		$I_C = 500\text{ mA}, I_B = 50\text{ mA}$		2.0	
<b>Small Signal Characteristics</b>					
$f_T$	Current Gain Bandwidth Product	$I_C = 20\text{ mA}, V_{CE} = 20\text{ V}, f = 100\text{ MHz}$	300		MHz
$C_{obo}$	Output Capacitance	$V_{CB} = 10\text{ V}, I_E = 0, f = 1\text{ MHz}$		8.0	pF
$C_{ibo}$	Input Capacitance	$V_{EB} = 0.5\text{ V}, I_C = 0, f = 1\text{ MHz}$		25	pF
$rb'C_c$	Collector Base Time Constant	$I_C = 20\text{ mA}, V_{CB} = 20\text{ V}, f = 31.8\text{ MHz}$		150	pS
NF	Noise Figure	$I_C = 100\text{ }\mu\text{A}, V_{CE} = 10\text{ V}, R_S = 1.0\text{ k}\Omega, f = 1.0\text{ kHz}$		4.0	dB
$Re(h_{ie})$	Real Part of Common-Emitter High Frequency Input Impedance	$I_C = 20\text{ mA}, V_{CE} = 20\text{ V}, f = 300\text{ MHz}$		60	$\Omega$
<b>Switching Characteristics</b>					
$t_d$	Delay Time	$V_{CC} = 30\text{ V}, V_{EB(off)} = 0.5\text{ V}, I_C = 150\text{ mA}, I_{B1} = 15\text{ mA}$		10	ns
$t_r$	Rise Time			25	ns
$t_s$	Storage Time	$V_{CC} = 30\text{ V}, I_C = 150\text{ mA}, I_{B1} = I_{B2} = 15\text{ mA}$		225	ns
$t_f$	Fall Time			60	ns

### Note:

4. Pulse test: pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2.0\%$ .

Physical Dimensions

TO-92 (Bulk)



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994.
- D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:

- P - BIPOLAR
- F - JFET
- M - DMOS
- E - EMITTER
- B - BASE
- C - COLLECTOR
- D - DRAIN
- S - SOURCE
- G - GATE

- E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEABLE AT JFET "F" OPTION.
- F) DRAWING FILENAME: MKT-ZA03DREV3.

Figure 1. 3-LEAD, TO92, JEDEC TO-92 COMPLIANT STRAIGHT LEAD CONFIGURATION (OLD TO92AM3)

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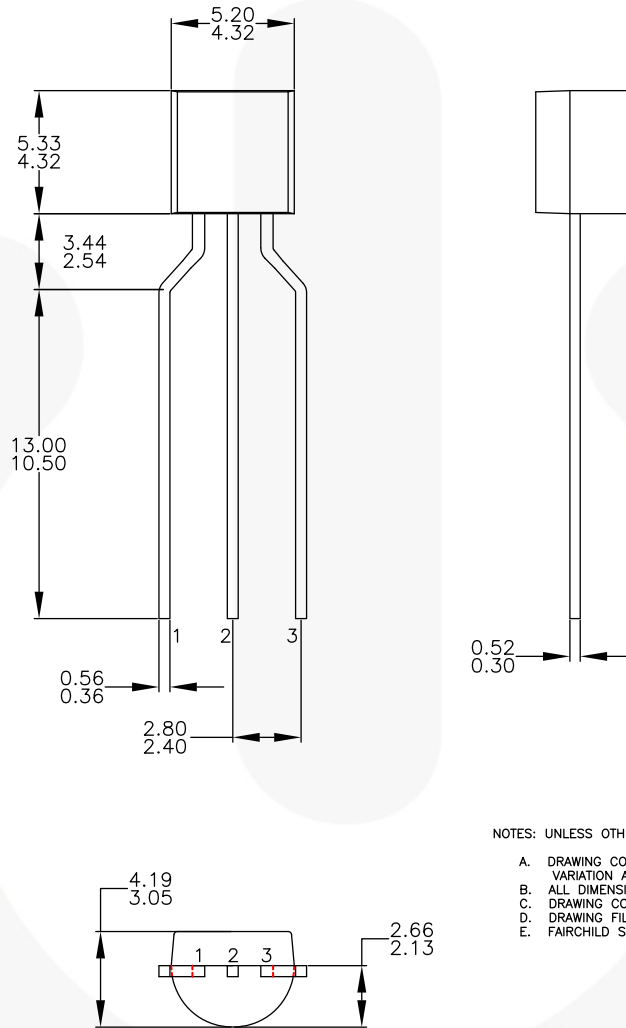
<http://www.fairchildsemi.com/dwg/ZA/ZA03D.pdf>

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Physical Dimensions (Continued)

TO-92 (Ammo, Tape and Reel)



NOTES: UNLESS OTHERWISE SPECIFIED

- A. DRAWING CONFORMS TO JEDEC MS-013, VARIATION AC.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5M-2009.
- D. DRAWING FILENAME: MKT-ZA03FREV3.
- E. FAIRCHILD SEMICONDUCTOR.

Figure 2. 3-LEAD, TO-92, MOLDED 0.200 IN LINE SPACING LEAD FORM (J61Z OPTION)

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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