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PN512

Full NFC Forum-compliant frontend

Rev. 5.2 — 16 June 2016
111352

Product data sheet
COMPANY PUBLIC

1. General description

PN512 is the most broadly adopted NFC frontend - powering more than 10 billion NFC transactions per year.

It is a highly integrated NFC frontend for contactless communication at 13.56 MHz. This NFC frontend utilizes an outstanding modulation and demodulation concept completely integrated for different kinds of contactless communication methods and protocols at 13.56 MHz.

The PN512 NFC frontend supports 4 different operating modes

- Reader/Writer mode supporting ISO/IEC 14443A/MIFARE and FeliCa scheme
- Reader/Writer mode supporting ISO/IEC 14443B
- Card Operation mode supporting ISO/IEC 14443A/MIFARE and FeliCa scheme
- NFCIP-1 mode

Enabled in Reader/Writer mode for ISO/IEC 14443A/MIFARE, the PN512's internal transmitter part is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443A/ MIFARE cards and transponders without additional active circuitry. The receiver part provides a robust and efficient implementation of a demodulation and decoding circuitry for signals from ISO/IEC 14443A/MIFARE compatible cards and transponders. The digital part handles the complete ISO/IEC 14443A framing and error detection (Parity and CRC).

Enabled in Reader/Writer mode for FeliCa, the PN512 NFC frontend supports the FeliCa communication scheme. The receiver part provides a robust and efficient implementation of the demodulation and decoding circuitry for FeliCa coded signals. The digital part handles the FeliCa framing and error detection like CRC. The PN512 supports contactless communication using FeliCa Higher transfer speeds up to 424 kbit/s in both directions.

The PN512 supports all layers of the ISO/IEC 14443B reader/writer communication scheme, given correct implementation of additional components, like oscillator, power supply, coil etc. and provided that standardized protocols, e.g. like ISO/IEC 14443-4 and/or ISO/IEC 14443B anticollision are correctly implemented.

In Card Operation mode, the PN512 NFC frontend is able to answer to a reader/writer command either according to the FeliCa or ISO/IEC 14443A/MIFARE card interface scheme. The PN512 generates the digital load modulated signals and in addition with an external circuit the answer can be sent back to the reader/writer. A complete card functionality is only possible in combination with a secure IC using the S^2C interface.

Additionally, the PN512 NFC frontend offers the possibility to communicate directly to an NFCIP-1 device in the NFCIP-1 mode. The NFCIP-1 mode offers different communication mode and transfer speeds up to 424 kbit/s according to the Ecma 340 and ISO/IEC 18092 NFCIP-1 Standard. The digital part handles the complete NFCIP-1 framing and error detection.

Various host controller interfaces are implemented:

- 8-bit parallel interface[1]
- SPI interface
- serial UART (similar to RS232 with voltage levels according pad voltage supply)
- I^2C interface.

1.1 Different available versions

The PN512 is available in three versions:

- PN5120A0HN1/C2 (HVQFN32), PN5120A0HN/C2 (HVQFN40) and PN5120A0ET/C2 (TFBGA64), hereafter named as version 2.0

- PN512AA0HN1/C2 (HVQFN32) and PN512AA0HN1/C2BI (HVQFN32 with Burn In), hereafter named as industrial version, fulfilling the automotive qualification stated in AEC-Q100 grade 3 from the Automotive Electronics Council, defining the critical stress test qualification for automotive integrated circuits (ICs).

  The customer recognizes that:

  – since the product was not originally designed for automotive use, it will not be possible to achieve the levels of quality and failure analysis that are normally associated with products explicitly designed for automotive use.
  – the product qualification conforms to AEC-Q100.
  – all product production locations are certified according to TS16949.

- PN5120A0HN1/C1(HVQFN32) and PN5120A0HN/C1 (HVQFN40), hereafter named as version 1.0

The data sheet describes the functionality for the industrial version and version 2.0. The differences of the version 1.0 to the version 2.0 are summarized in Section 20. The industrial version has only differences within the outlined characteristics and limitations.

1. 8-bit parallel Interface only available in HVQFN40 package.

2. Features and benefits

- Includes NXP ISO/IEC14443-A, Innovatron ISO/IEC14443-B and NXP MIFARE Crypto 1 intellectual property licensing rights
- Fast and cost-efficient NFC design startup
- Highly integrated analog circuitry to demodulate and decode responses
- Buffered output drivers for connecting an antenna with the minimum number of external components
- Integrated RF Level detector
- Integrated data mode detector
- Supports ISO/IEC 14443 A/MIFARE
- Supports ISO/IEC 14443 B Read/Write modes
- Typical operating distance in Read/Write mode up to 50 mm depending on the antenna size and tuning
- Typical operating distance in NFCIP-1 mode up to 50 mm depending on the antenna size and tuning and power supply
- Typical operating distance in ISO/IEC 14443A/MIFARE card or FeliCa Card Operation mode of about 100 mm depending on the antenna size and tuning and the external field strength
- Supports MIFARE Classic encryption in Reader/Writer mode
- ISO/IEC 14443A higher transfer speed communication at 212 kbit/s and 424 kbit/s
- Contactless communication according to the FeliCa scheme at 212 kbit/s and 424 kbit/s
- Integrated RF interface for NFCIP-1 up to 424 kbit/s
- S^2C interface
- Additional power supply to directly supply the smart card IC connected via S^2C
- Supported host interfaces
  - SPI up to 10 Mbit/s
  - I^2C-bus interface up to 400 kBd in Fast mode, up to 3400 kBd in High-speed mode
  - RS232 Serial UART up to 1228.8 kBd, with voltage levels dependant on pin voltage supply
  - 8-bit parallel interface with and without Address Latch Enable
- FIFO buffer handles 64 byte send and receive
- Flexible interrupt modes
- Hard reset with low power function
- Power-down mode per software
- Programmable timer
- Internal oscillator for connection to 27.12 MHz quartz crystal
- 2.5 V to 3.6 V power supply
- CRC coprocessor
- Programmable I/O pins
- Internal self-test

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	analog supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	-	3.6	V
V_{DDD}	digital supply voltage						
$V_{DD(TVDD)}$	TVDD supply voltage						
$V_{DD(PVDD)}$	PVDD supply voltage		[3]	1.6	-	3.6	V
$V_{DD(SVDD)}$	SVDD supply voltage	$V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V		1.6	-	3.6	V
I_{pd}	power-down current	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)} = 3$ V					
		hard power-down; pin NRSTPD set LOW	[4]	-	-	5	µA
		soft power-down; RF level detector on	[4]	-	-	10	µA
I_{DDD}	digital supply current	pin DVDD; $V_{DDD} = 3$ V		-	6.5	9	mA
I_{DDA}	analog supply current	pin AVDD; $V_{DDA} = 3$ V, CommandReg register's RcvOff bit = 0		-	7	10	mA
		pin AVDD; receiver switched off; $V_{DDA} = 3$ V, CommandReg register's RcvOff bit = 1		-	3	5	mA
$I_{DD(PVDD)}$	PVDD supply current	pin PVDD	[5]	-	-	40	mA
$I_{DD(TVDD)}$	TVDD supply current	pin TVDD; continuous wave	[6][7][8]	-	60	100	mA
T_{amb}	ambient temperature	HVQFN32, HVQFN40, TFBGA64		−30		+85	°C
Industrial version PN512AA0HN1:							
I_{pd}	power-down current	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)} = 3$ V					
		hard power-down; pin NRSTPD set LOW	[4]	-	-	15	µA
		soft power-down; RF level detector on	[4]	-	-	30	µA
T_{amb}	ambient temperature	HVQFN32		−40	-	+90	°C

[1] Supply voltages below 3 V reduce the performance in, for example, the achievable operating distance.

[2] V_{DDA}, V_{DDD} and $V_{DD(TVDD)}$ must always be the same voltage.

[3] $V_{DD(PVDD)}$ must always be the same or lower voltage than V_{DDD}.

[4] I_{pd} is the total current for all supplies.

[5] $I_{DD(PVDD)}$ depends on the overall load at the digital pins.

[6] $I_{DD(TVDD)}$ depends on $V_{DD(TVDD)}$ and the external circuit connected to pins TX1 and TX2.

[7] During typical circuit operation, the overall current is below 100 mA.

[8] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between pins TX1 and TX2 at 13.56 MHz.

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN5120A0HN1/C2	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
PN5120A0HN/C2	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-1
PN512AA0HN1/C2	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
PN512AA0HN1/C2BI	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
PN5120A0HN1/C1	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
PN5120A0HN/C1	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-1
PN5120A0ET/C2	TFBGA64	plastic thin fine-pitch ball grid array package; 64 balls	SOT1336-1

5. Block diagram

The analog interface handles the modulation and demodulation of the analog signals according to the Card Receiving mode, Reader/Writer mode and NFCIP-1 mode communication scheme.

The RF level detector detects the presence of an external RF-field delivered by the antenna to the RX pin.

The Data mode detector detects a MIFARE, FeliCa or NFCIP-1 mode in order to prepare the internal receiver to demodulate signals, which are sent to the PN512.

The communication (S^2C) interface provides digital signals to support communication for transfer speeds above 424 kbit/s and digital signals to communicate to a secure IC.

The contactless UART manages the protocol requirements for the communication protocols in cooperation with the host. The FIFO buffer ensures fast and convenient data transfer to and from the host and the contactless UART and vice versa.

Various host interfaces are implemented to meet different customer requirements.

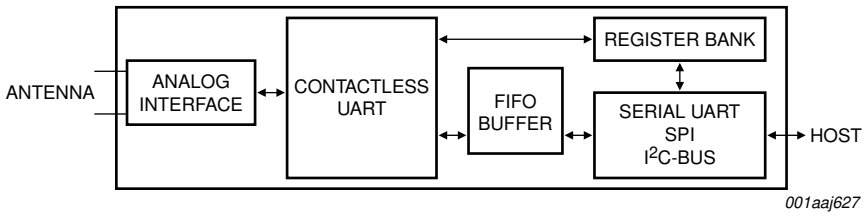

Fig 1. Simplified block diagram of the PN512

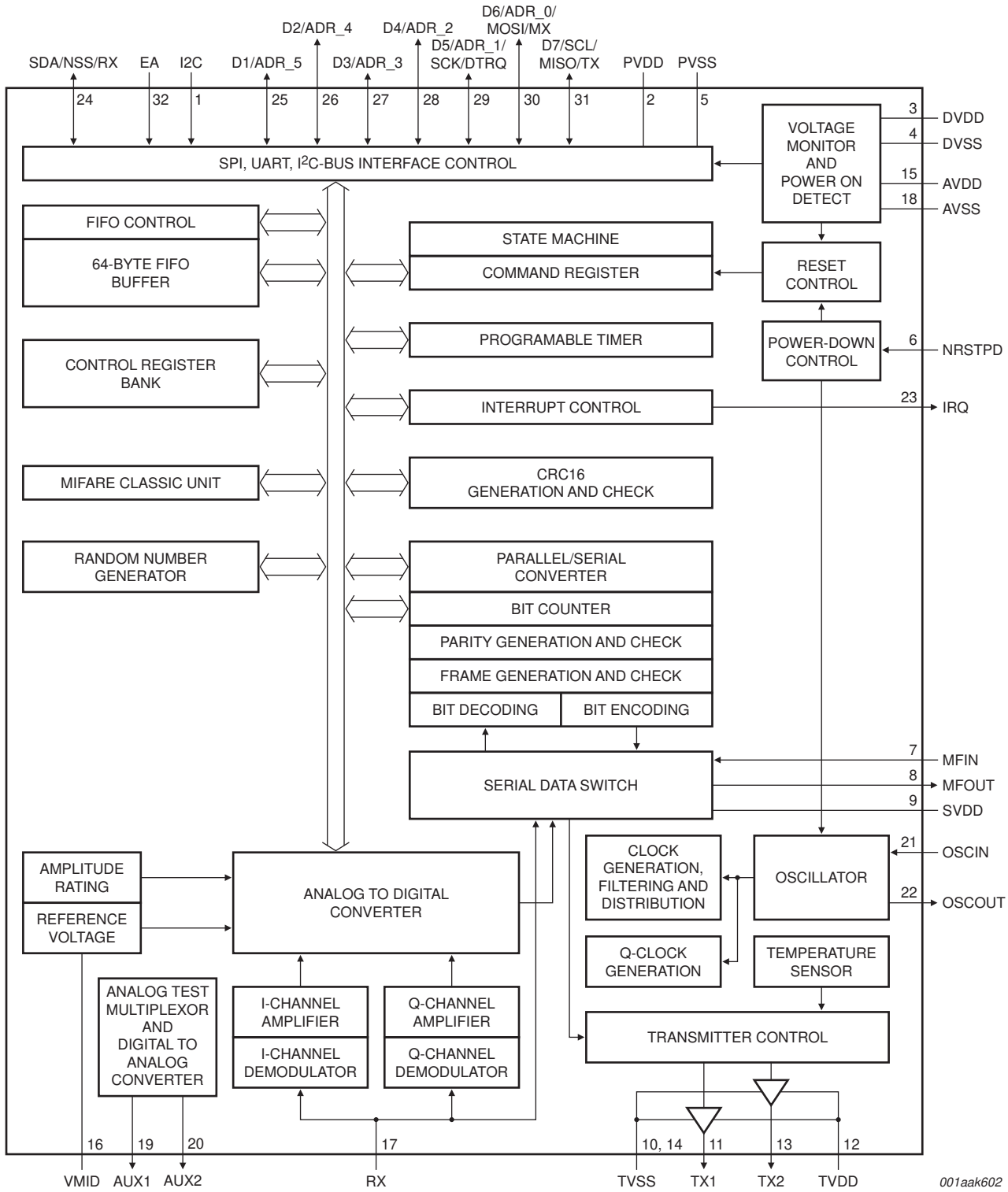

Fig 2. Detailed block diagram of the PN512

6. Pinning information

6.1 Pinning

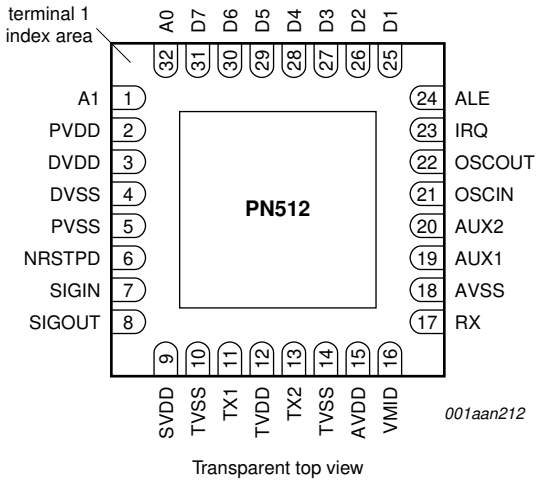

Fig 3. Pinning configuration HVQFN32 (SOT617-1)

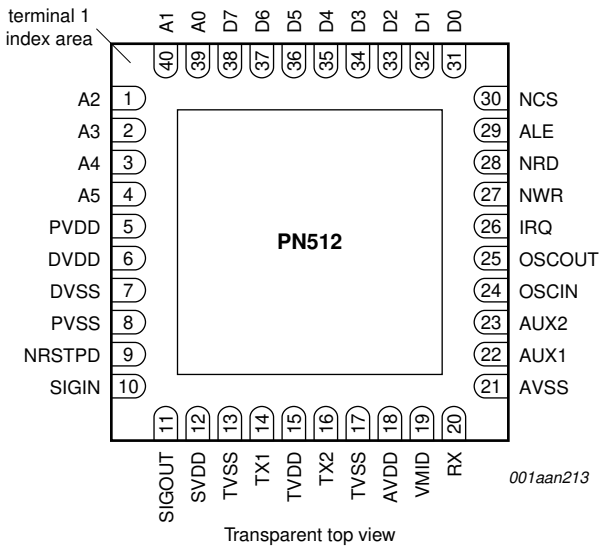

Fig 4. Pinning configuration HVQFN40 (SOT618-1)

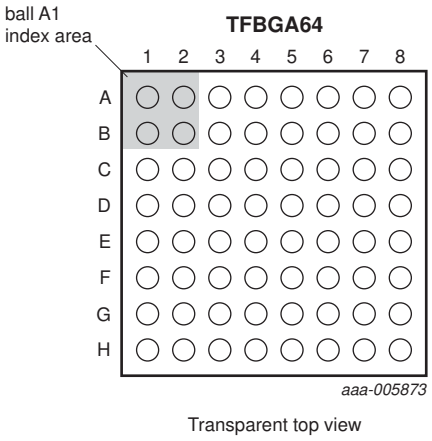

Fig 5. Pin configuration TFBGA64 (SOT1336-1)

6.2 Pin description

Table 3. Pin description HVQFN32

Pin	Symbol	Type	Description
1	A1	I	**Address Line**
2	PVDD	PWR	**Pad power supply**
3	DVDD	PWR	**Digital Power Supply**
4	DVSS	PWR	**Digital Ground**
5	PVSS	PWR	**Pad power supply ground**
6	NRSTPD	I	**Not Reset and Power Down:** When LOW, internal current sinks are switched off, the oscillator is inhibited, and the input pads are disconnected from the outside world. With a positive edge on this pin the internal reset phase starts.
7	SIGIN	I	**Communication Interface Input:** accepts a digital, serial data stream
8	SIGOUT	O	**Communication Interface Output**: delivers a serial data stream
9	SVDD	PWR	**S2C Pad Power Supply:** provides power to the S^2C pads
10	TVSS	PWR	**Transmitter Ground:** supplies the output stage of TX1 and TX2
11	TX1	O	**Transmitter 1:** delivers the modulated 13.56 MHz energy carrier
12	TVDD	PWR	**Transmitter Power Supply:** supplies the output stage of TX1 and TX2
13	TX2	O	**Transmitter 2:** delivers the modulated 13.56 MHz energy carrier
14	TVSS	PWR	**Transmitter Ground:** supplies the output stage of TX1 and TX2
15	AVDD	PWR	**Analog Power Supply**
16	VMID	PWR	**Internal Reference Voltage:** This pin delivers the internal reference voltage.
17	RX	I	**Receiver Input**
18	AVSS	PWR	**Analog Ground**
19	AUX1	O	**Auxiliary Outputs:** These pins are used for testing.
20	AUX2	O	
21	OSCIN	I	**Crystal Oscillator Input:** input to the inverting amplifier of the oscillator. This pin is also the input for an externally generated clock (f_{osc} = 27.12 MHz).
22	OSCOUT	O	**Crystal Oscillator Output:** Output of the inverting amplifier of the oscillator.
23	IRQ	O	**Interrupt Request:** output to signal an interrupt event
24	ALE	I	**Address Latch Enable:** signal to latch AD0 to AD5 into the internal address latch when HIGH.
25 to 31	D1 to D7	I/O	**8-bit Bi-directional Data Bus.** **Remark:** An 8-bit parallel interface is not available. **Remark:** If the host controller selects I^2C as digital host controller interface, these pins can be used to define the I^2C address. **Remark:** For serial interfaces this pins can be used for test signals or I/Os.
32	A0	I	**Address Line**

Table 4. Pin description HVQFN40

Pin	Symbol	Type	Description
1 to 4	A2 to A5	I	**Address Line**
5	PVDD	PWR	**Pad power supply**
6	DVDD	PWR	**Digital Power Supply**
7	DVSS	PWR	**Digital Ground**
8	PVSS	PWR	**Pad power supply ground**
9	NRSTPD	I	**Not Reset and Power Down:** When LOW, internal current sinks are switched off, the oscillator is inhibited, and the input pads are disconnected from the outside world. With a positive edge on this pin the internal reset phase starts.
10	SIGIN	I	**Communication Interface Input:** accepts a digital, serial data stream
11	SIGOUT	O	**Communication Interface Output**: delivers a serial data stream
12	SVDD	PWR	**S^2C Pad Power Supply:** provides power to the S^2C pads
13	TVSS	PWR	**Transmitter Ground:** supplies the output stage of TX1 and TX2
14	TX1	O	**Transmitter 1:** delivers the modulated 13.56 MHz energy carrier
15	TVDD	PWR	**Transmitter Power Supply:** supplies the output stage of TX1 and TX2
16	TX2	O	**Transmitter 2:** delivers the modulated 13.56 MHz energy carrier
17	TVSS	PWR	**Transmitter Ground:** supplies the output stage of TX1 and TX2
18	AVDD	PWR	**Analog Power Supply**
19	VMID	PWR	**Internal Reference Voltage:** This pin delivers the internal reference voltage.
20	RX	I	**Receiver Input**
21	AVSS	PWR	**Analog Ground**
22	AUX1	O	**Auxiliary Outputs:** These pins are used for testing.
23	AUX2	O	
24	OSCIN	I	**Crystal Oscillator Input:** input to the inverting amplifier of the oscillator. This pin is also the input for an externally generated clock (f_{osc} = 27.12 MHz).
25	OSCOUT	O	**Crystal Oscillator Output:** Output of the inverting amplifier of the oscillator.
26	IRQ	O	**Interrupt Request:** output to signal an interrupt event
27	NWR	I	**Not Write:** strobe to write data (applied on D0 to D7) into the PN512 register
28	NRD	I	**Not Read:** strobe to read data from the PN512 register (applied on D0 to D7)
29	ALE	I	**Address Latch Enable:** signal to latch AD0 to AD5 into the internal address latch when HIGH.
30	NCS	I	**Not Chip Select:** selects and activates the host controller interface of the PN512
31 to 38	D0 to D7	I/O	**8-bit Bi-directional Data Bus.** **Remark:** For serial interfaces this pins can be used for test signals or I/Os. **Remark:** If the host controller selects I^2C as digital host controller interface, these pins can be used to define the I^2C address.
39 to 40	A0 to A1	I	**Address Line**

Table 5. Pin description TFBGA64

Pin	Symbol	Type	Description
A1 to A5, A8, B3, B4, B8, E1	PVSS	PWR	**Pad power supply ground**
A6	D4	I/O	**8-bit Bi-directional Data Bus.**
A7	D2	I/O	**Remark:** For serial interfaces this pins can be used for test signals or I/Os. **Remark:** If the host controller selects I^2C as digital host controller interface, these pins can be used to define the I^2C address.
B1	PVDD	PWR	**Pad power supply**
B2	A0	I	**Address Line**
B5	D5	I/O	**8-bit Bi-directional Data Bus.**
B6	D3	I/O	**Remark:** For serial interfaces this pins can be used for test signals or I/Os.
B7	D1	I/O	**Remark:** If the host controller selects I^2C as digital host controller interface, these pins can be used to define the I^2C address.
C1	DVDD	PWR	**Digital Power Supply**
C2	A1	I	**Address Line**
C3	D7	I/O	**8-bit Bi-directional Data Bus.**
C4	D6	I/O	**Remark:** For serial interfaces this pins can be used for test signals or I/Os. **Remark:** If the host controller selects I^2C as digital host controller interface, these pins can be used to define the I^2C address.
C5	IRQ	O	**Interrupt Request:** output to signal an interrupt event
C6	ALE	I	**Address Latch Enable:** signal to latch AD0 to AD5 into the internal address latch when HIGH.
C7, C8, D6, D8, E6, E8, F7, G8, H8	AVSS	PWR	**Analog Ground**
D1	DVSS	PWR	**Digital Ground**
D2	NRSTPD	I	**Not Reset and Power Down:** When LOW, internal current sinks are switched off, the oscillator is inhibited, and the input pads are disconnected from the outside world. With a positive edge on this pin the internal reset phase starts.
D3 to D5, E3 to E5, F3, F4, G1 to G6, H1, H2, H6	TVSS	PWR	**Transmitter Ground:** supplies the output stage of TX1 and TX2
D7	OSCOUT	O	**Crystal Oscillator Output:** Output of the inverting amplifier of the oscillator.
E2	SIGIN	I	**Communication Interface Input:** accepts a digital, serial data stream
E7	OSCIN	I	**Crystal Oscillator Input:** input to the inverting amplifier of the oscillator. This pin is also the input for an externally generated clock (f_{osc} = 27.12 MHz).
F1	SVDD	PWR	**S^2C Pad Power Supply:** provides power to the S^2C pads
F2	SIGOUT	O	**Communication Interface Output**: delivers a serial data stream
F5	AUX1	O	**Auxiliary Outputs:** These pins are used for testing.
F6	AUX2	O	
F8	RX	I	**Receiver Input**
G7	VMID	PWR	**Internal Reference Voltage:** This pin delivers the internal reference voltage.
H3	TX1	O	**Transmitter 1:** delivers the modulated 13.56 MHz energy carrier

Table 5. Pin description TFBGA64

Pin	Symbol	Type	Description
H4	TVDD	PWR	**Transmitter Power Supply:** supplies the output stage of TX1 and TX2
H5	TX2	O	**Transmitter 2:** delivers the modulated 13.56 MHz energy carrier
H7	AVDD	PWR	**Analog Power Supply**

7. Functional description

The PN512 transmission module supports the Read/Write mode for ISO/IEC 14443 A/MIFARE and ISO/IEC 14443 B using various transfer speeds and modulation protocols.

PN512 NFC frontend supports the following operating modes:

- Reader/Writer mode supporting ISO/IEC 14443A/MIFARE and FeliCa scheme
- Card Operation mode supporting ISO/IEC 14443A/MIFARE and FeliCa scheme
- NFCIP-1 mode

The modes support different transfer speeds and modulation schemes. The following chapters will explain the different modes in detail.

Note: All indicated modulation indices and modes in this chapter are system parameters. This means that beside the IC settings a suitable antenna tuning is required to achieve the optimum performance.

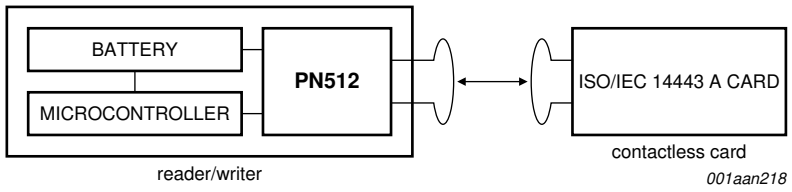

Fig 6. PN512 Read/Write mode

7.1 ISO/IEC 14443 A/MIFARE functionality

The physical level communication is shown in Figure 7.

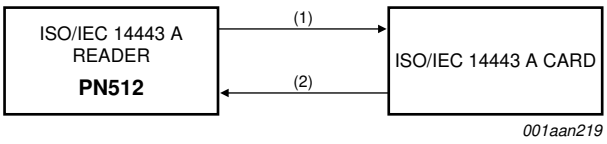

Fig 7. ISO/IEC 14443 A/MIFARE Read/Write mode communication diagram

The physical parameters are described in Table 4.

Table 6. Communication overview for ISO/IEC 14443 A/MIFARE reader/writer

Communication direction	Signal type	Transfer speed		
		106 kBd	212 kBd	424 kBd
Reader to card (send data from the PN512 to a card)	reader side modulation	100 % ASK	100 % ASK	100 % ASK
	bit encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding
	bit length	128 (13.56 µs)	64 (13.56 µs)	32 (13.56 µs)

Table 6. Communication overview for ISO/IEC 14443 A/MIFARE reader/writer *...continued*

Communication direction	Signal type	Transfer speed		
		106 kBd	212 kBd	424 kBd
Card to reader (PN512 receives data from a card)	card side modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit encoding	Manchester encoding	BPSK	BPSK

The PN512's contactless UART and dedicated external host must manage the complete ISO/IEC 14443 A/MIFARE protocol. Figure 8 shows the data coding and framing according to ISO/IEC 14443 A/MIFARE.

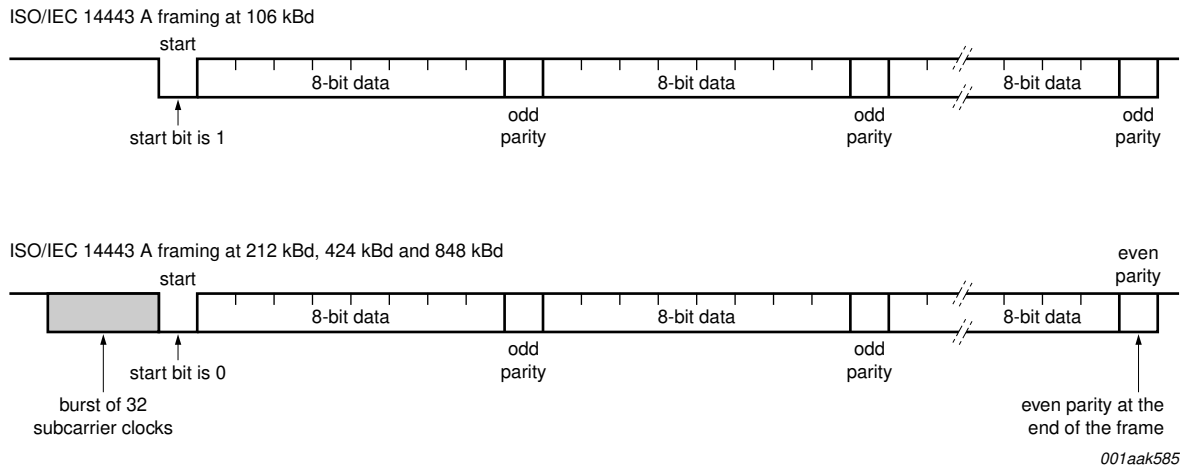

Fig 8. Data coding and framing according to ISO/IEC 14443 A

The internal CRC coprocessor calculates the CRC value based on ISO/IEC 14443 A part 3 and handles parity generation internally according to the transfer speed. Automatic parity generation can be switched off using the ManualRCVReg register's ParityDisable bit.

7.2 ISO/IEC 14443 B functionality

The PN512 reader IC fully supports international standard ISO 14443 which includes communication schemes ISO 14443 A and ISO 14443 B.

Refer to the ISO 14443 reference documents *Identification cards - Contactless integrated circuit cards - Proximity cards* (parts 1 to 4).

7.3 FeliCa reader/writer functionality

The FeliCa mode is the general reader/writer to card communication scheme according to the FeliCa specification. The following diagram describes the communication on a physical level, the communication overview describes the physical parameters.

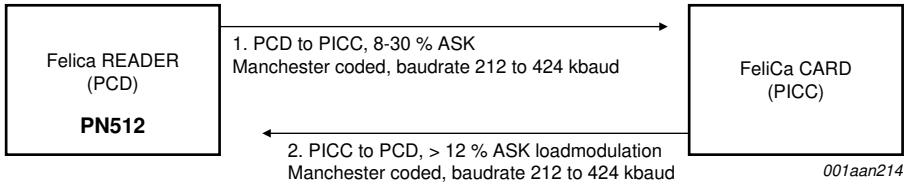

Fig 9. FeliCa reader/writer communication diagram

Table 7. Communication overview for FeliCa reader/writer

Communication direction		FeliCa	FeliCa Higher transfer speeds
	Transfer speed	**212 kbit/s**	**424 kbit/s**
PN512 → card	Modulation on reader side	8-30 % ASK	8-30 % ASK
	bit coding	Manchester Coding	Manchester Coding
	Bitlength	(64/13.56) µs	(32/13.56) µs
card → PN512	Loadmodulation on card side	> 12 % ASK	> 12 % ASK
	bit coding	Manchester coding	Manchester coding

The contactless UART of PN512 and a dedicated external host controller are required to handle the complete FeliCa protocol.

7.3.1 FeliCa framing and coding

Table 8. FeliCa framing and coding

Preamble						Sync		Len	n-Data				CRC	
00h	00h	00h	00h	00h	00h	B2h	4Dh							

To enable the FeliCa communication a 6 byte preamble (00h, 00h, 00h, 00h, 00h, 00h) and 2 bytes Sync bytes (B2h, 4Dh) are sent to synchronize the receiver.

The following Len byte indicates the length of the sent data bytes plus the LEN byte itself. The CRC calculation is done according to the FeliCa definitions with the MSB first.

To transmit data on the RF interface, the host controller has to send the Len- and data-bytes to the PN512's FIFO-buffer. The preamble and the sync bytes are generated by the PN512 automatically and must not be written to the FIFO by the host controller. The PN512 performs internally the CRC calculation and adds the result to the data frame.

Example for FeliCa CRC Calculation:

Table 9. Start value for the CRC Polynomial: (00h), (00h)

Preamble						Sync		Len	2 Data Bytes		CRC	
00h	00h	00h	00h	00h	00h	B2h	4Dh	03h	ABh	CDh	90h	35h

7.4 NFCIP-1 mode

The NFCIP-1 communication differentiates between an active and a Passive Communication mode.

- Active Communication mode means both the initiator and the target are using their own RF field to transmit data.
- Passive Communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active in terms of generating the RF field.
- Initiator: generates RF field at 13.56 MHz and starts the NFCIP-1 communication
- Target: responds to initiator command either in a load modulation scheme in Passive Communication mode or using a self generated and self modulated RF field for Active Communication mode.

In order to fully support the NFCIP-1 standard the PN512 supports the Active and Passive Communication mode at the transfer speeds 106 kbit/s, 212 kbit/s and 424 kbit/s as defined in the NFCIP-1 standard.

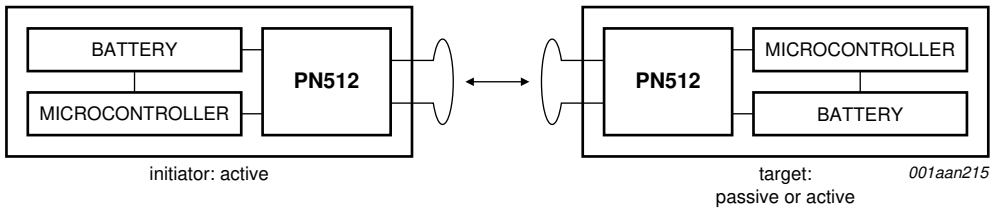

Fig 10. NFCIP-1 mode

7.4.1 Active communication mode

Active communication mode means both the initiator and the target are using their own RF field to transmit data.

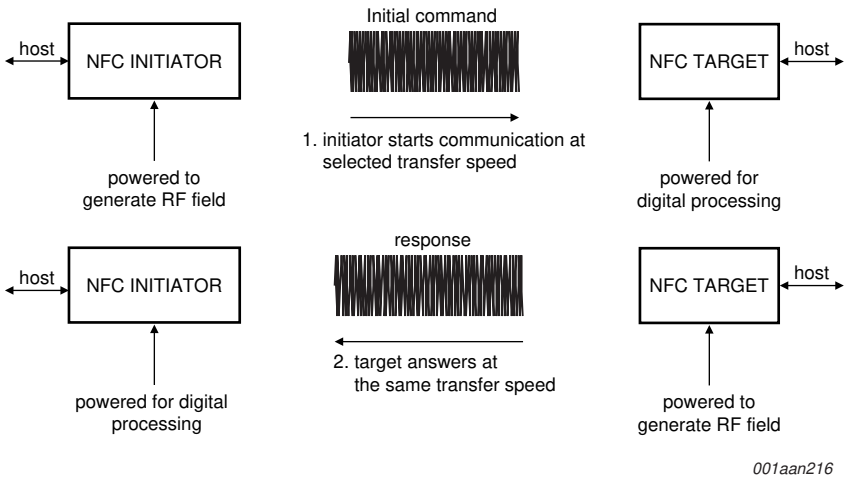

Fig 11. Active communication mode

Table 10. Communication overview for Active communication mode

Communication direction	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s	1.69 Mbit/s, 3.39 Mbit/s
Initiator → Target	According to ISO/IEC 14443A 100 % ASK, Modified Miller Coded	According to FeliCa, 8-30 % ASK Manchester Coded		digital capability to handle this communication	
Target → Initiator					

The contactless UART of PN512 and a dedicated host controller are required to handle the NFCIP-1 protocol.

Note: Transfer Speeds above 424 kbit/s are not defined in the NFCIP-1 standard. The PN512 supports these transfer speeds only with dedicated external circuits.

7.4.2 Passive communication mode

Passive Communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active meaning generating the RF field.

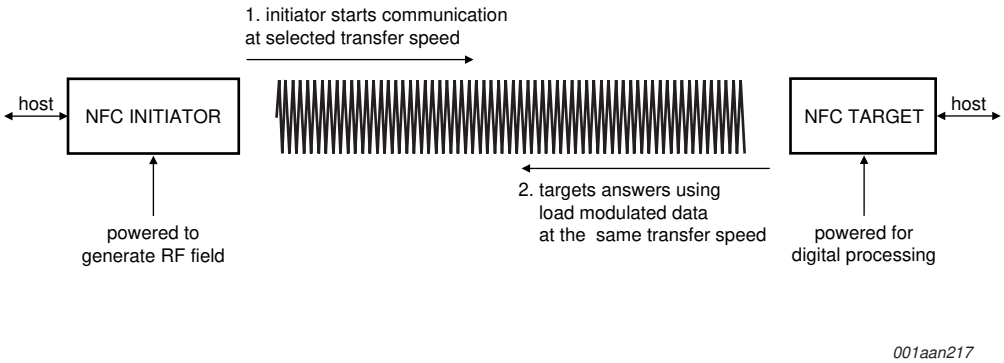

Fig 12. Passive communication mode

Table 11. Communication overview for Passive communication mode

Communication direction	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s	1.69 Mbit/s, 3.39 Mbit/s
Initiator → Target	According to ISO/IEC 14443A 100 % ASK, Modified Miller Coded	According to FeliCa, 8-30 % ASK Manchester Coded		digital capability to handle this communication	
Target → Initiator	According to ISO/IEC 14443A subcarrier load modulation, Manchester Coded	According to FeliCa, > 12 % ASK Manchester Coded			

The contactless UART of PN512 and a dedicated host controller are required to handle the NFCIP-1 protocol.

Note: Transfer Speeds above 424 kbit/s are not defined in the NFCIP-1 standard. The PN512 supports these transfer speeds only with dedicated external circuits.

7.4.3 NFCIP-1 framing and coding

The NFCIP-1 framing and coding in Active and Passive Communication mode is defined in the NFCIP-1 standard.

Table 12. Framing and coding overview

Transfer speed	Framing and Coding
106 kbit/s	According to the ISO/IEC 14443A/MIFARE scheme
212 kbit/s	According to the FeliCa scheme
424 kbit/s	According to the FeliCa scheme

7.4.4 NFCIP-1 protocol support

The NFCIP-1 protocol is not completely described in this document. For detailed explanation of the protocol refer to the NFCIP-1 standard. However the datalink layer is according to the following policy:

- Speed shall not be changed while continuum data exchange in a transaction.
- Transaction includes initialization and anticollision methods and data exchange (in continuous way, meaning no interruption by another transaction).

In order not to disturb current infrastructure based on 13.56 MHz general rules to start NFCIP-1 communication are defined in the following way.

1. Per default NFCIP-1 device is in Target mode meaning its RF field is switched off.
2. The RF level detector is active.
3. Only if application requires the NFCIP-1 device shall switch to Initiator mode.
4. Initiator shall only switch on its RF field if no external RF field is detected by RF Level detector during a time of TIDT.
5. The initiator performs initialization according to the selected mode.

7.4.5 MIFARE Card operation mode

Table 13. MIFARE Card operation mode

Communication direction		ISO/IEC 14443A/ MIFARE	MIFARE Higher transfer speeds	
	transfer speed	106 kbit/s	212 kbit/s	424 kbit/s
reader/writer → PN512	Modulation on reader side	100 % ASK	100 % ASK	100 % ASK
	bit coding	Modified Miller	Modified Miller	Modified Miller
	Bitlength	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs
PN512 → reader/ writer	Modulation on PN512 side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	Manchester coding	BPSK	BPSK

7.4.6 FeliCa Card operation mode

Table 14. FeliCa Card operation mode

Communication direction		FeliCa	FeliCa Higher transfer speeds
	Transfer speed	**212 kbit/s**	**424 kbit/s**
reader/writer → PN512	Modulation on reader side	8-30 % ASK	8-30 % ASK
	bit coding	Manchester Coding	Manchester Coding
	Bitlength	(64/13.56) μs	(32/13.56) μs
PN512 → reader/ writer	Load modulation on PN512 side	> 12 % ASK load modulation	> 12 % ASK load modulation
	bit coding	Manchester coding	Manchester coding

8. PN512 register SET

8.1 PN512 registers overview

Table 15. PN512 registers overview

Addr (hex)	Register Name	Function
Page 0: Command and Status		
0	PageReg	Selects the register page
1	CommandReg	Starts and stops command execution
2	ComIEnReg	Controls bits to enable and disable the passing of Interrupt Requests
3	DivIEnReg	Controls bits to enable and disable the passing of Interrupt Requests
4	ComIrqReg	Contains Interrupt Request bits
5	DivIrqReg	Contains Interrupt Request bits
6	ErrorReg	Error bits showing the error status of the last command executed
7	Status1Reg	Contains status bits for communication
8	Status2Reg	Contains status bits of the receiver and transmitter
9	FIFODataReg	In- and output of 64 byte FIFO-buffer
A	FIFOLevelReg	Indicates the number of bytes stored in the FIFO
B	WaterLevelReg	Defines the level for FIFO under- and overflow warning
C	ControlReg	Contains miscellaneous Control Registers
D	BitFramingReg	Adjustments for bit oriented frames
E	CollReg	Bit position of the first bit collision detected on the RF-interface
F	RFU	Reserved for future use
Page 1: Command		
0	PageReg	Selects the register page
1	ModeReg	Defines general modes for transmitting and receiving
2	TxModeReg	Defines the data rate and framing during transmission
3	RxModeReg	Defines the data rate and framing during receiving
4	TxControlReg	Controls the logical behavior of the antenna driver pins TX1 and TX2
5	TxAutoReg	Controls the setting of the antenna drivers

Table 15. PN512 registers overview *…continued*

Addr (hex)	Register Name	Function
6	TxSelReg	Selects the internal sources for the antenna driver
7	RxSelReg	Selects internal receiver settings
8	RxThresholdReg	Selects thresholds for the bit decoder
9	DemodReg	Defines demodulator settings
A	FelNFC1Reg	Defines the length of the valid range for the receive package
B	FelNFC2Reg	Defines the length of the valid range for the receive package
C	MifNFCReg	Controls the communication in ISO/IEC 14443/MIFARE and NFC target mode at 106 kbit
D	ManualRCVReg	Allows manual fine tuning of the internal receiver
E	TypeBReg	Configure the ISO/IEC 14443 type B
F	SerialSpeedReg	Selects the speed of the serial UART interface
Page 2: CFG		
0	PageReg	Selects the register page
1	CRCResultReg	Shows the actual MSB and LSB values of the CRC calculation
2		
3	GsNOffReg	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation, when the driver is switched off
4	ModWidthReg	Controls the setting of the ModWidth
5	TxBitPhaseReg	Adjust the TX bit phase at 106 kbit
6	RFCfgReg	Configures the receiver gain and RF level
7	GsNOnReg	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation when the drivers are switched on
8	CWGsPReg	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation during times of no modulation
9	ModGsPReg	Selects the conductance of the antenna driver pins TX1 and TX2 for modulation during modulation
A	TModeReg TPrescalerReg	Defines settings for the internal timer
B		
C	TReloadReg	Describes the 16-bit timer reload value
D		
E	TCounterValReg	Shows the 16-bit actual timer value
F		
Page 3: TestRegister		
0	PageReg	selects the register page
1	TestSel1Reg	General test signal configuration
2	TestSel2Reg	General test signal configuration and PRBS control
3	TestPinEnReg	Enables pin output driver on 8-bit parallel bus (Note: For serial interfaces only)
4	TestPin ValueReg	Defines the values for the 8-bit parallel bus when it is used as I/O bus
5	TestBusReg	Shows the status of the internal testbus
6	AutoTestReg	Controls the digital selftest

Table 15. PN512 registers overview *...continued*

Addr (hex)	Register Name	Function
7	VersionReg	Shows the version
8	AnalogTestReg	Controls the pins AUX1 and AUX2
9	TestDAC1Reg	Defines the test value for the TestDAC1
A	TestDAC2Reg	Defines the test value for the TestDAC2
B	TestADCReg	Shows the actual value of ADC I and Q
C-F	RFT	Reserved for production tests

8.1.1 Register bit behavior

Depending on the functionality of a register, the access conditions to the register can vary. In principle bits with same behavior are grouped in common registers. In Table 16 the access conditions are described.

Table 16. Behavior of register bits and its designation

Abbreviation	Behavior	Description
r/w	read and write	These bits can be written and read by the µ-Controller. Since they are used only for control means, there content is not influenced by internal state machines, e.g. the PageSelect-Register may be written and read by the µ-Controller. It will also be read by internal state machines, but never changed by them.
dy	dynamic	These bits can be written and read by the µ-Controller. Nevertheless, they may also be written automatically by internal state machines, e.g. the Command-Register changes its value automatically after the execution of the actual command.
r	read only	These registers hold bits, which value is determined by internal states only, e.g. the CRCReady bit can not be written from external but shows internal states.
w	write only	Reading these registers returns always ZERO.
RFU	-	These registers are reserved for future use. In case of a PN512 Version version 2.0 (VersionReg = 82h) a read access to these registers returns always the value “0”. Nevertheless this is not guaranteed for future chips versions where the value is undefined. In case of a write access, it is recommended to write always the value “0”.
RFT	-	These registers are reserved for production tests and shall not be changed.

8.2 Register description

8.2.1 Page 0: Command and status

8.2.1.1 PageReg

Selects the register page.

Table 17. PageReg register (address 00h); reset value: 00h, 0000000b

	7	6	5	4	3	2	1	0
	UsePage Select	0	0	0	0	0	PageSelect	
Access Rights	r/w	RFU	RFU	RFU	RFU	RFU	r/w	r/w

Table 18. Description of PageReg bits

Bit	Symbol	Description
7	UsePageSelect	Set to logic 1, the value of PageSelect is used as register address A5 and A4. The LSB-bits of the register address are defined by the address pins or the internal address latch, respectively. Set to logic 0, the whole content of the internal address latch defines the register address. The address pins are used as described in Section 9.1 “Automatic microcontroller interface detection”.
6 to 2	-	Reserved for future use.
1 to 0	PageSelect	The value of PageSelect is used only if UsePageSelect is set to logic 1. In this case it specifies the register page (which is A5 and A4 of the register address).

8.2.1.2 CommandReg

Starts and stops command execution.

Table 19. CommandReg register (address 01h); reset value: 20h, 00100000b

	7	6	5	4	3	2	1	0
	0	0	RcvOff	Power Down	Command			
Access Rights	RFU	RFU	r/w	dy	dy	dy	dy	dy

Table 20. Description of CommandReg bits

Bit	Symbol	Description
7 to 6	-	Reserved for future use.
5	RcvOff	Set to logic 1, the analog part of the receiver is switched off.
4	PowerDown	Set to logic 1, Soft Power-down mode is entered. Set to logic 0, the PN512 starts the wake up procedure. During this procedure this bit still shows a 1. A 0 indicates that the PN512 is ready for operations; see Section 15.2 “Soft power-down mode”. Note: The bit Power Down cannot be set, when the command SoftReset has been activated.
3 to 0	Command	Activates a command according to the Command Code. Reading this register shows, which command is actually executed (see Section 18.3 “PN512 command overview”).

8.2.1.3 CommIEnReg

Control bits to enable and disable the passing of interrupt requests.

Table 21. CommIEnReg register (address 02h); reset value: 80h, 10000000b

	7	6	5	4	3	2	1	0
	IRqInv	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn	ErrIEn	TimerIEn
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 22. Description of CommIEnReg bits

Bit	Symbol	Description
7	IRqInv	Set to logic 1, the signal on pin IRQ is inverted with respect to bit IRq in the register Status1Reg. Set to logic 0, the signal on pin IRQ is equal to bit IRq. In combination with bit IRqPushPull in register DivIEnReg, the default value of 1 ensures, that the output level on pin IRQ is 3-state.
6	TxIEn	Allows the transmitter interrupt request (indicated by bit TxIRq) to be propagated to pin IRQ.
5	RxIEn	Allows the receiver interrupt request (indicated by bit RxIRq) to be propagated to pin IRQ.
4	IdleIEn	Allows the idle interrupt request (indicated by bit IdleIRq) to be propagated to pin IRQ.
3	HiAlertIEn	Allows the high alert interrupt request (indicated by bit HiAlertIRq) to be propagated to pin IRQ.
2	LoAlertIEn	Allows the low alert interrupt request (indicated by bit LoAlertIRq) to be propagated to pin IRQ.
1	ErrIEn	Allows the error interrupt request (indicated by bit ErrIRq) to be propagated to pin IRQ.
0	TimerIEn	Allows the timer interrupt request (indicated by bit TimerIRq) to be propagated to pin IRQ.