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PN532/C1

Near Field Communication (NFC) controller

Rev. 3.6 — 28 November 2017
115436

Product data sheet
COMPANY PUBLIC

1. General description

The PN532 is a highly integrated transceiver module for contactless communication at 13.56 MHz based on the 80C51 microcontroller core. It supports 6 different operating modes:

- ISO/IEC 14443A/MIFARE Reader/Writer
- FeliCa Reader/Writer
- ISO/IEC 14443B Reader/Writer
- ISO/IEC 14443A/MIFARE Card MIFARE Classic 1K or MIFARE Classic 4K card emulation mode
- FeliCa Card emulation
- ISO/IEC 18092, ECMA 340 Peer-to-Peer

The PN532 implements a demodulator and decoder for signals from ISO/IEC 14443A/MIFARE compatible cards and transponders. The PN532 handles the complete ISO/IEC 14443A framing and error detection (Parity & CRC).

The PN532 supports MIFARE Classic 1K or MIFARE Classic 4K card emulation mode. The PN532 supports contactless communication using MIFARE Higher transfer speeds up to 424 kbit/s in both directions.

The PN532 can demodulate and decode FeliCa coded signals. The PN532 handles the FeliCa framing and error detection. The PN532 supports contactless communication using FeliCa Higher transfer speeds up to 424 kbit/s in both directions.

The PN532 supports layers 2 and 3 of the ISO/IEC 14443 B Reader/Writer communication scheme, except anticollision. This must be implemented in firmware as well as upper layers.

In card emulation mode, the PN532 is able to answer to a Reader/Writer command either according to the FeliCa or ISO/IEC 14443A/MIFARE card interface scheme. The PN532 generates the load modulation signals, either from its transmitter or from the LOADMOD pin driving an external active circuit. A complete secure card functionality is only possible in combination with a secure IC using the NFC-WI/S^{2}C interface.

Compliant to ECMA 340 and ISO/IEC 18092 NFCIP-1 Passive and Active communication modes, the PN532 offers the possibility to communicate to another NFCIP-1 compliant device, at transfer speeds up to 424 kbit/s.The PN532 handles the complete NFCIP-1 framing and error detection.

The PN532 transceiver can be connected to an external antenna for Reader/Writer or Card/PICC modes, without any additional active component.

The PN532 supports the following host interfaces:

- SPI
- I^2C
- High Speed UART (HSU)

An embedded low-dropout voltage regulator allows the device to be connected directly to a battery. In addition, a power switch is included to supply power to a secure IC.

2. Features and benefits

- 80C51 microcontroller core with 40 KB ROM and 1 KB RAM
- Highly integrated demodulator and decoder
- Buffered output drivers to connect an antenna with minimum number of external components
- Integrated RF level detector
- Integrated data mode detector
- Supports ISO/IEC 14443A/MIFARE
- Supports ISO/IEC 14443B (Reader/Writer mode only)
- Typical operating distance in Reader/Writer mode for communication to ISO/IEC 14443A/MIFARE, ISO/IEC 14443B or FeliCa cards up to 50 mm depending on antenna size and tuning
- Typical operating distance in NFCIP-1 mode up to 50 mm depending on antenna size, tuning and power supply
- Typical operating distance in ISO/IEC 14443A/MIFARE or FeliCa card emulation mode of approximately 100 mm depending on antenna size, tuning and external field strength
- Supports MIFARE Classic 1K or MIFARE Classic 4K encryption in Reader/Writer mode and MIFARE higher transfer speed communication at 212 kbit/s and 424 kbit/s
- Supports contactless communication according to the FeliCa protocol at 212 kbit/s and 424 kbit/s
- Integrated RF interface for NFCIP-1 up to 424 kbit/s
- Possibility to communicate on the RF interface above 424 kbit/s using external analog components
- Supported host interfaces
  - SPI interface
  - I^2C interface
  - High-speed UART
- Dedicated host interrupts
- Low power modes
  - Hard-Power-Down mode (1 μA typical)
  - Soft-Power-Down mode (22 μA typical)
- Automatic wake-up on I^2C, HSU and SPI interfaces when device is in Power-down mode
- Programmable timers
- Crystal oscillator
- 2.7 to 5.5 V power supply operating range
- Power switch for external secure companion chip
- Dedicated IO ports for external device control
- Integrated antenna detector for production tests
- ECMA 373 NFC-WI interface to connect an external secure IC

3. Applications

- Mobile and portable devices
- Consumer applications

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	battery supply voltage			2.7	-	5.5	V
ICV_{DD}	LDO output voltage	V_{BAT} > 3.4 V V_{SS} = 0 V	[1]	2.7	3	3.4	V
PV_{DD}	Supply voltage for host interface	V_{SS} = 0 V		1.6	-	3.6	V
SV_{DD}	Output voltage for secure IC interface	V_{SS} = 0 V (SV_{DD} Switch Enabled)		DV_{DD} -0.5	-	DV_{DD}	V
I_{HPD}	Hard-Power-Down current consumption	V_{BAT} = 5 V		-	-	2	µA
I_{SPD}	Soft-Power-Down current consumption	V_{BAT} = 5 V, RF level detector on		-	-	45	µA
I_{DVDD}	Digital supply current	V_{BAT} = 5 V, SV_{DD} switch off	[1]	-	25	-	mA
I_{SVDD}	SV_{DD} load current	V_{BAT} = 5 V, SV_{DD} switch on		-	-	30	mA
I_{AVDD}	Analog supply current	V_{BAT} = 5 V		-	6	-	mA
I_{TVDD}	Transmitter supply current	During RF transmission, V_{BAT} = 5 V		-	60[3]	150[4]	mA
P_{tot}	Continuous total power dissipation	T_{amb} = -30 to +85 °C	[2]	-	-	0.5	W
T_{amb}	ambient temperature			–30	-	+85	°C

[1] DV_{DD}, AV_{DD} and TV_{DD} must always be at the same supply voltage.

[2] The total current consumption depends on the firmware version (different internal IC clock speed)

[3] With an antenna tuned at 50 Ω at 13.56 MHz

[4] The antenna should be tuned not to exceed this current limit (the detuning effect when coupling with another device must be taken into account)

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN5321A3HN/C1xx[1][2][4]	HVQFN40	Heatsink Very thin Quad Flat package; 40 pins, plastic, body 6 x 6 x 0.85 mm; leadless; MSL level 2[3].	SOT618-1

[1] xx refers to the ROM code version. The ROM code functionalities are described in the User-Manual document. Each ROM code has its own User-Manual.

[2] This NXP IC is licensed under Innovatron's ISO/IEC 14443 Type B patent license.

[3] This is tested according the joint IPC/JEDEC standard J-STD-020C of July 2004.

[4] Purchase of an NXP Semiconductors IC that complies with one of the NFC Standards (ISO/IEC18.092; ISO/IEC21.481) does not convey an implied license under any patent right on that standards.

6. Block diagram

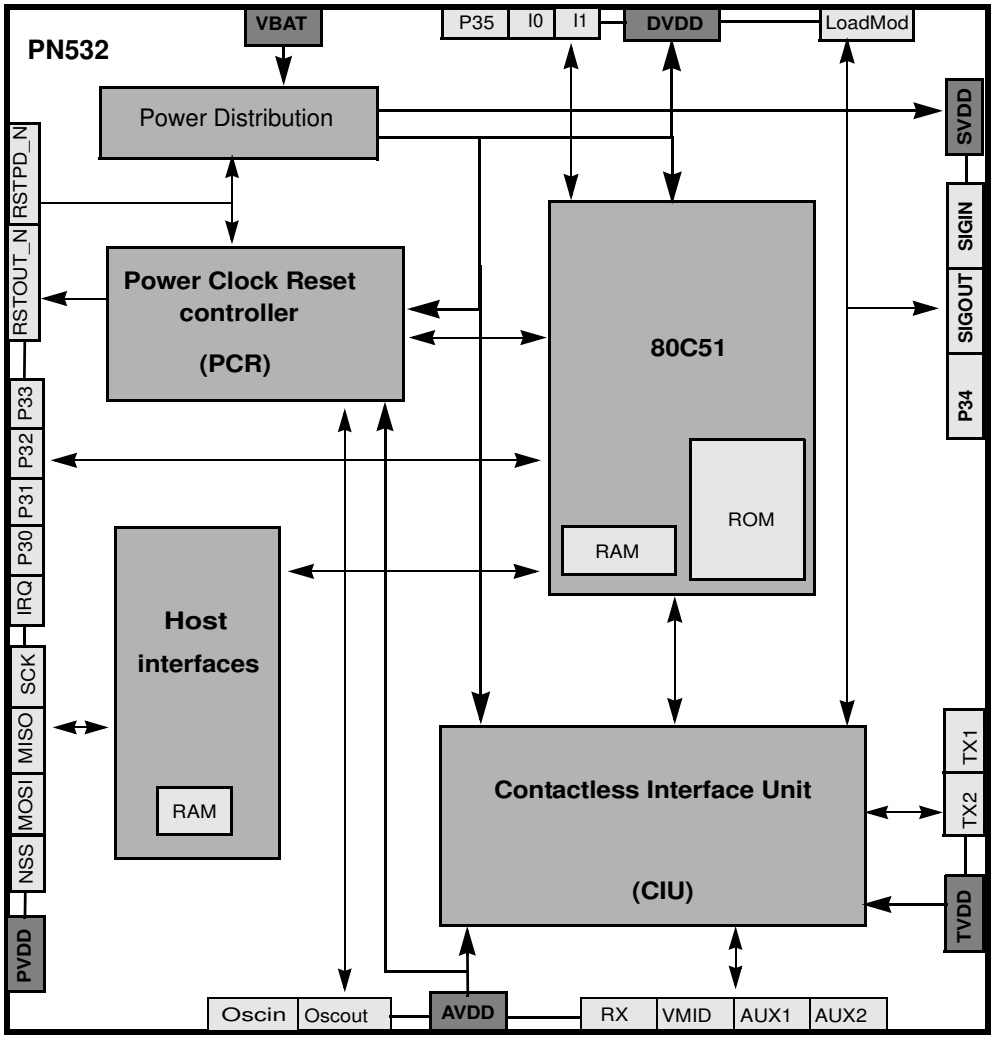

Fig 1. Block diagram of PN532

7. Pinning information

7.1 Pinning

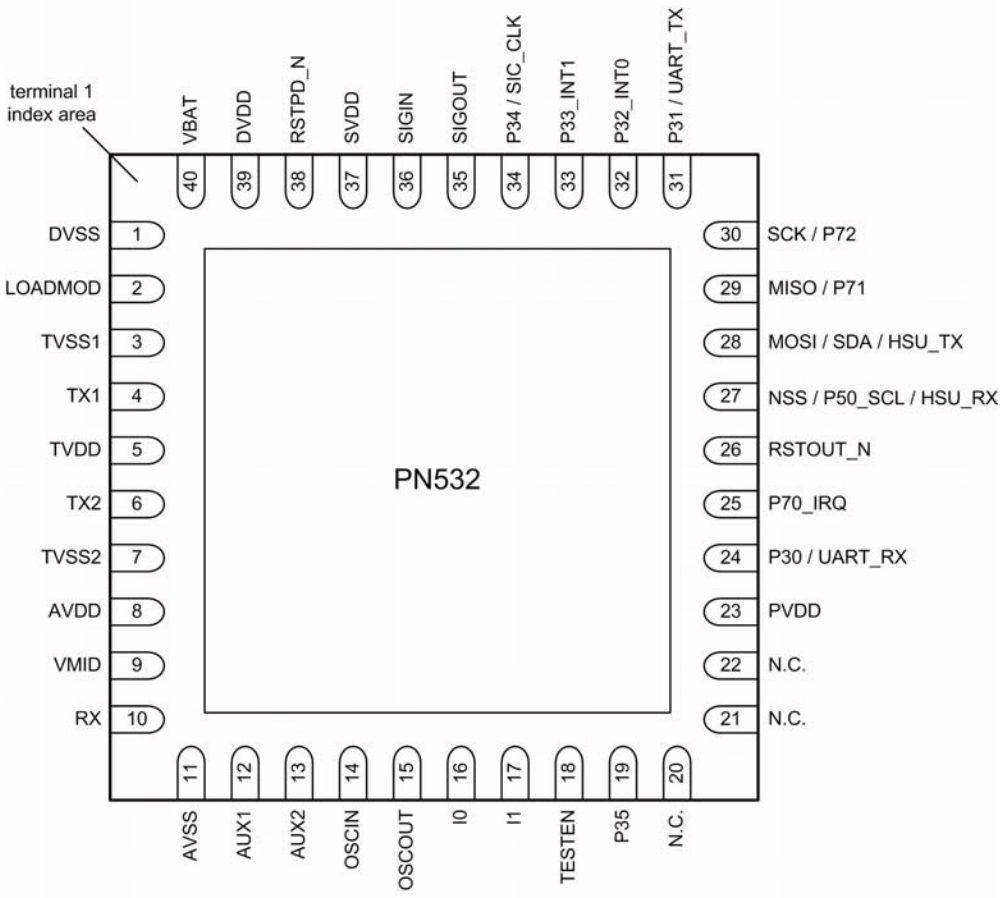

Fig 2. Pin configuration for HVQFN 40 (SOT618-1)

7.2 Pin description

Table 3. PN532 Pin description

Symbol	Pin	Type	Ref Voltage	Description
DVSS	1	PWR		Digital ground.
LOADMOD	2	O	DVDD	Load modulation signal.
TVSS1	3	PWR		Transmitter ground.
TX1	4	O	TVDD	Transmitter output 1: transmits modulated 13.56 MHz energy carrier.
TVDD	5	PWR		Transmitter power supply.
TX2	6	O	TVDD	Transmitter output 2: transmits modulated 13.56 MHz energy carrier.
TVSS2	7	PWR		Transmitter ground.
AVDD	8	PWR		Analog power supply.
VMID	9	O	AVDD	Internally generated reference voltage to bias the receiving path
RX	10	I	AVDD	Receiver input.
AVSS	11	PWR		Analog ground.
AUX1	12	O	AVDD	Auxiliary output 1: analog and digital test signals.
AUX2	13	O	AVDD	Auxiliary output 2: analog and digital test signals.
OSCIN	14	I	AVDD	Crystal oscillator input: to oscillator inverting amplifier.
OSCOUT	15	O	AVDD	Crystal oscillator output: from oscillator inverting amplifier.
I0	16	I	DVDD	Host interface selector 0.
I1	17	I	DVDD	Host interface selector 1.
TESTEN	18	I	DVDD	Reserved for test: connect to ground for normal operation.
P35	19	IO	DVDD	General purpose IO.
N.C.	20			Not connected.
N.C.	21			Not connected.
N.C.	22			Not connected.
PVDD	23	PWR		Pad power supply.
P30 / UART_RX	24	IO	PVDD	General purpose IO / Debug UART receive input.
P70_IRQ	25	IO	PVDD	General purpose IO. Can be used as Interrupt request to host.
RSTOUT_N	26	O	PVDD	Reset indicator: when low, circuit is in reset state.
NSS / P50_SCL / HSU_RX	27	IO	PVDD	Host interface pin: SPI Not Slave Selected (NSS) or I^2C clock (SCL) or HSU receive (HSU_RX). Refer to Table 72 on page 48 for details.
MOSI / SDA / HSU_TX	28	IO	PVDD	Host interface pin: SPI Master Out Slave In (MOSI) or I^2C data (SDA) or HSU transmit (HSU_TX). Refer to Table 72 on page 48 for details.
MISO / P71	29	IO	PVDD	Host interface pin: SPI Master In Slave Out (MISO). Refer to Table 72 on page 48 for details. Can be used as general purpose IO.

Table 3. PN532 Pin description *...continued*

Symbol	Pin	Type	Ref Voltage	Description
SCK / P72	30	IO	PVDD	Host interface pin: SPI serial clock. Refer to Table 72 on page 48 for details. Can be used as general purpose IO.
P31 / UART_TX	31	IO	PVDD	General purpose IO/ Debug UART TX.
P32_INT0	32	IO	PVDD	General purpose IO / Interrupt source INT0.
P33_INT1	33	IO	PVDD	General purpose IO / Interrupt source INT1.
P34 / SIC_CLK	34	IO	SVDD	General purpose IO / Secure IC clock.
SIGOUT	35	O	SVDD	Contactless communication interface output: delivers a serial data stream according to NFCIP-1 to a secure IC.
SIGIN	36	I	SVDD	Contactless communication interface input: accepts a serial data stream according to NFCIP-1 and from a secure IC.
SVDD	37	O		Switchable output power for secure IC power supply with overload detection. Used as a reference voltage for secure IC communication.
RSTPD_N	38	I	PVDD	Reset and Power-Down: When low, internal current sources are switched off, the oscillator is disabled, and input pads are disconnected from the outside world. The internal reset phase starts on the negative edge on this pin.
DVDD	39	O		Internal digital power supply.
VBAT	40	PWR		Main external power supply.

8. Functional description

8.1 80C51

The PN532 is controlled via an embedded 80C51 microcontroller core (for more details http://www.standardics.nxp.com/support/documents/microcontrollers/?scope=80C51). Its principle features are listed below:

- 6-clock cycle CPU. One machine cycle comprises 6 clock cycles or states (S1 to S6). An instruction needs at least one machine cycle.
- ROM interface
- RAM interface to embedded IDATA and XRAM memories (see Figure 4 on page 11)
- Peripheral interface (PIF)
- Power control module to manage the CPU power consumption
- Clock module to control CPU clock during Shutdown and Wake-up modes
- Port module interface to configure I/O pads
- Interrupt controller
- Three timers
- Debug UART

The block diagram describes the main blocks described in this 80C51 section.

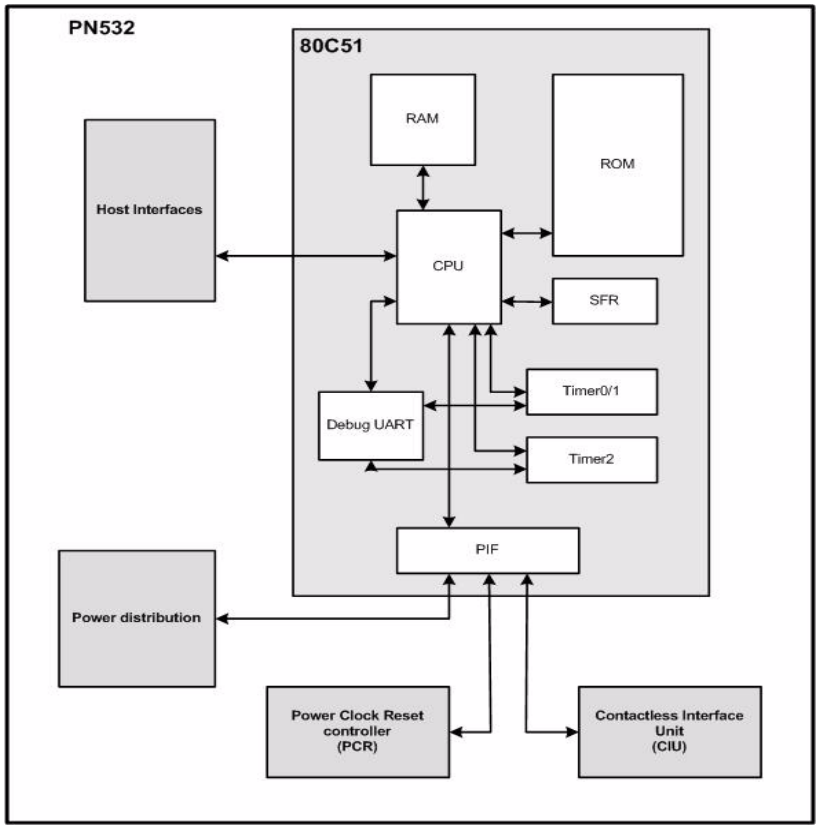

Fig 3. PN532 80C51 block description

8.1.1 PN532 memory map

The memory map of PN532 is composed of 2 main memory spaces: data memory and program memory. The following figure illustrates the structure.

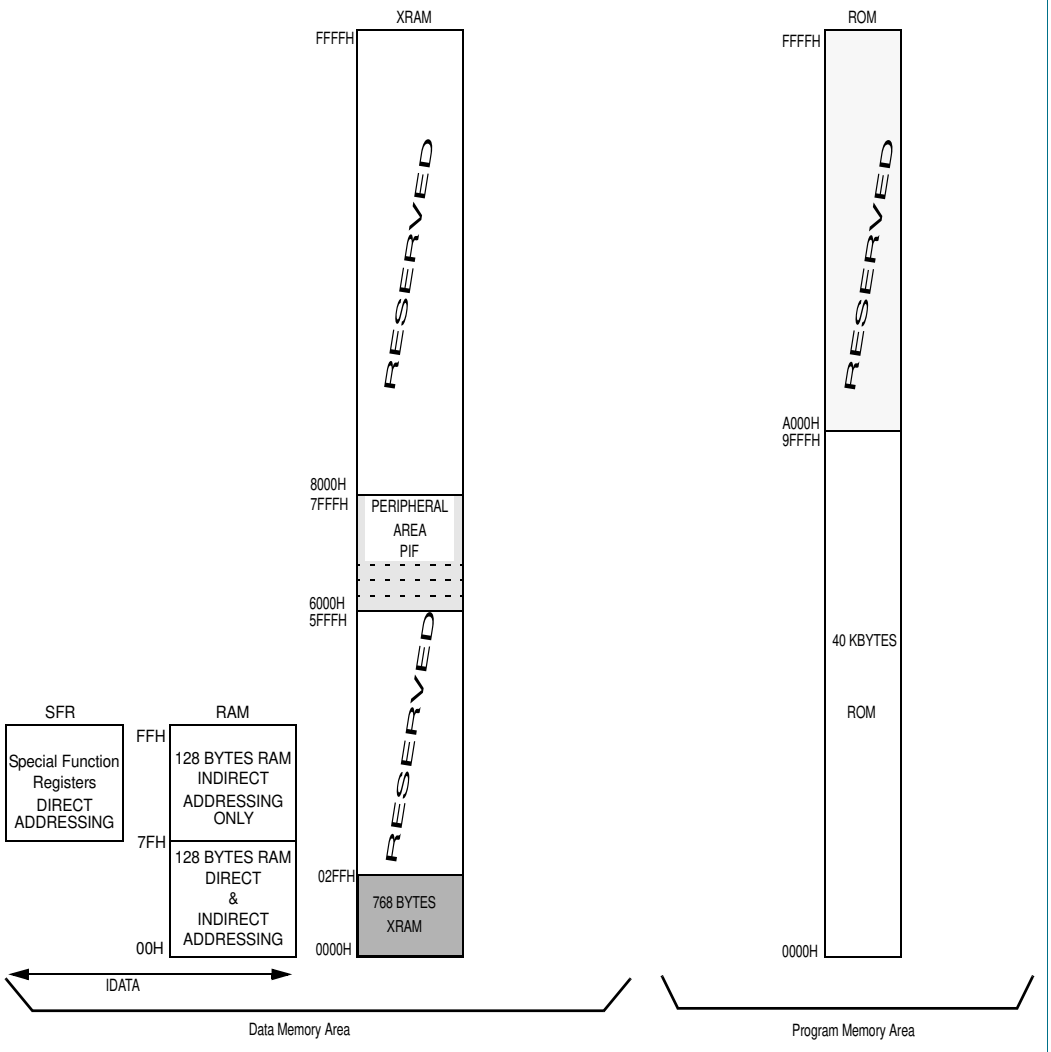

Fig 4. PN532 memory map overview

8.1.2 Data memory

Data memory is itself divided into 2 spaces:

- 384-byte IDATA with byte-wide addressing
  - 258-byte RAM
  - 128-byte SFR
- 1 bank of 64 KB extended RAM (XRAM) with 2-byte-wide addressing

8.1.2.1 IDATA memory

The IDATA memory is mapped into 3 blocks, which are referred as Lower IDATA RAM, Upper IDATA RAM, and SFR. Addresses to these blocks are byte-wide, which implies an address space of only 256 bytes. However, 384 bytes can be addressed within IDATA memory through the use of direct and indirect address mechanisms.

- Direct addressing: the operand is specified by an 8-bit address field in the instruction.
- Indirect addressing: the instruction specifies a register where the address of the operand is stored.

For the range 80h to FFh, direct addressing will access the SFR space; indirect addressing accesses Upper IDATA RAM. For the range 0h0 to 7Fh, Lower IDATA RAM is accessed, regardless of addressing mode. This behavior is summarized in the table below:

Table 4. IDATA memory addressing

Address	Addressing mode	
	Direct	**Indirect**
00h to 7Fh	Lower IDATA RAM	Lower IDATA RAM
80h to FFh	SFRs	Upper IDATA RAM

The SFRs and their addresses are described in the Table 5:

Table 5. SFR map of NFC controller

Address	Bit-addressable	Byte-addressable							Address
F8h	IP1		XRAMP		P3CFGA	P3CFGB			FFh
F0h	B				P7CFGA	P7CFGB		P7	F7h
E8h	IE1	CIU_Status2	CIU_FIFOData	CIU_FIFOLevel	CIU_WaterLevel	CIU_Control	CIU_BitFraming	CIU_Coll	EFh
E0h	ACC								E7h
D8h	I^2CC0N	I^2CSTA	I^2CDAT	I^2CADR				CIU_Status1	DFh
D0h	PSW	CIU_Command	CIU_CommIEn	CIU_DivIEn	CIU_CommIrq	CIU_DivIrq	CIU_Error		D7h
C8h	T2CON	T2MOD	RCAP2L	RCAP2H	T2L	T2H			CFh
C0h									C7h
B8h	IP0								BFh
B0h	P3								B7h
A8h	IE0	SPIcontrol	SPIstatus	HSU_STA	HSU_CTR	HSU_PRE	HSU_CNT		AFh
A0h		FITEN	FDATA	FSIZE					A7h
98h	S0CON	SBUF	RWL	TWL	FIFOFS	FIFOFF	SFF	FIT	9Fh
90h									97h
88h	T01CON	T01MOD	T0L	T1L	T0H	T1H			8Fh
80h		SP	DPL	DPH				PCON	87h

8.1.2.2 XRAM memory

The XRAM memory is divided into 2 memory spaces:

- 0000h to 5FFFh: reserved for addressing embedded RAM. For the PN532, only accesses between 0000h and 02FF are valid.
- 6000h to 7FFFh: reserved for addressing embedded peripherals. This space is divided into 32 regions of 256 bytes each. Addressing can be performed using R0 or R1 and the XRAMP SFR.

The Table 6 depicts the mapping of internal peripherals into XRAM.

Table 6. Peripheral mapping into XRAM memory space

Base Address	End Address	Description
6000h	60FFh	Reserved.
6100h	61FFh	IOs and miscellaneous registers configuration Refer to Section 8.2 “General purpose IOs configurations” on page 38
6200h	62FFh	Power Clock and Reset controller Refer to Section 8.5.7 “PCR extension registers” on page 93
6300h	633Fh	Contactless Unit Interface Refer to Section 8.6 “Contactless Interface Unit (CIU)” on page 99
6340h	FFFFh	Reserved

XRAM is accessed via the dedicated MOVX instructions. There are two access modes:

- 16-bit data pointer (DPTR): the full XRAM address space can be accessed.
- paging mechanism: the upper address byte is stored in the SFR register XRAMP; the lower byte is stored in either R1 or R0.

The Figure 5 illustrates both mechanisms.

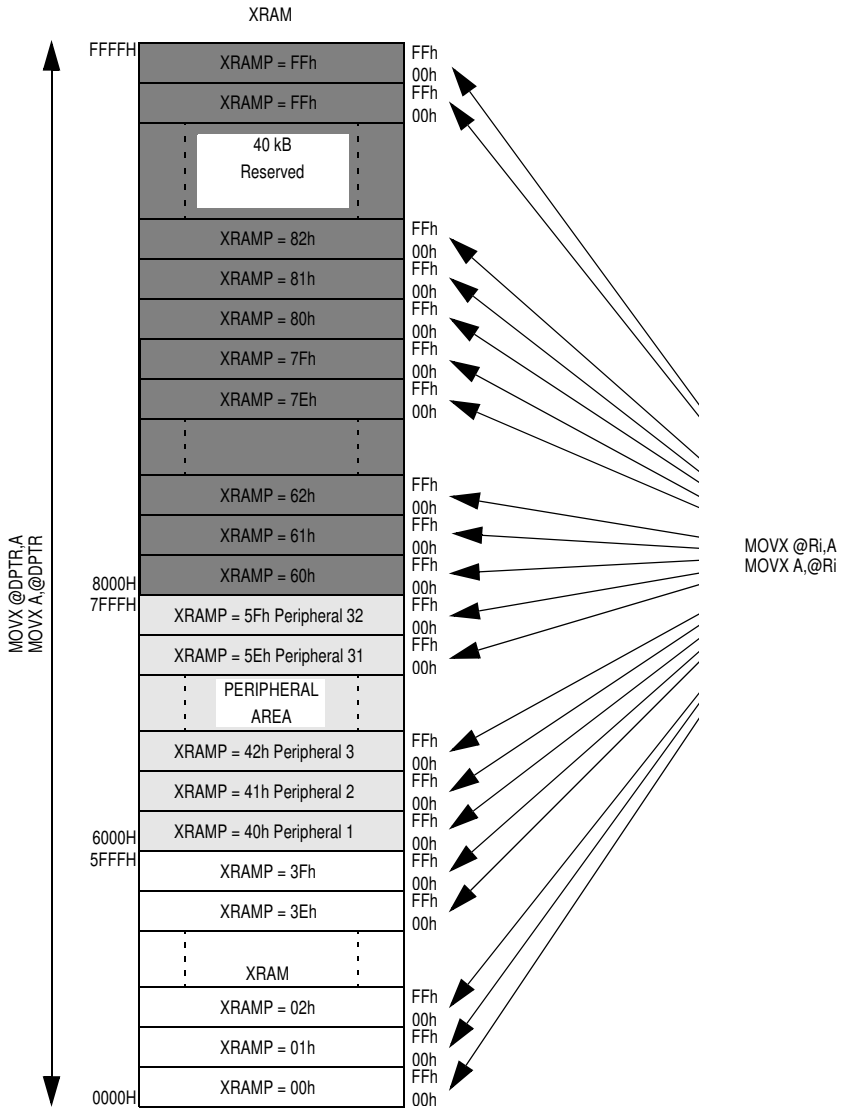

Fig 5. Indirect addressing of XRAM memory space

8.1.3 Program memory

PN532 program memory ranges from 0000h to 9FFFh, which is physically mapped to the 40 KB ROM.

8.1.4 PCON module

The Power Control (PCON) module is configured using the PCON SFR register.

Table 7. PCON register (SFR: address 87h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SMOD	-					CPU_PD	-
Reset	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R/W	R/W

Table 8. Description of PCON bits

Bit	Symbol	Description
7	SMOD	**Serial MODe:** When set to logic 1, the baud rate of the Debug UART is doubled
6 to 3	-	Reserved.
1	CPU_PD	**Power-down:** When set to logic 1, the microcontroller goes in Power-down mode
0	Reserved	**This bit should only ever contain logic 0.**

8.1.5 Interrupt Controller

The interrupt controller has the following features:

- 13 interrupt sources
- Interrupt enable registers IE0 and IE1
- Interrupt priority registers IP0 and IP1
- Wake-up from Power-Down state

8.1.5.1 Interrupt vectors

The mapping between interrupt sources and interrupt vectors is shown in Table 9.

Table 9. Interrupt vector

Interrupt number	Interrupt vector	Interrupt sources	Incremental priority level (conflict resolution level)
0	0003h	External P32_INT0	Highest
1	000Bh	Timer0 interrupt	
2	0013h	External P33_INT1	
3	001Bh	Timer1 interrupt	
4	0023h	Debug UART interrupt	
5	002Bh	Timer2 interrupt	
6	0033h	NFC-WI interrupt	
7	003Bh	LDO overcurrent interrupt	
8	0043h	Reserved	
9	004Bh	CIU interrupt 1	
10	0053h	CIU interrupt 0	
11	005Bh	I^2C interrupt	
12	0063h	SPI, FIFO, or HSU interrupts	
13	006Bh	Reserved	
14	0073h	General Purpose IRQ	Lowest

8.1.5.2 Interrupt enable: IE0 and IE1 registers

Each interrupt source can be individually enabled or disabled by setting a bit in IE0 or IE1. In register IE0, a global interrupt enable bit can be set to logic 0 to disable all interrupts at once.

The 2 following tables describe IE0.

Table 10. Interrupt controller IE0 register (SFR: address A8h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IE0_7	IE0_6	IE0_5	IE0_4	IE0_3	IE0_2	IE0_1	IE0_0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 11. Description of IE0 bits

Bit	Symbol	Description
7	IE0_7	**Global interrupt enable** When set to logic 1, the interrupts can be enabled. When set to logic 0, all the interrupts are disabled.
6	IE0_6	**NFC-WI counter interrupt enable** When set to logic 1, NFC-WI interrupt is enabled. See Table 164 on page 126.
5	IE0_5	**Timer2 interrupt enable** When set to logic 1, Timer2 interrupt is enabled. See Table 36 on page 28.
4	IE0_4	**Debug UART interrupt enable** When set to logic 1, Debug UART interrupt is enabled. See Table 49 on page 33.
3	IE0_3	**Timer1 interrupt enable** When set to logic 1, Timer1 interrupt is enabled. See Table 23 on page 23.
2	IE0_2	**P33_INT1 interrupt enable** When set to logic 1, P33_INT1 pin interrupt is enabled. See Table 23 on page 23. The polarity of P33_INT1 can be inverted (see Table 73 on page 49).
1	IE0_1	**Timer0 interrupt enable** When set to logic 1, Timer0 interrupt is enabled. See Table 23 on page 23.
0	IE0_0	**P32_INT0 interrupt enable** When set to logic 1, P32_INT0 pin interrupt is enabled. See Table 23 on page 23.

The 2 following tables describe IE1.

Table 12. Interrupt controller IE1 register (SFR: address E8h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IE1_7	-	IE1_5	IE1_4	IE1_3	IE1_2	-	IE1_0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 13. Description of IE1 bits

Bit	Symbol	Description
7	IE1_7	**General purpose IRQ interrupt enable**. When set to logic 1, enables interrupt function of P34, P35, P50_SCL and P71 according to their respective enable and level control bits. See Table 19 on page 20, Table 137 on page 95 and Table 143 on page 97.
6	-	Reserved. This bit must be set to logic 0
5	IE1_5	**FIFO, SPI and HSU interrupt enable**. When set to logic 1, enables FIFO interrupts, SPI interrupts, HSU interrupt. In HSU mode, the interrupt is when NSS is at logic 0. For the FIFO interrupts, see Table 112 on page 76. For the SPI interrupts, see Table 122 on page 81.
4	IE1_4	**I2C interrupt enable**. When set to logic 1, enables I^2C interrupt. See Table 77 on page 54.
3	IE1_3	**CIU interrupt 0 enable**. When set to logic 1, enables CIU interrupt 0: CIU_IRQ_0. See Table 190 on page 151.
2	IE1_2	**CIU interrupt 1 enable.** When set to logic 1, enables the CIU interrupt 1: CIU_IRQ_1. See Table 190 on page 151.
1	-	Reserved. This bit must be set to logic 0.
0	IE1_0	LDO overcurrent interrupt enable. When set to logic 1, enables the LDO overcurrent detection interrupt. See Table 127 on page 88.

8.1.5.3 Interrupt prioritization: IP0 and IP1 registers

Each interrupt source can be individually programmed to be one of two priority levels by setting or clearing a bit in the interrupt priority registers IP0 and IP1. If two interrupt requests of different priority levels are received simultaneously, the request with the high priority is serviced first. On the other hand, if the interrupts are of the same priority, precedence is resolved by comparing their respective conflict resolution levels (see Table 9 on page 16 for details). The processing of a low priority interrupt can be interrupted by one with a high priority.

A RETI (Return From Interrupt) instruction jumps to the address immediately succeeding the point at which the interrupt was serviced. The instruction found at the return address will be executed, prior to servicing any pending interrupts.

The 2 following tables describe IP0.

Table 14. Interrupt controller IP0 register (SFR: address B8h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IP0_7	IP0_6	IP0_5	IP0_4	IP0_3	IP0_2	IP0_1	IP0_0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 15. Description of IP0 bits

Bit	Symbol	Description
7	IP0_7	Reserved
6	IP0_6	When set to logic 1, NFC-WI interrupt is set to high priority.
5	IP0_5	When set to logic 1, Timer2 interrupt is set to high priority.
4	IP0_4	When set to logic 1, Debug UART interrupt is set to high priority.
3	IP0_3	When set to logic 1, Timer1 interrupt is set to high priority.
2	IP0_2	When set to logic 1, external P33_INT1 pin is set to high priority.
1	IP0_1	When set to logic 1, Timer0 interrupt is set to high priority.
0	IP0_0	When set to logic 1, external P32_INT0 pin is set to high priority.

The 2 following tables describe IP1.

Table 16. Interrupt controller IP1 register (SFR: address F8h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IP1_7	-	IP1_5	IP1_4	IP1_3	IP1_2	-	
Reset	0	0	0	0	0	0	00	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Table 17. Description of IP1 bits

Bit	Symbol	Description
7	IP1_7	When set to logic 1, General Purpose IRQ interrupt is set to high priority.
6	-	**Reserved. This bit must be set to logic 0.**
5	IP1_5	When set to logic 1, combined SPI, FIFO and HSU interrupt is set to high priority.
4	IP1_4	When set to logic 1, I^2C interrupt is set to high priority.
3	IP1_3	When set to logic 1, CIU interrupt 0 is set to high priority.
2	IP1_2	When set to logic 1, CIU interrupt 1 is set to high priority.
1	-	**Reserved. This bit must be set to logic 0.**
0	IP1_0	When set to logic 1, interrupt number 7 is set to high priority.

8.1.5.4 General purpose IRQ control

The general purpose interrupts are controlled by register GPIRQ.

NOTE: this is not a standard feature of the 8051.

Table 18. GPIRQ register (address 6107h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	gpirq_level_P71	gpirq_level_P50	gpirq_level_P35	gpirq_level_P34	gpirq_enable_P71	gpirq_enable_P50	gpirq_enable_P35	gpirq_enable_P34
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 19. Description of GPIRQ bits

Bit	Symbol	Description
7	gpirq_level_P71	**Configures the polarity of signal on P71 to generate a GPIRQ interrupt event (assuming gpirq_enable_P71 is set).** When set to logic 0, an interrupt will be generated if P71 is at logic 0. When set to logic 1, an interrupt will be generated if P71 is at logic 1.
6	gpirq_level_P50	**Configures the polarity of signal on P50 to generate a GPIRQ interrupt event (assuming gpirq_enable_P50 is set).** When set to logic 0, an interrupt will be generated if P50_SCL is at logic 0. When set to logic 1, an interrupt will be generated if P50_SCL is at logic 1.
5	gpirq_level_P35	**Configures the polarity of signal on P35 to generate a GPIRQ interrupt event (assuming gpirq_enable_P35 is set).** When set to logic 0, an interrupt will be generated if P35 is at logic 0. When set to logic 1, an interrupt will be generated if P35 is at logic 1.
4	gpirq_level_P34	**Configures the polarity of signal on P34 to generate a GPIRQ interrupt event (assuming gpirq_enable_P34 is set).** When set to logic 0, an interrupt will be generated if P34 is at logic 0. When set to logic 1, an interrupt will be generated if P34 is at logic 1. **Remark:** If hide_svdd_sig of the register control_rngpower is set and gpirq_enable_P34 is also set then this bit will be asserted independently of the level on the pad P34.
3	gpirq_enable_P71	When set to logic 1, enables pad P71 to generate a GPIRQ interrupt event.[1]
2	gpirq_enable_P50	When set to logic 1, enables pad P50_SCL to generate a GPIRQ interrupt event.[1]
1	gpirq_enable_P35	When set to logic 1, enables pad P35 to generate a GPIRQ interrupt event.[1]
0	gpirq_enable_P34	When set to logic 1, enables pad P34 to generate a GPIRQ interrupt event.[1]

[1] The bit IE1_7 of register IE1 (see Table 13 on page 18) has also to be set to logic 1 to enable the corresponding CPU interrupt.

8.1.6 Timer0/1 description

Timer0/1 are general purpose timer/counters. Timer0/1 has the following functionality:

- Configurable edge or level detection interrupts
- Timer or counter operation
- 4 timer/counter modes
- Baud rate generation for Debug UART

Timer0/1 comprises two 16-bit timer/counters: Timer0 and Timer1. Both can be configured as either a timer or an event counter.

Each of the timers can operate in one of four modes:

- Mode 0: 13-bit timer/counter
- Mode 1: 16-bit timer/counter
- Mode 2: 8-bit timer/counter with programmable preload value
- Mode 3: two individual 8-bit timer/counters (Timer0 only)

In the ‘timer’ function, the timer/counter is incremented every machine cycle. The count rate is 1/6 of the CPU clock frequency (CPU_CLK).

In the ‘counter’ function, the timer/counter is incremented in response to a 1-to-0 transition on the input pins P34 / SIC_CLK (Timer0) or P35 (Timer1). In this mode, the external input is sampled during state S5 of every machine cycle. If the associated pin is at logic 1 for a machine cycle, followed by logic 0 on the next machine cycle, the count is incremented. The new count value appears in the timer/counter in state S3 of the machine cycle following the one in which the transition was detected. The maximum count rate is 1/12 of the CPU_CLK frequency. There are no restrictions on the duty cycle of the external input signal but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

The overflow output ‘t1_ovf’ of Timer1 can be used as a baud rate generator for the Debug UART. The Timer1 interrupt should be disabled in this case. For most applications which drive the Debug UART, Timer1 is configured for ‘timer’ operation and in auto-reload mode.

8.1.6.1 Timer0/1 registers

The Timer0/1 module contains six Special Function Registers (SFRs) which can be accessed by the CPU.

Table 20. Timer0/1 Special Function registers list

Name	Size [bytes]	Address Offset	Description	Access
T01CON	1	88h	Timer0/1 control register	R/W
T01MOD	1	89h	Timer0/1 mode register	R/W
T0L	1	8Ah	Timer0 timer/counter lower byte	R/W
T1L	1	8Bh	Timer1 timer/counter lower byte	R/W
T0H	1	8Ch	Timer0 timer/counter upper byte	R/W
T1H	1	8Dh	Timer1 timer/counter upper byte	R/W

The firmware performs a register read in state S5 and a register write in state S6. The hardware loads bits TF0 and TF1 of the register T01CON during state S2 and state S4 respectively. The hardware loads bits IE0 and IE1 of the register T01CON during state S1 and reset these bits during state S2. The registers T0L, T0H, T1L, T1H are updated by the hardware during states S1, S2, S3 and S4 respectively. At the end of a machine cycle, the firmware load has overridden the hardware load as the firmware writes in state S6.

Table 21. Timer0/1 SFR registers CPU state access

		CPU STATE					
Register	**Bit**	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**
T01CON	TF0		HW read			SW read	SW write
	TF1				HW read	SW read	SW write
	IE0 / IE1	HW write	HW reset			SW read	SW write
TOL		HW write				SW read	SW write
TOH			HW write			SW read	SW write
T1L				HW write		SW read	SW write
T1H					HW write	SW read	SW write

8.1.6.2 T01CON register

The register is used to control Timer0/1 and report its status.

Table 22. Timer0/1 T01CON register (SFR address 88h), bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 23. Description of Timer0/1 T01CON register bits

Bit	Symbol	Description
7	TF1	**Timer1 overflow.** Set to logic 1 by hardware on a Timer1 overflow. The flag is set to logic 0 by the CPU after 2 machine cycles. The bit IE0_3 of register IE0 (see Table 11 on page 17) has to be set to logic 1 to enable the corresponding CPU interrupt.
6	TR1	**Timer1 run control**. Set by firmware only. When set to logic 1, Timer1 is enabled.
5	TF0	**Timer0 overflow**. Set by hardware on a Timer0 overflow. The flag is set to logic 0 by the CPU after 2 machine cycles. The bit IE0_1 of register IE0 (see Table 11 on page 17) has to be set to logic 1 to enable the corresponding CPU interrupt.
4	TR0	**Timer0 run control**. Set by firmware only. When set to logic 1, Timer0 is enabled.
3	IE1	**External Interrupt1 event**. Set to logic 1 by hardware when an external interrupt is detected on P33_INT1. The bit IE0_2 of register IE0 (see Table 11 on page 17) has to be set to logic 1 to enable the corresponding CPU interrupt.
2	IT1	**External Interrupt1 control**. Set by firmware only. When set to logic 1, Interrupt1 triggers on a falling edge of P33_INT1. When set to logic 0, Interrupt1 triggers on a low level of P33_INT1.
1	IE0	**External Interrupt0 event**. Set to logic 1 by hardware when an external interrupt is detected on P32_INT0. The bit IE0_0 of register IE0 (see Table 11 on page 17) has to be set to logic 1 to enable the corresponding CPU interrupt.
0	IT0	**External Interrupt0 control**. Set by firmware only. When set to logic 1, Interrupt0 triggered by a falling edge on P32_INT0. When set to logic 0, Interrupt0 triggered by a low level on P32_INT0.

8.1.6.3 T01MOD register

This register is used to configure Timer0/1.

Table 24. Timer 0/1 T01MOD register (SFR address 89h), bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	GATE1	C/T1	M11	M10	GATE0	C/T0	M01	M00
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 25. Description of T01MOD bits

Bit	Symbol	Description
7	GATE1	**Timer1 gate control.** Set by firmware only. When set to logic 1, Timer1 is enabled only when P33_INT1 is high and bit TR1 of register T01CON is set. When set to logic 0, Timer1 is enabled.
6	C/T1	**Timer1 timer/counter selector.** Set by firmware only. When set to logic 1, Timer1 is set to counter operation. When set to logic 0, Timer1 is set to timer operation.
5 to 4	M[11:10]	**Timer1 mode.** Set by firmware only. • Mode 0: M11 = 0 and M10 = 0 – 8192 counter – T1L serves as a 5-bit prescaler • Mode 1: M11 = 0 and M10 = 1 – 16-bit timer/counter – T1H and T1L are cascaded • Mode 2: M11 = 1 and M10 = 0 – 8-bit auto-reload timer/counter. – T1H stores value to be reloaded into T1L each time T1L overflows. • Mode 3: M11 = 1 and M10 = 1 – Timer1 is stopped (count frozen).

Table 25. Description of T01MOD bits *…continued*

Bit	Symbol	Description
3	GATE0	**Timer0 gate control.** Set by firmware only. When set to logic 1, Timer0 is enabled only when P32_INT0 is high and bit TR0 of register T01CON is set. When set to logic 0, Timer0 is enabled.
2	C/T0	**Timer0 timer/counter selector.** Set by firmware only. When set to logic 1, Timer0 is set to counter operation. When set to logic 0, Timer0 is set to timer operation.
1 to 0	M[01:00]	**Timer0 mode.** Set by firmware only. • Mode 0: M01 = 0 and M00 = 0 – 8192 timer – T0L acts as a 5-bit prescaler. • Mode 1: M01 = 0 and M00 = 1 – 16-bit timer/counter – T0H and T0L are cascaded. • Mode 2: M01 = 1 and M00 = 0 – 8-bit auto-reload timer/counter – T0H stores value to be reloaded into T0L each time T0L overflows. • Mode 3: M01 = 1 and M00 = 1 – Timer0 split into two 8-bit timer/counters T0H and T0L – T0H is controlled by the control bit of Timer1: bit TR1 of register T01CON – T0L is controlled by standard Timer0 control: “{P32_INT0 OR (NOT GATE0)} AND bit TR0”.

8.1.6.4 T0L and T0H registers

These are the actual timer/counter bytes for Timer0: T0L is the lower byte; T0H is the upper byte.

Table 26. Timer0/1 T0L register (SFR address 8Ah), bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	T0L.7	T0L.6	T0L.5	T0L.4	T0L.3	T0L.2	T0L.1	T0L.0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 27. Description of T0L bits

Bit	Symbol	Description
7:0	T0L.7 to T0L.0	Timer0 timer/counter lower byte

Table 28. Timer0/1 T0H register (SFR address 8Ch), bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	T0H.7	T0H.6	T0H.5	T0H.4	T0H.3	T0H.2	T0H.1	T0H.0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 29. Description of T0H bits

Bit	Symbol	Description
7 to 0	T0H.7 to T0H.0	Timer0 timer/counter upper byte