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PN7120

NFC controller with integrated firmware, supporting all NFC Forum modes

Rev. 3.5 — 11 June 2018
312435

Product data sheet
COMPANY PUBLIC

1 Introduction

This document describes the functionality and electrical specification of the NFC Controller PN7120.

Additional documents describing the product functionality further are available for design-in support. Refer to the references listed in this document to get access to the full for full documentation provided by NXP.

In this document the term „MIFARE Classic card“ refers to a MIFARE Classic IC-based contactless card.

2 General description

PN7120, the best plug'n play full NFC solution - easy integration into any OS environment, with integrated firmware and NCI interface designed for contactless communication at 13.56 MHz.

It is the ideal solution for rapidly integrating NFC technology in any application, especially those running OS environment like Linux and Android, reducing Bill of Material (BOM) size and cost, thanks to:

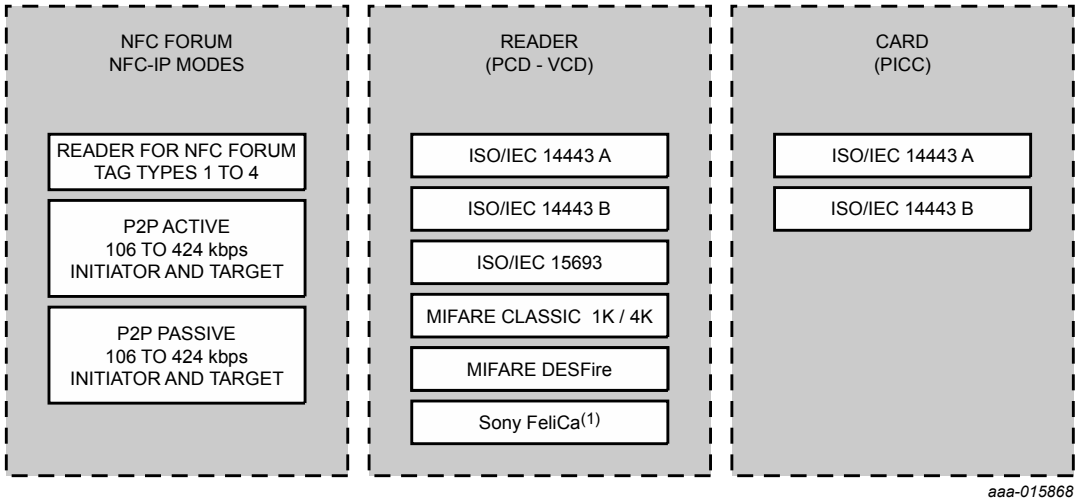
- full NFC forum compliancy (see [11]) with small form factor antenna
- embedded NFC firmware providing all NFC protocols as pre-integrated feature
- direct connection to the main host or microcontroller, by I^2C-bus physical and NCI protocol
- ultra-low power consumption in polling loop mode
- Highly efficient integrated power management unit (PMU) allowing direct supply from a battery

PN7120 embeds a new generation RF contactless front-end supporting various transmission modes according to NFCIP-1 and NFCIP-2, ISO/IEC 14443, ISO/IEC 15693, ISO/IEC 18000-3, MIFARE Classic IC-based card and FeliCa card specifications. It embeds an ARM Cortex-M0 microcontroller core loaded with the integrated firmware supporting the NCI 1.0 host communication.

The contactless front-end design brings a major performance step-up with on one hand a higher sensitivity and on the other hand the capability to work in active load modulation communication enabling the support of small antenna form factor

Supported transmission modes are listed in Figure 1. For contactless card functionality, the PN7120 can act autonomously if previously configured by the host in such a manner.

PN7120 integrated firmware provides an easy integration and validation cycle as all the NFC real-time constraints, protocols and device discovery (polling loop) are being taken care internally. In few NCI commands, host SW can configure the PN7120 to notify for card or peer detection and start communicating with them.



1. According to ISO/IEC 18092 (Ecma 340) standard.

Figure 1. PN7120 transmission modes

3 Features and benefits

- Includes NXP ISO/IEC 14443-A and Innovatron ISO/IEC 14443-B intellectual property licensing rights
- ARM Cortex-M0 microcontroller core
- Highly integrated demodulator and decoder
- Buffered output drivers to connect an antenna with minimum number of external components
- Integrated RF level detector
- Integrated Polling Loop for automatic device discovery
- RF protocols supported
  - NFCIP-1, NFCIP-2 protocol (see [7] and [10])
  - ISO/IEC 14443A, ISO/IEC 14443B PICC mode via host interface (see[2])
  - ISO/IEC 14443A, ISO/IEC 14443B PCD designed according to NFC Forum digital protocol T4T platform and ISO-DEP (see [11])
  - FeliCa PCD mode
  - MIFARE Classic PCD encryption mechanism (MIFARE Classic 1K/4K)
  - NFC Forum tag 1 to 4 (MIFARE Ultralight, Jewel, Open FeliCa tag, MIFARE DESFire) (see [11])
  - ISO/IEC 15693/ICODE VCD mode (see [8])
- Supported host interfaces
  - NCI protocol interface according to NFC Forum standardization (see [1])
  - I^2C-bus High-speed mode (see[3])
- Integrated power management unit
  - Direct connection to a battery (2.3 V to 5.5 V voltage supply range)
  - Support different Hard Power-Down/Standby states activated by firmware
  - Autonomous mode when host is shut down
- Automatic wake-up via RF field, internal timer and I^2C-bus interface
- Integrated non-volatile memory to store data and executable code for customization

4 Applications

- All devices requiring NFC functionality especially those running in an Android or Linux environment
- TVs, set-top boxes, Blu-ray decoders, audio devices
- Home automation, gateways, wireless routers
- Home appliances
- Wearables, remote controls, healthcare, fitness
- Printers, IP phones, gaming consoles, accessories

5 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	Card Emulation and Passive Target; V_{SS} = 0 V [1] [2]	2.3	-	5.5	V
		Reader, Active Initiator and Active Target; V_{SS} = 0 V [1] [2]	2.7	-	5.5	V
V_{DD}	supply voltage	internal supply voltage	1.65	1.8	1.95	V
$V_{DD(PAD)}$	$V_{DD(PAD)}$ supply voltage	supply voltage for host interface				
		1.8 V host supply; V_{SS} = 0 V [1]	1.65	1.8	1.95	V
		3.3 V host supply; V_{SS} = 0 V [1]	3.0	-	3.6	V
I_{BAT}	battery supply current	in Hard Power Down state; V_{BAT} = 3.6 V; T = 25 °C	-	10	12	µA
		in Standby state; V_{BAT} = 3.6 V; T = 25 °C	-	-	20	µA
		in Monitor state; V_{BAT} = 2.75 V; T = 25 °C	-	-	12	µA
		in low-power polling loop; V_{BAT} = 3.6 V; T = 25 °C; loop time = 500 ms	-	150	-	µA
		PCD mode at typical 3 V [3]	-	-	170	mA
$I_{O(VDDPAD)}$	output current on pin $V_{DD(PAD)}$	total current which can be pulled on $V_{DD(PAD)}$ referenced outputs	-	-	15	mA
$I_{th(Ilim)}$	current limit threshold current	current limiter on $V_{DD(TX)}$ pin; $V_{DD(TX)}$ = 3.1 V [3][4]	-	180	-	mA
P_{tot}	total power dissipation	Reader; $I_{VDD(TX)}$ = 100 mA; V_{BAT} = 5.5 V	-	-	0.5	W
T_{amb}	ambient temperature	JEDEC PCB-0.5	-30	+25	+85	°C

[1] V_{SS} represents V_{SS}, V_{SS1}, V_{SS2}, V_{SS3}, V_{SS4}, $V_{SS(PAD)}$ and $V_{SS(TX)}$.
[2] The antenna should be tuned not to exceed this current limit (the detuning effect when coupling with another device must be taken into account).
[3] The antenna shall be tuned not to exceed the maximum of I_{VBAT}.
[4] This is the threshold of a built-in protection done to limit the current out of $V_{DD(TX)}$ in case of any issue at antenna pins to avoid burning the device. It is not allowed in operational mode to have $I_{VDD(TX)}$ such that I_{VBAT} maximum value is exceeded.

6 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN7120A0EV/C1xxxx	VFBGA49	plastic very thin fine-pitch ball grid array package; 49 balls	SOT1320-1

7 Marking

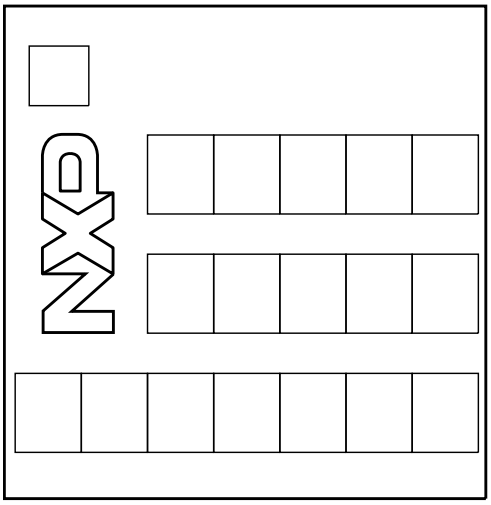


Figure 2. PN7120 package marking (top view)

Table 3. Marking code

Line number	Marking code
Line 1	product version identification
Line 2	diffusion batch sequence number
Line 3	manufacturing code including: • diffusion center code: – N: TSMC – s: Global Foundry • assembly center code: – S: APK – X: ASEN • RoHS compliancy indicator: – D: Dark Green; fully compliant RoHS and no halogen and antimony • manufacturing year and week, 3 digits: – Y: year – WW: week code • product life cycle status code: – X: means not qualified product – nothing means released product

8 Block diagram

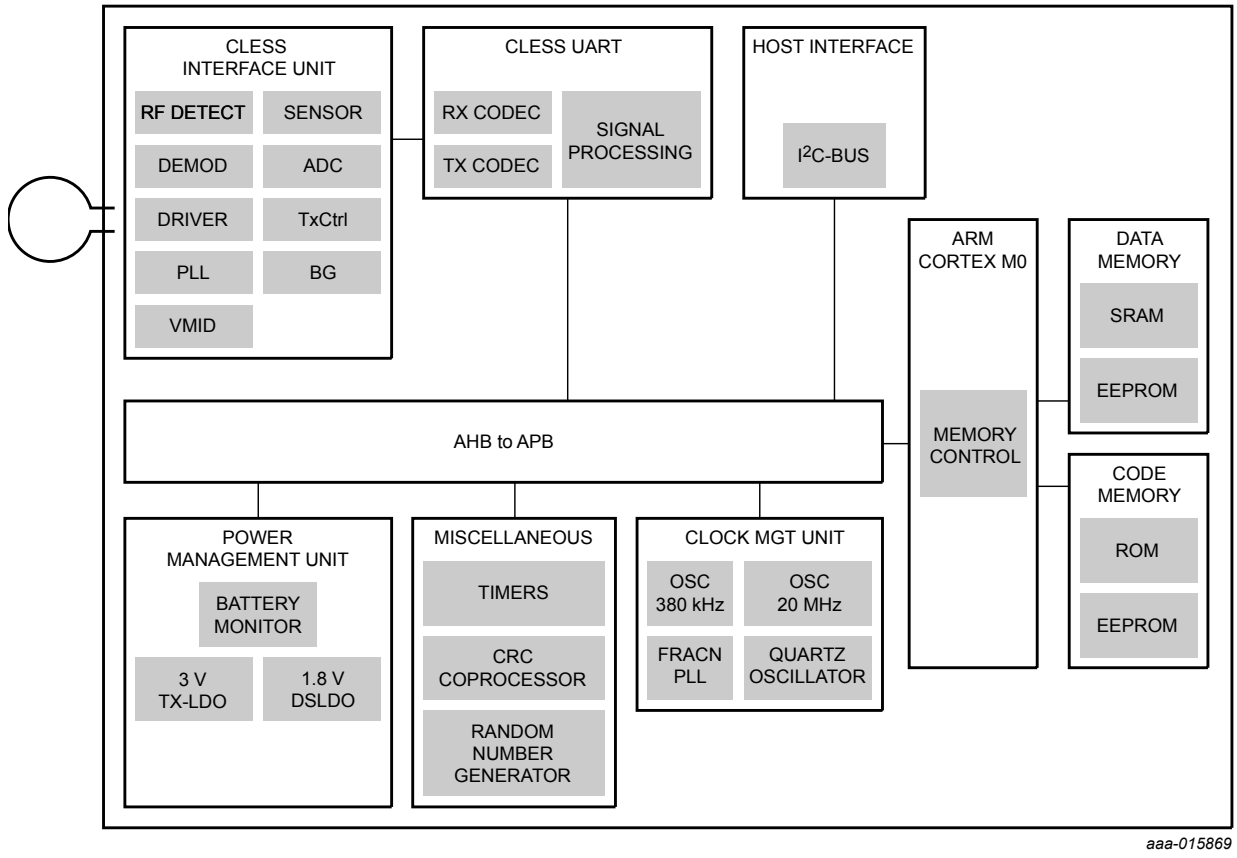


Figure 3. PN7120 block diagram

9 Pinning information

9.1 Pinning

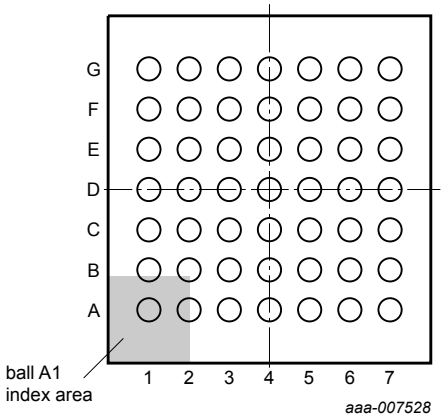


Figure 4. PN7120 pinning (bottom view)

Table 4. PN7120 pin description

Symbol	Pin	Type[1]	Refer	Description
i.c.	A1	-	-	internally connected; must be connected to ground
CLK_REQ	A2	O	$V_{DD(PAD)}$	clock request pin
XTAL1	A3	I	V_{DD}	PLL clock input. Oscillator input
i.c.	A4	-	-	internally connected; leave open
i.c.	A5	-	-	internally connected; leave open
i.c.	A6	-	-	internally connected; leave open
i.c.	A7	-	-	internally connected; leave open
I2CSCL	B1	I	$V_{DD(PAD)}$	I^2C-bus serial clock input
I2CADR0	B2	I	$V_{DD(PAD)}$	I^2C-bus address bit 0 input
i.c.	B3	-	-	internally connected; leave open
i.c.	B4	-	-	internally connected; leave open
i.c.	B5	-	-	internally connected; must be connected to ground
V_{SS1}	B6	G	n/a	ground
i.c.	B7	-	-	internally connected; leave open
I2CSDA	C1	I/O	$V_{DD(PAD)}$	I^2C-bus serial data
$V_{SS(PAD)}$	C2	G	n/a	pad ground
XTAL2	C3	O	V_{DD}	oscillator output
V_{SS}	C4	G	n/a	ground
n.c.	C5	-	-	not connected

Symbol	Pin	Type[1]	Refer	Description
V_{DD}	C6	P	n/a	LDO output supply voltage
V_{BAT}	C7	P	n/a	battery supply voltage
IRQ	D1	O	$V_{DD(PAD)}$	interrupt request output
BOOST_CTRL	D2	O	$V_{DD(PAD)}$	booster control, see [5]
$V_{DD(PAD)}$	D3	P	n/a	pad supply voltage
V_{SS2}	D4	G	n/a	ground
i.c.	D5	-	-	internally connected; leave open
V_{SS3}	D6	G	n/a	ground
i.c.	D7	-	-	internally connected; leave open
VEN	E1	I	V_{BAT}	reset pin. Set the device in Hard Power Down
$V_{SS(DC\_DC)}$	E2	G	n/a	ground
n.c.	E3	-	-	not connected
n.c.	E4	-	-	not connected
n.c.	E5	-	-	not connected
n.c.	E6	-	-	not connected
$V_{DD(TX)}$	E7	P	n/a	contactless transmitter output supply voltage for decoupling
i.c.	F1	-	-	internally connected; leave open
i.c.	F2	-	-	internally connected; leave open
V_{SS4}	F3	G	n/a	ground
i.c.	F4	-	-	internally connected; leave open
RXN	F5	I	V_{DD}	negative receiver input
RXP	F6	I	V_{DD}	positive receiver input
$V_{DD(MID)}$	F7	P	n/a	receiver reference input supply voltage
V_{BAT2}	G1	P	n/a	battery supply voltage; must be connected to V_{BAT}
V_{BAT1}	G2	P	n/a	battery supply voltage; must be connected to V_{BAT}
TX1	G3	O	$V_{DD(TX)}$	antenna driver output
$V_{SS(TX)}$	G4	G	n/a	contactless transmitter ground
TX2	G5	O	$V_{DD(TX)}$	antenna driver output
ANT2	G6	P	n/a	antenna connection for Listen mode
ANT1	G7	P	n/a	antenna connection for Listen mode

[1] P = power supply; G = ground; I = input, O = output; I/O = input/output.

10 Functional description

PN7120 can be connected on a host controller through I^2C-bus. The logical interface towards the host baseband is NCI-compliant [1] with additional command set for NXP-specific product features. This IC is fully user controllable by the firmware interface described in [4].

Moreover, PN7120 provides flexible and integrated power management unit in order to preserve energy supporting Power Off mode.

In the following chapters you will find also more details about PN7120 with references to very useful application note such as:

- PN7120 User Manual ([4]):
  User Manual describes the software interfaces (API) based on the NFC forum NCI standard. It does give full description of all the NXP NCI extensions coming in addition to NCI standard ([1]).
- PN7120 Hardware Design Guide ([5]):
  Hardware Design Guide provides an overview on the different hardware design options offered by the IC and provides guidelines on how to select the most appropriate ones for a given implementation. In particular, this document highlights the different chip power states and how to operate them in order to minimize the average NFC-related power consumption so to enhance the battery lifetime.
- PN7120 Antenna and Tuning Design Guide ([6]):
  Antenna and Tuning Design Guide provides some guidelines regarding the way to design an NFC antenna for the PN7120 chip.
  It also explains how to determine the tuning/matching network to place between this antenna and the PN7120.
  Standalone antenna performances evaluation and final RF system validation (PN7120 + tuning/matching network + NFC antenna within its final environment) are also covered by this document.
- PN7120 Low-Power Mode Configuration ([9]):
  Low-Power Mode Configuration documentation provides guidance on how PN7120 can be configured in order to reduce current consumption by using Low-power polling mode.

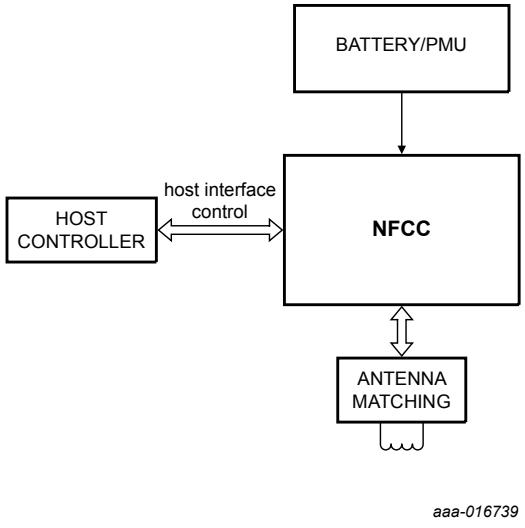


Figure 5. PN7120 connection

10.1 System modes

10.1.1 System power modes

PN7120 is designed in order to enable the different power modes from the system.

2 power modes are specified: Full power mode and Power Off mode.

Table 5. System power modes description

System power mode	Description
Full power mode	the main supply (V_{BAT}) as well as the host interface supply ($V_{DD(PAD)}$) is available, all use cases can be executed
Power Off mode	the system is kept Hard Power Down (HPD)

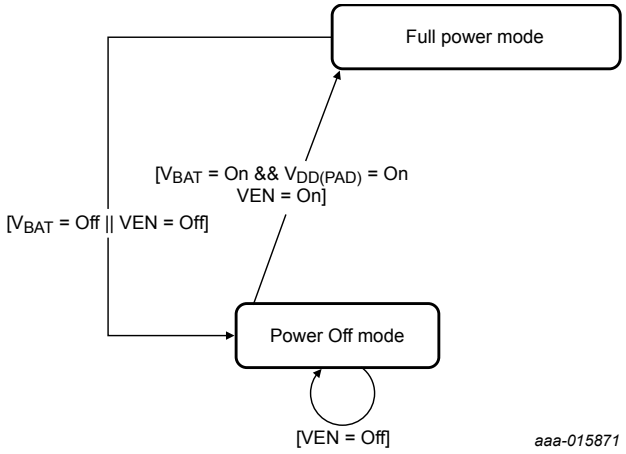


Figure 6. System power mode diagram

Table 6 summarizes the system power mode of the PN7120 depending on the status of the external supplies available in the system:

Table 6. System power modes configuration

V_{BAT}	VEN	Power mode
Off	X	Power Off mode
On	Off	Power Off mode
On	On	Full power mode

Depending on power modes, some application states are limited:

Table 7. System power modes description

System power mode	Allowed communication modes
Power Off mode	no communication mode available
Full power mode	Reader/Writer, Card Emulation, P2P modes

10.1.2 PN7120 power states

Next to system power modes defined by the status of the power supplies, the power states include the logical status of the system thus extend the power modes.

4 power states are specified: Monitor, Hard Power Down (HPD), Standby, Active.

Table 8. PN7120 power states

Power state name	Description
Monitor	The PN7120 is supplied by V_{BAT} which voltage is below its programmable critical level, VEN voltage > 1.1 V and the Monitor state is enabled. The system power mode is Power Off mode.
Hard Power Down	The PN7120 is supplied by V_{BAT} which voltage is above its programmable critical level when Monitor state is enabled and PN7120 is kept in Hard Power Down (VEN voltage is kept low by host or SW programming) to have the minimum power consumption. The system power mode is in Power Off.
Standby	The PN7120 is supplied by V_{BAT} which voltage is above its programmable critical level when the Monitor state is enabled, VEN voltage is high (by host or SW programming) and minimum part of PN7120 is kept supplied to enable configured wake-up sources which allow to switch to Active state; RF field, Host interface. The system power mode is Full power mode.
Active	The PN7120 is supplied by V_{BAT} which voltage is above its programmable critical level when Monitor state is enabled, VEN voltage is high (by host or SW programming) and the PN7120 internal blocks are supplied. 3 functional modes are defined: Idle, Listener and Poller. The system power mode is Full power mode.

At application level, the PN7120 will continuously switch between different states to optimize the current consumption (polling loop mode). Refer to Table 1 for targeted current consumption in here described states.

The PN7120 is designed to allow the host controller to have full control over its functional states, thus of the power consumption of the PN7120 based NFC solution and possibility to restrict parts of the PN7120 functionality.

10.1.2.1 Monitor state

In Monitor state, the PN7120 will exit it only if the battery voltage recovers over the critical level. Battery voltage monitor thresholds show hysteresis behavior as defined in Table 26.

PN7120 will autonomously shut-down internal PMU supply to protect the battery from deep discharge.

10.1.2.2 Hard Power Down (HPD) state

The Hard Power Down state is entered when $V_{DD(PAD)}$ and V_{BAT} are high by setting VEN voltage < 0.4 V. As these signals are under host control, the PN7120 has no influence on entering or exiting this state.

10.1.2.3 Standby state

Active state is PN7120's default state after boot sequence in order to allow a quick configuration of PN7120. It is recommended to change the default state to Standby state after first boot in order to save power. PN7120 can switch to Standby state autonomously (if configured by host).

In this state PN7120 most blocks including CPU are no more supplied. Number of wake-up sources exist to put PN7120 into Active state:

- I^2C-bus interface wake-up event
- Antenna RF level detector
- Internal timer event when using polling loop (380 kHz Low-power oscillator is enabled)

If wake-up event occurs, PN7120 will switch to Active state. Any further operation depends on software configuration and/or wake-up source.

10.1.2.4 Active state

Within the Active state, the system is acting as an NFC device. The device can be in 3 different functional modes: Idle, Poller and Target.

Table 9. Functional modes in active state

Functional modes	Description
Idle	the PN7120 is active and host interface communication is on going. The RF interface is not activated. If Standby state is de-activated PN7120 stays in Idle mode even when no host communication.
Listener	the PN7120 is active and is listening to external device. The RF interface is activated.
Poller	the PN7120 is active and is in Poller mode. It polls external device. The RF interface is activated.

Poller mode:

In this mode, PN7120 is acting as Reader/Writer or NFC Initiator, searching for or communicating with passive tags or NFC target. Once RF communication has ended, PN7120 will switch to Idle mode or Standby state to save energy. Poller mode shall be used with 2.7 V < V_{BAT} < 5.5 V and VEN voltage > 1.1 V. Poller mode shall not be used with V_{BAT} < 2.7 V. PV_{DD} is within its operational range (see Table 1).

Listener mode:

In this mode, PN7120 is acting as a card or as an NFC Target. Listener mode shall be used with 2.3 V < V_{BAT} < 5.5 V and VEN voltage > 1.1 V. Once RF communication has ended, PN7120 will switch to Idle mode or Standby state to save energy.

10.1.2.5 Polling loop

The polling loop will sequentially set PN7120 in different power states (Active or Standby). All RF technologies supported by PN7120 can be independently enabled within this polling loop.

There are 2 main phases in the polling loop:

- Listening phase. The PN7120 can be in Standby power state or Listener mode
- Polling phase. The PN7120 is in Poller mode

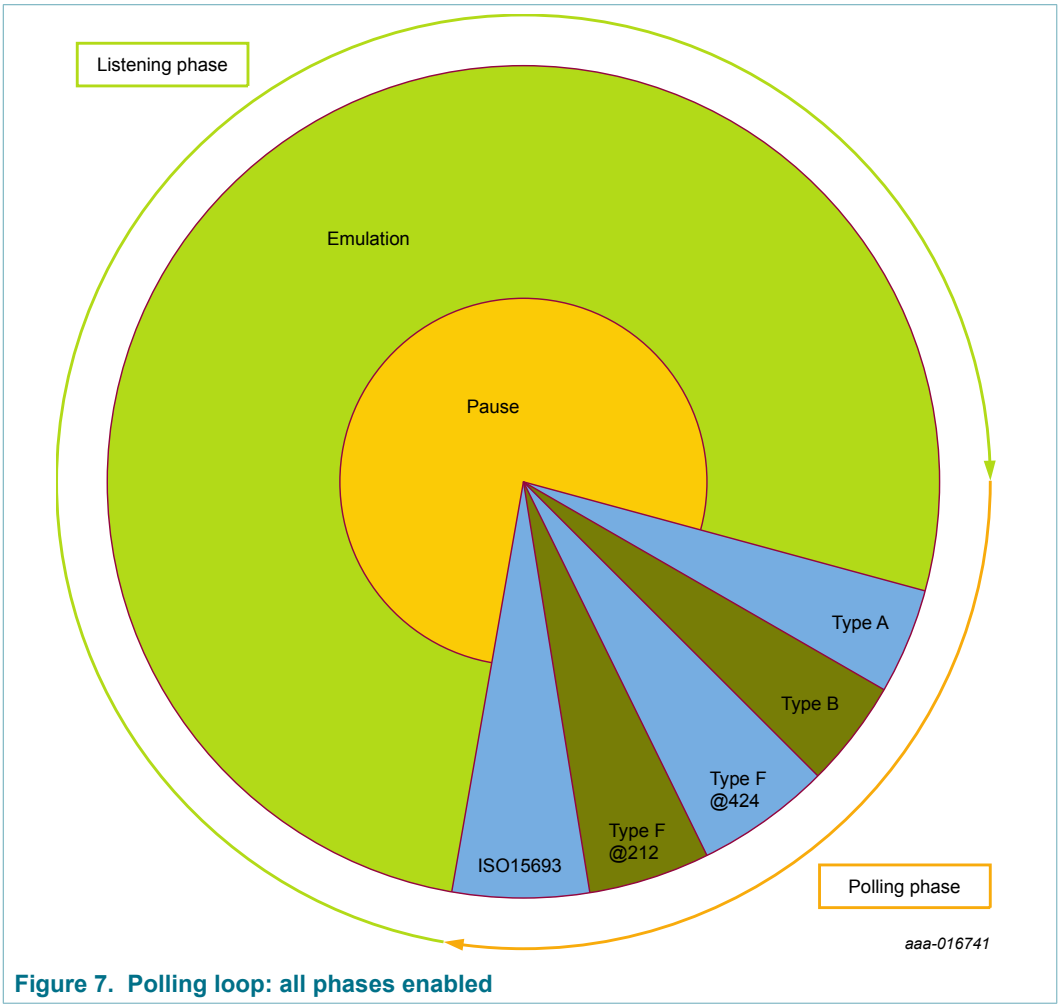


Figure 7. Polling loop: all phases enabled

Listening phase uses Standby power state (when no RF field) and PN7120 goes to Listener mode when RF field is detected. When in Polling phase, PN7120 goes to Poller mode.

To further decrease the power consumption when running the polling loop, PN7120 features a low-power RF polling. When PN7120 is in Polling phase instead of sending regularly RF command PN7120 senses with a short RF field duration if there is any NFC Target or card/tag present. If yes, then it goes back to standard polling loop. With 500 ms (configurable duration, see [4]) listening phase duration, the average power consumption is around 150 µA.

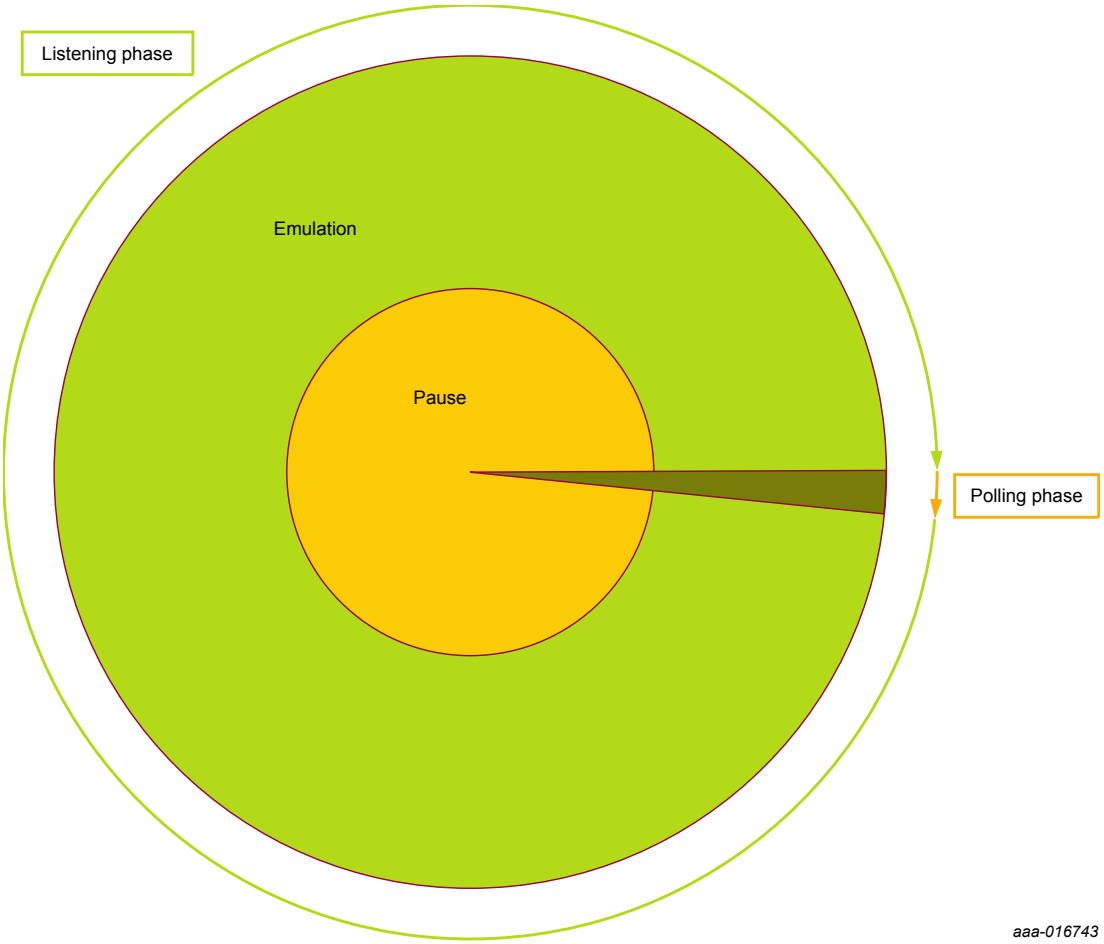


Figure 8. Polling loop: low-power RF polling

Detailed description of polling loop configuration options is given in [4].

10.2 Microcontroller

PN7120 is controlled via an embedded ARM Cortex-M0 microcontroller core.

PN7120 features integrated in firmware are referenced in [4]

10.3 Host interfaces

PN7120 provides the support of an I^2C-bus Slave Interface, up to 3.4 MBaud.

The host interface is waken-up on I^2C-bus address.

To enable and ensure data flow control between PN7120 and host controller, additionally a dedicated interrupt line IRQ is provided which Active state is programmable. See [4] for more information.

10.3.1 I²C-bus interface

The I²C-bus interface implements a slave I²C-bus interface with integrated shift register, shift timing generation and slave address recognition.

I²C-bus Standard mode (100 kHz SCL), Fast mode (400 kHz SCL) and High-speed mode (3.4 MHz SCL) are supported.

The mains hardware characteristics of the I²C-bus module are:

- Support slave I²C-bus
- Standard, Fast and High-speed modes supported
- Wake-up of PN7120 on its address only
- Serial clock synchronization can be used by PN7120 as a handshake mechanism to suspend and resume serial transfer (clock stretching)

The I²C-bus interface module meets the I²C-bus specification [3] except General call, 10-bit addressing and Fast mode Plus (Fm+).

10.3.1.1 I²C-bus configuration

The I²C-bus interface shares four pins with I²C-bus interface also supported by PN7120. When I²C-bus is configured in EEPROM settings, functionality of interface pins changes to one described in Table 10.

Table 10. Functionality for I²C-bus interface

Pin name	Functionality
I2CADR0	I²C-bus address 0
I2CSDA	I²C-bus data line
I2CSCL	I²C-bus clock line

PN7120 supports 7-bit addressing mode. Selection of the I²C-bus address is done by 2-pin configurations on top of a fixed binary header: 0, 1, 0, 1, 0, 0, I2CADR0, R/W.

Table 11. I²C-bus interface addressing

I2CADR0	I²C-bus address (R/W = 0, write)	I²C-bus address (R/W = 1, read)
0	0x50	0x51
1	0x52	0x53

10.4 PN7120 clock concept

There are 4 different clock sources in PN7120:

- 27.12 MHz clock coming either/or from:
  - Internal oscillator for 27.12 MHz crystal connection
  - Integrated PLL unit which includes a 1 GHz VCO
- 13.56 MHz RF clock recovered from RF field
- Low-power oscillator 20 MHz
- Low-power oscillator 380 kHz

10.4.1 27.12 MHz quartz oscillator

When enabled, the 27.12 MHz quartz oscillator applied to PN7120 is the time reference for the RF front end when PN7120 is behaving in Reader mode or NFCIP-1 initiator.

Therefore stability of the clock frequency is an important factor for reliable operation. It is recommended to adopt the circuit shown in Figure 9.

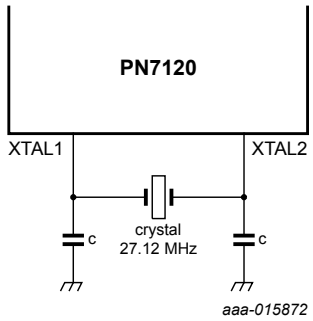


Figure 9. 27.12 MHz crystal oscillator connection

Table 12 describes the levels of accuracy and stability required on the crystal.

Table 12. Crystal requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{xtal}	crystal frequency	ISO/IEC and FCC compliancy	-	27.12	-	MHz
Δf_{xtal}	crystal frequency accuracy	full operating range [1]	-100	-	+100	ppm
		all V_{BAT} range; T = 20 °C [1]	-50	-	+50	ppm
		all temperature range; V_{BAT} = 3.6 V [1]	-50	-	+50	ppm
ESR	equivalent series resistance		-	50	100	Ω
C_L	load capacitance		-	10	-	pF
$P_{o(xtal)}$	crystal output power		-	-	100	µW

[1] This requirement is according to FCC regulations requirements. To meet only ISO/IEC 14443 and ISO/IEC 18092, then ± 14 kHz apply.

10.4.2 Integrated PLL to make use of external clock

When enabled, the PLL is designed to generate a low noise 27.12 MHz for an input clock 13 MHz, 19.2 MHz, 24 MHz, 26 MHz, 38.4 MHz and 52 MHz.

The 27.12 MHz of the PLL is used as the time reference for the RF front end when PN7120 is behaving in Reader mode or NFC Initiator as well as in NFC Target when configured in Active communication mode.

The input clock on XTAL1 shall comply with the.following phase noise requirements for the following input frequency: 13 MHz, 19.2 MHz, 24 MHz, 26 MHz, 38.4 MHz and 52 MHz:

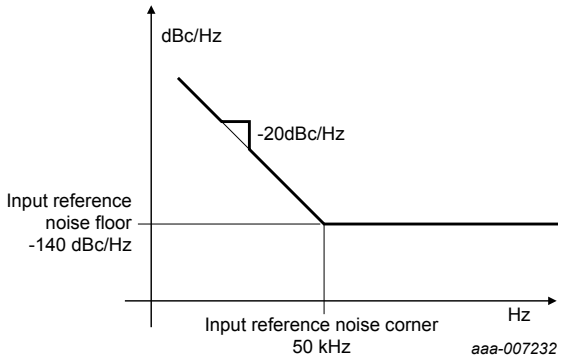


Figure 10. Input reference phase noise characteristics

This phase noise is equivalent to an RMS jitter of 6.23 ps from 10 Hz to 1 MHz. For configuration of input frequency, refer to [8]. There are 6 pre programmed and validated frequencies for the PLL: 13 MHz, 19.2 MHz, 24 MHz, 26 MHz, 38.4 MHz and 52 MHz.

Table 13. PLL input requirements

Coupling: single-ended, AC coupling;

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	ISO/IEC and FCC compliancy	-	13	-	MHz
			-	19.2	-	MHz
			-	24	-	MHz
			-	26	-	MHz
			-	38.4	-	MHz
			-	52	-	MHz
$f_{i(ref)acc}$	reference input frequency accuracy	full operating range; frequencies typical values: 13 MHz, 26 MHz and 52 MHz [1]	-25	-	+25	ppm
		full operating range; frequencies typical values: 19.2 MHz, 24 MHz and 38.4 MHz [1]	-50	-	+50	ppm
φ_n	phase noise	input noise floor at 50 kHz	-140	-	-	dB/Hz
Sinusoidal shape						
$V_{i(p-p)}$	peak-to-peak input voltage		0.2	-	1.8	V
$V_{i(clk)}$	clock input voltage		0	-	1.8	V
Square shape						
$V_{i(clk)}$	clock input voltage		0	-	1.8 ± 10 %	V

[1] This requirement is according to FCC regulations requirements. To meet only ISO/IEC 14443 and ISO/IEC 18092, then ± 400 ppm limits apply.

For detailed description of clock request mechanisms, refer to [4] and [5].

10.4.3 Low-power 20 MHz oscillator

Low-power 20 MHz oscillator is used as system clock of the system.

10.4.4 Low-power 380 kHz oscillator

A Low Frequency Oscillator (LFO) is implemented to drive a counter (WUC) waking-up PN7120 from Standby state. This allows implementation of low-power reader polling loop at application level. Moreover, this 380 kHz is used as the reference clock for write access to EEPROM memory.

10.5 Power concept

10.5.1 PMU functional description

The Power Management Unit of PN7120 generates internal supplies required by PN7120 out of V_{BAT} input supply voltage:

- V_{DD}: internal supply voltage
- $V_{DD(TX)}$: output supply voltage for the RF transmitter

The Figure 11 describes the main blocks available in PMU:

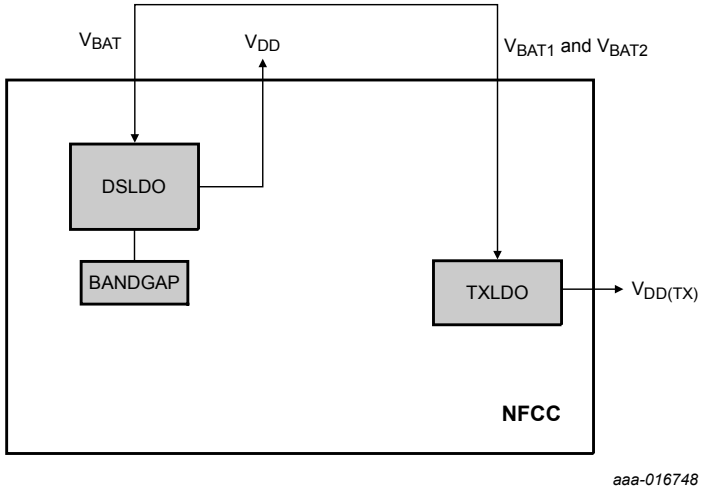


Figure 11. PMU functional diagram

10.5.2 DSLDO: Dual Supply LDO

The input pin of the DSLDO is V_{BAT}.

The Low drop-out regulator provides V_{DD} required in PN7120.

10.5.3 TXLDO

This is the LDO which generates the transmitter voltage.

The value of $V_{DD(TX)}$ is configured at 3.1 V ± 0.2 V.

$V_{DD(TX)}$ value is given according to the minimum targeted V_{BAT} value for which Reader mode shall work.

For V_{BAT} above 3.1 V, $V_{DD(TX)}$ = 3.1 V:

$$V_{BAT} \geq 3.1V \Rightarrow V_{DD(TX)} = 3.1V$$

$$3.1V > V_{BAT} \geq 2.3V \Rightarrow V_{DD(TX)} = V_{BAT}$$

In Standby state, $V_{DD(TX)}$ is around 2.5 V with some ripples; it toggles between 2.35 V to 2.65 V with a period which depends on the capacitance and load on $V_{DD(TX)}$.

Figure 12 shows $V_{DD(TX)}$ behavior for 3.1 V:

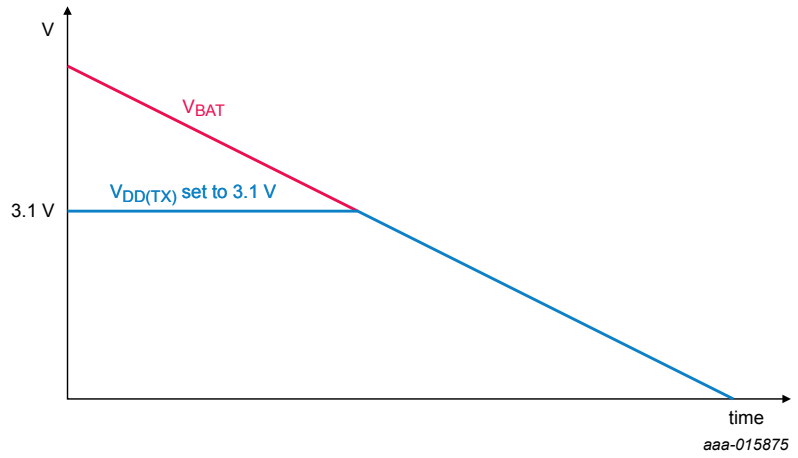


Figure 12. $V_{DD(TX)}$ offset disabled behavior

Figure 13 shows the case where the PN7120 is in Standby state:

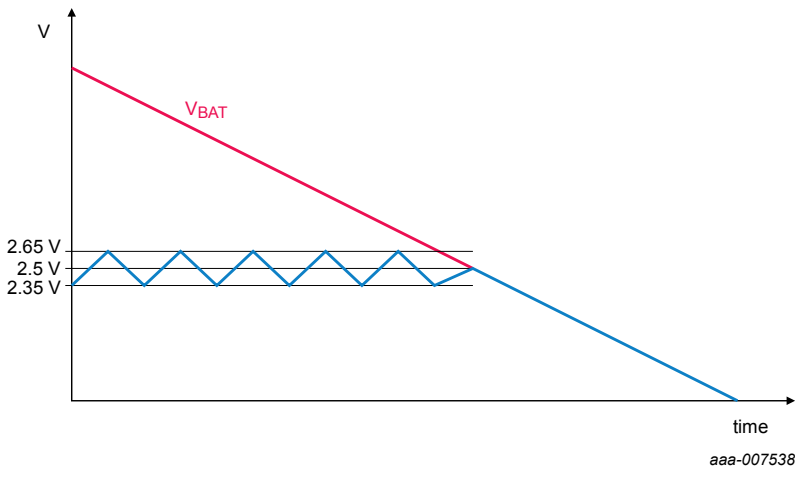


Figure 13. $V_{DD(TX)}$ behavior when PN7120 is in Standby state

10.5.3.1 TXLDO limiter

The TXLDO includes a current limiter to avoid too high current within TX1, TX2 when in reader or initiator modes.

The current limiter block compares an image of the TXLDO output current to a reference. Once the reference is reached, the output current gets limited which is equivalent to a typical output current of 220 mA whatever V_{BAT} = 2.7 V and 180 mA for V_{BAT} = 3.1 V.

10.5.4 Battery voltage monitor

The PN7120 features low-power V_{BAT} voltage monitor which protects the host device battery from being discharged below critical levels. When V_{BAT} voltage goes below $V_{BATcritical}$ threshold, then the PN7120 goes in Monitor state. Refer to Figure 14 for principle schematic of the battery monitor.

The battery voltage monitor is enabled via an EEPROM setting.

The $V_{BATcritical}$ threshold can be configured to 2.3 V or 2.75 V by an EEPROM setting.

At the first start-up, V_{BAT} voltage monitor functionality is OFF and then enabled if properly configured in EEPROM. The PN7120 monitors battery voltage continuously.

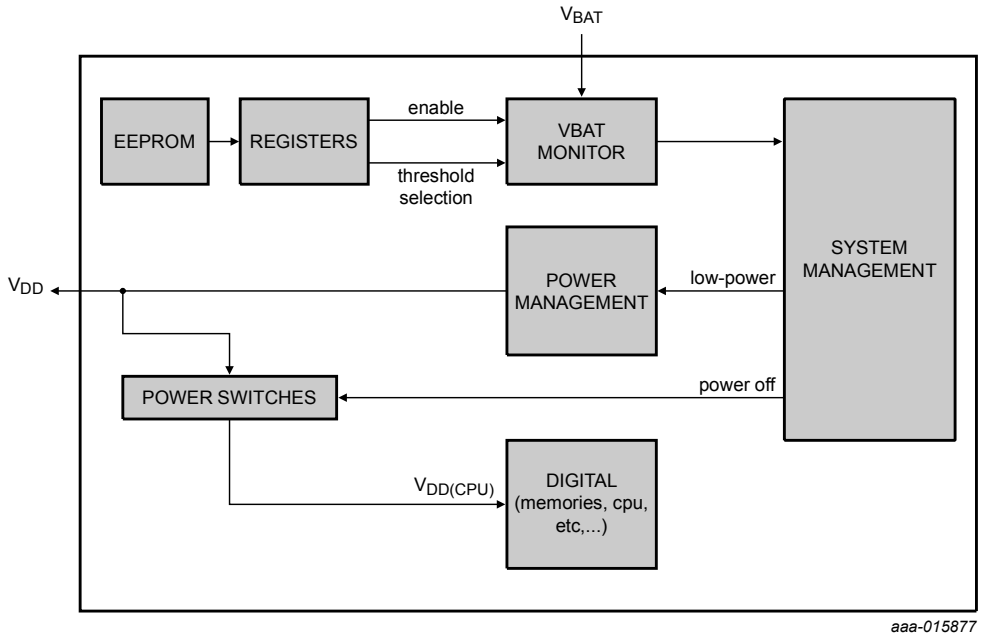


Figure 14. Battery voltage monitor principle

The value of the critical level can be configured to 2.3 V or 2.75 V by an EEPROM setting. This value has a typical hysteresis around 150 mV.

10.6 Reset concept

10.6.1 Resetting PN7120

To enter reset there are 2 ways:

- Pulling VEN voltage low (Hard Power Down state)
- if V_{BAT} monitor is enabled: lowering V_{BAT} below the monitor threshold (Monitor state, if VEN voltage is kept above 1.1 V)

Reset means resetting the embedded FW execution and the registers values to their default values. Part of these default values is defined from EEPROM data loaded values, others are hardware defined. See [4] to know which ones are accessible to tune PN7120 to the application environment.

To get out of reset:

- Pulling VEN voltage high with V_{BAT} above V_{BAT} monitor threshold if enabled

Figure 15 shows reset done via VEN pin.

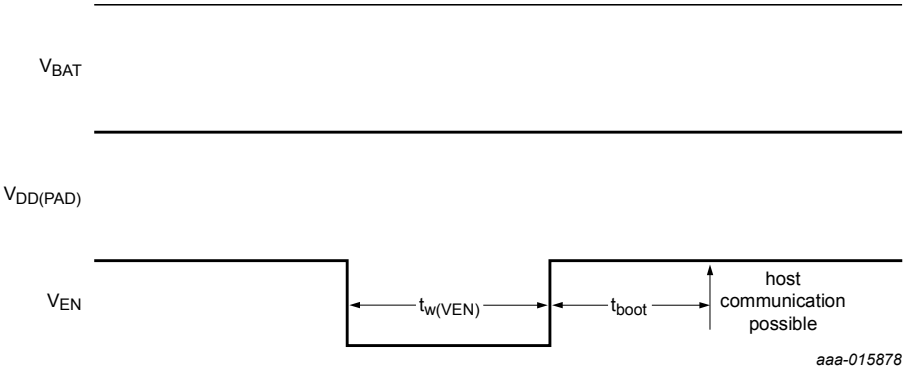


Figure 15. Resetting PN7120 via VEN pin

See Section 15.3.2 for the timings values.

10.6.2 Power-up sequences

There are 2 different supplies for PN7120. PN7120 allows these supplies to be set up independently, therefore different power-up sequences have to be considered.

10.6.2.1 V_{BAT} is set up before $V_{DD(PAD)}$

This is at least the case when V_{BAT} pin is directly connected to the battery and when PN7120 V_{BAT} is always supplied as soon the system is supplied.

As VEN pin is referred to V_{BAT} pin, VEN voltage shall go high after V_{BAT} has been set.

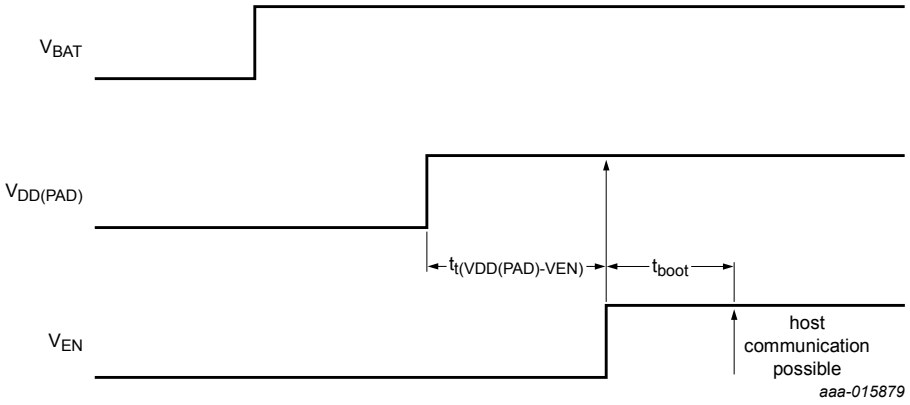


Figure 16. V_{BAT} is set up before $V_{DD(PAD)}$

See Section 15.2.3 for the timings values.

10.6.2.2 $V_{DD(PAD)}$ and V_{BAT} are set up in the same time

It is at least the case when V_{BAT} pin is connected to a PMU/regulator which also supply $V_{DD(PAD)}$.

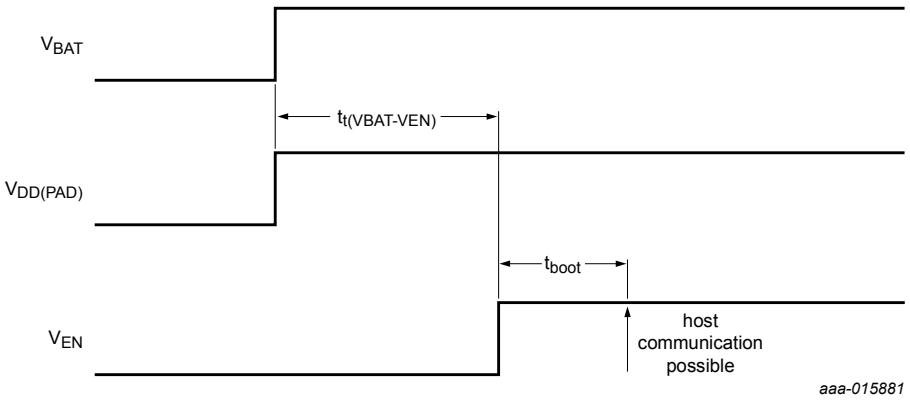


Figure 17. $V_{DD(PAD)}$ and V_{BAT} are set up in the same time

See Section 15.2.3 for the timings values.

10.6.2.3 PN7120 has been enabled before $V_{DD(PAD)}$ is set up or before $V_{DD(PAD)}$ has been cut off

This can be the case when V_{BAT} pin is directly connected to the battery and when $V_{DD(PAD)}$ is generated from a PMU. When the battery voltage is too low, then the PMU might no more be able to generate $V_{DD(PAD)}$. When the device gets charged again, then $V_{DD(PAD)}$ is set up again.

As the pins to select the interface are biased from $V_{DD(PAD)}$, when $V_{DD(PAD)}$ disappears the pins might not be correctly biased internally and the information might be lost. Therefore it is required to make the IC boot after $V_{DD(PAD)}$ is set up again.

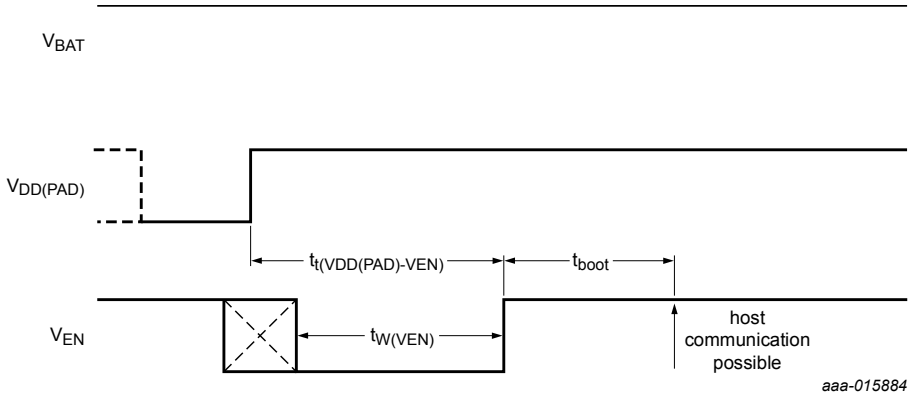


Figure 18. $V_{DD(PAD)}$ is set up or cut-off after PN7120 has been enabled

See Section 15.2.3 for the timings values.

10.6.3 Power-down sequence

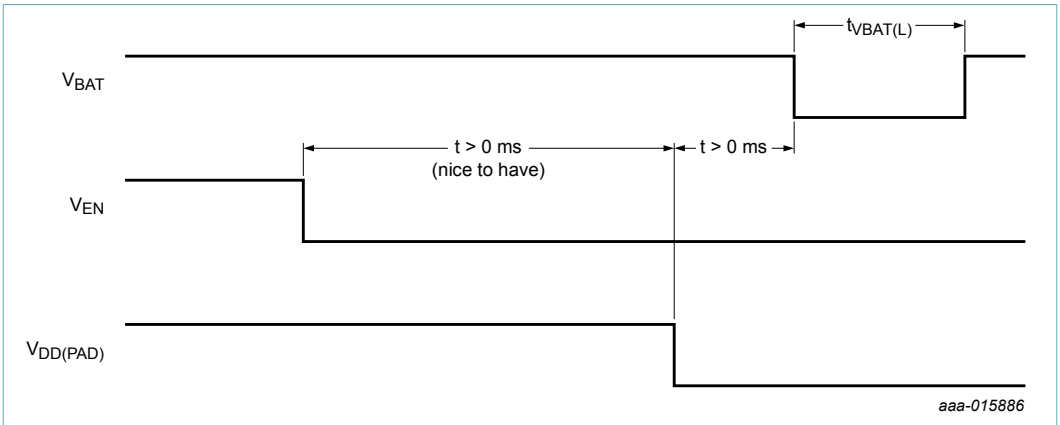


Figure 19. PN7120 power-down sequence

10.7 Contactless Interface Unit

PN7120 supports various communication modes at different transfer speeds and modulation schemes. The following chapters give more detailed overview of selected communication modes.

Remark: all indicated modulation index and modes in this chapter are system parameters. This means that beside the IC settings a suitable antenna tuning is required to achieve the optimum performance.

10.7.1 Reader/Writer communication modes

Generally 5 Reader/Writer communication modes are supported:

- PCD Reader/Writer for ISO/IEC 14443 type A and for MIFARE Classic
- PCD Reader/Writer for Jewel/Topaz
- PCD Reader/Writer for FeliCa
- PCD Reader/Writer for ISO/IEC 14443B