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PN7150

High performance NFC controller with integrated firmware, supporting all NFC Forum modes

Rev. 3.7 — 24 April 2018
317437

Product data sheet
COMPANY PUBLIC

1 Introduction

This document describes the functionality and electrical specification of the NFC Controller PN7150.

Additional documents describing the product functionality further are available for design-in support. Refer to the references listed in this document to get access to the full documentation provided by NXP.

2 General description

Best plug´n play and high-performance full NFC solution PN7150 is a full NFC controller solution with integrated firmware and NCI interface designed for contactless communication at 13.56 MHz. It is compatible with NFC forum requirements.

PN7150 is designed based on learnings from previous NXP NFC device generation. It is the ideal solution for rapidly integrating NFC technology in any application, especially those running O/S environment like Linux and Android, reducing Bill of Material (BOM) size and cost, thanks to:

- Full NFC forum compliancy (see [1]) with small form factor antenna
- Embedded NFC firmware providing all NFC protocols as pre-integrated feature
- Direct connection to the main host or microcontroller, by I^2C-bus physical and NCI protocol
- Ultra-low power consumption in polling loop mode
- Highly efficient integrated power management unit (PMU) allowing direct supply from a battery

PN7150 embeds a new generation RF contactless front-end supporting various transmission modes according to NFCIP-1 and NFCIP-2, ISO/IEC 14443, ISO/IEC 15693, MIFARE Classic IC-based card and FeliCa card specifications. It embeds an ARM Cortex-M0 microcontroller core loaded with the integrated firmware supporting the NCI 1.0 host communication. It also allows to provide a higher output power by supplying the transmitter output stage from 3.0 V to 4.75 V.

The contactless front-end design brings a major performance step-up with on one hand a higher sensitivity and on the other hand the capability to work in active load modulation communication enabling the support of small antenna form factor.

Supported transmission modes are listed in Figure 1. For contactless card functionality, the PN7150 can act autonomously if previously configured by the host in such a manner.

PN7150 integrated firmware provides an easy integration and validation cycle as all the NFC real-time constraints, protocols and device discovery (polling loop) are being taken care internally. In few NCI commands, host SW can configure the PN7150 to notify for card or peer detection and start communicating with them.

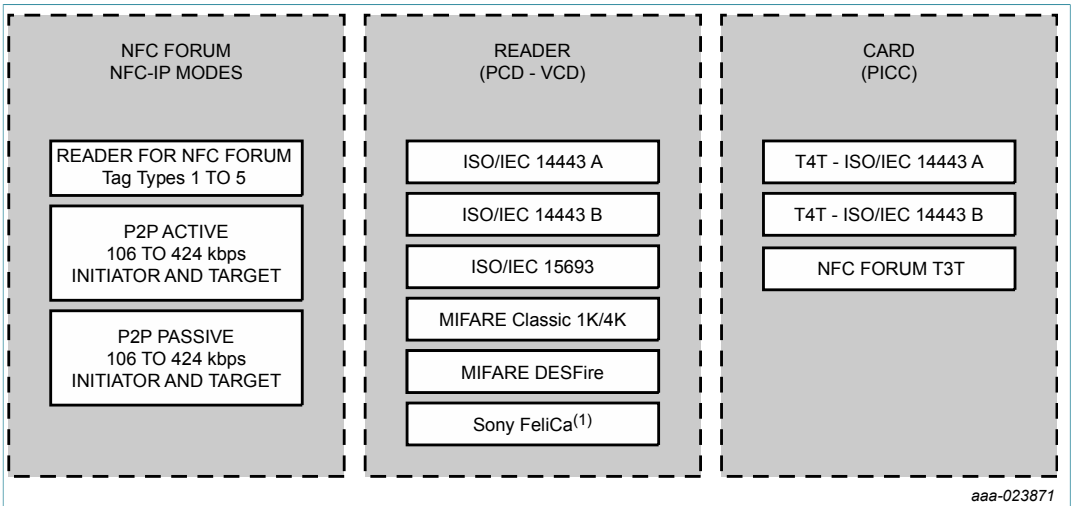

Figure 1. PN7150 transmission modes

1. According to ISO/IEC 18092 (Ecma 340) standard.

3 Features and benefits

- Includes NXP ISO/IEC14443-A and Innovatron ISO/IEC14443-B intellectual property licensing rights
- ARM Cortex-M0 microcontroller core
- Highly integrated demodulator and decoder
- Buffered output drivers to connect an antenna with minimum number of external components
- Integrated RF level detector
- Integrated Polling Loop for automatic device discovery
- RF protocols supported
  - NFCIP-1, NFCIP-2 protocol (see [8] and [11])
  - ISO/IEC 14443A, ISO/IEC 14443B PICC, NFC Forum T4T modes via host interface (see [3])
  - NFC Forum T3T via host interface
  - ISO/IEC 14443A, ISO/IEC 14443B PCD designed according to NFC Forum digital protocol T4T platform and ISO-DEP (see [1])
  - FeliCa PCD mode
  - MIFARE Classic PCD encryption mechanism (MIFARE Classic 1K/4K)
  - NFC Forum tag 1 to 5 (MIFARE Ultralight, Jewel, Open FeliCa tag, MIFARE DESFire) (see [1])
  - ISO/IEC 15693/ICODE VCD mode (see [9])
- Supported host interfaces
  - NCI protocol interface according to NFC Forum standardization (see [2])
  - I^2C-bus High-speed mode (see [4])
- Integrated power management unit
  - Direct connection to a battery (2.3 V to 5.5 V voltage supply range)
  - Support different Hard Power-Down/Standby states activated by firmware
  - Autonomous mode when host is shut down
- Automatic wake-up via RF field, internal timer and I^2C-bus interface
- Integrated non-volatile memory to store data and executable code for customization

4 Applications

- All devices requiring NFC functionality especially those running in an Android or Linux environment
- TVs, set-top boxes, blu-ray decoders, audio devices
- Home automation, gateways, wireless routers
- Home appliances
- Wearables, remote controls, healthcare, fitness
- Printers, IP phones, gaming consoles, accessories

5 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	Card Emulation and Passive Target; V_{SS} = 0 V	[1] [2]	2.3	-	5.5	V
		Reader, Active Initiator and Active Target; V_{SS} = 0 V	[1] [2]	2.7	-	5.5	V
V_{DD}	supply voltage	internal supply voltage		1.65	1.8	1.95	V
$V_{DD(PAD)}$	$V_{DD(PAD)}$ supply voltage	supply voltage for host interface					
		• 1.8 V host supply;V_{SS} = 0 V	[1]	1.65	1.8	1.95	V
		• 3 V host supply; V_{SS} = 0 V	[1]	3.0	-	3.6	V
I_{BAT}	battery supply current	in Hard Power Down state;V_{BAT} = 3.6 V; T = 25 °C	[3]	-	10	14	µA
		in Standby state;V_{BAT} = 3.6 V; T = 25 °C		-	20	-	µA
		in Monitor state;V_{BAT} = 2.75 V; T = 25 °C		-	-	14	µA
		in low-power polling loop;V_{BAT} = 3.6 V; T = 25 °C;loop time = 500 ms	[4]	-	150	-	µA
		PCD mode at typical 3 V	[2]	-	-	190	mA
$I_{O(VDDPAD)}$	output current on pin $V_{DD(PAD)}$	total current which can be pulled on $V_{DD(PAD)}$ referenced outputs		-	-	15	mA
$I_{th(Ilim)}$	current limit threshold current	current limiter on $V_{DD(TX)}$ pin;$V_{DD(TX)}$ = 3.3 V	[2]	-	180	-	mA
P_{tot}	total power dissipation	Reader; $I_{VDD(TX)}$ = 100 mA;V_{BAT} = 5.5 V		-	-	420	mW
T_{amb}	ambient temperature	JEDEC PCB-0.5		-30	-	+85	°C

[1] V_{SS} represents $V_{SS(PAD)}$ and $V_{SS(TX)}$.

[2] The antenna should be tuned not to exceed this current limit (the detuning effect when coupling with another device must be taken into account).

[3] External clock on NFC_CLK_XTAL1 must be LOW.

[4] See [10] for computing the power consumption as it depends on several parameters.

6 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN7150B0HN/C110xx[1]	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body; 6 mm × 6 mm × 0.85 mm	SOT618-1
PN7150B0UK/C110xx[1]	WLCSP42	wafer level chip-scale package; 42 bumps; 2.88 mm × 2.80 mm × 0.54 mm (Backside coating included)	SOT1459-1

[1] xx = firmware code variant

7 Marking HVQFN40

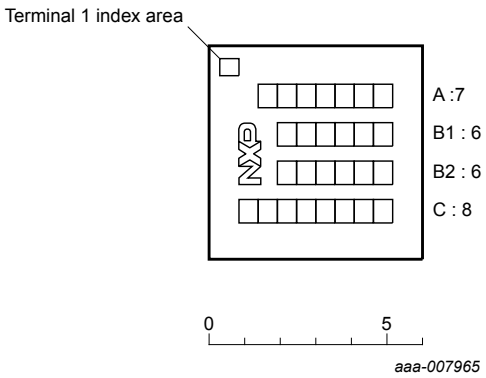

Figure 2. PN7150 package marking HVQFN40 (top view)

Table 3. Marking codes

Type number	Marking code
Line A	7 characters used: basic type number:PN7150x where x is the FW variant
Line B1	6 characters used: diffusion batch sequence number
Line B2	6 characters used: assembly ID number
Line C	7 characters used: manufacturing code including: • diffusion center code: – Z: SSMC – S: Powerchip (PTCT) • assembly center code: – S: ATKH • RoHS compliancy indicator: – D: Dark Green; fully compliant RoHS and no halogen and antimony • manufacturing year and week, 3 digits: – Y: year – WW: week code • product life cycle status code: – X: means not qualified product – nothing means released product

8 Marking WLCSP42

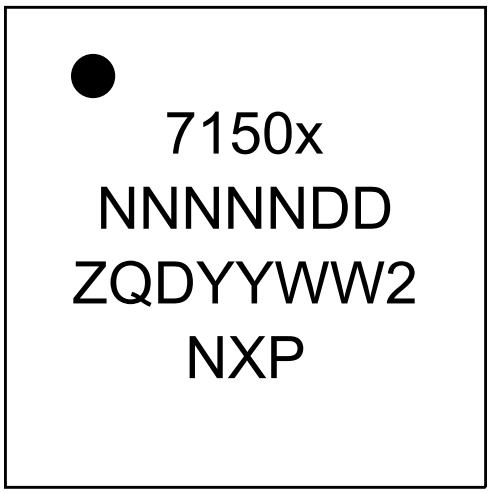

Figure 3. WLCSP42

Table 4. WLCSP package marking (top view)

Line number	Marking code
Line 1	Product identification • Product name: 7150x; where x is the variant.
Line 2	Diffusion batch sequence number • Diffusion fabrication code: NNNNN • Wafer ID: DD
Line 3	Manufacturing code including: • Diffusion center code: – Z: SSMC – s: Global Foundry – S: Powerchip (PTCT) • Assembly center code: – Q: ASE-CL • RoHS compliancy indicator: – D: Dark Green; fully compliant RoHS and no halogen and antimony • Manufacturing year and week; 4 digits: – YY: year – WW: week code • Mask layout version • Product life cycle status code: – X: not qualified product – Nothing means released product
Line 4	NXP logo

9 Block diagram

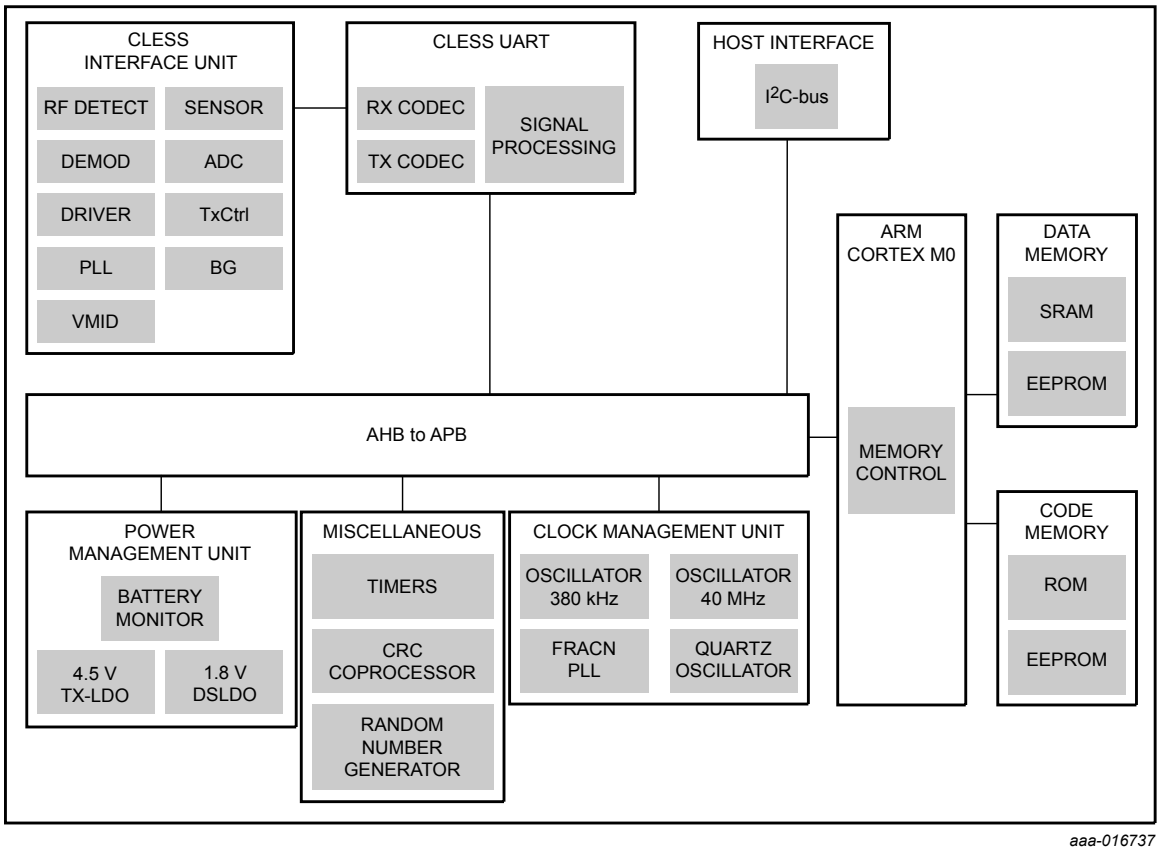

Fig 3. PN7150 block diagram

10 Pinning information

10.1 Pinning HVQFN40

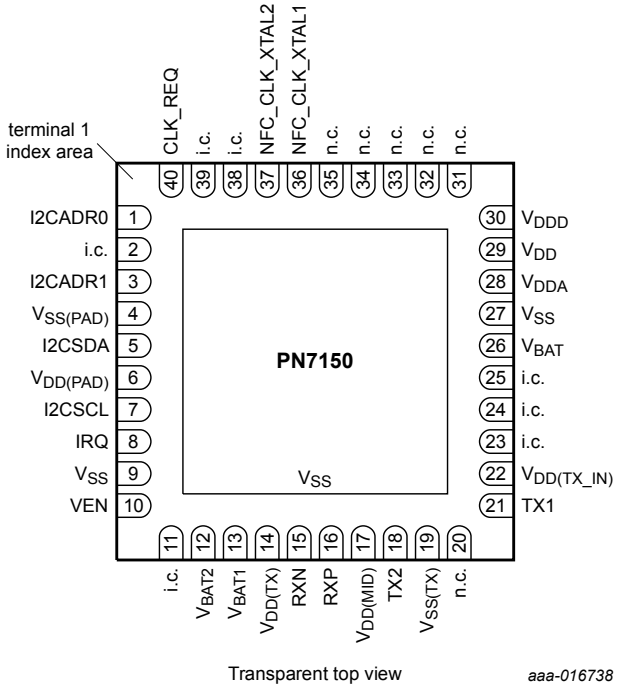

Fig 4. Pinning

Table 5. Pin description

Symbol	Pin	Type[1]	Refer	Description
I2CADR0	1	I	$V_{DD(PAD)}$	I^2C-bus address 0
i.c.	2	-	-	internally connected; must be connected to GND
I2CADR1	3	I	$V_{DD(PAD)}$	I^2C-bus address 1
$V_{SS(PAD)}$	4	G	n/a	pad ground
I2CSDA	5	I/O	$V_{DD(PAD)}$	I^2C-bus data line
$V_{DD(PAD)}$	6	P	n/a	pad supply voltage
I2CSCL	7	I	$V_{DD(PAD)}$	I^2C-bus clock line
IRQ	8	O	$V_{DD(PAD)}$	interrupt request output
V_{SS}	9	G	n/a	ground
VEN	10	I	V_{BAT}	reset pin. Set the device in Hard Power Down
i.c.	11	-	-	internally connected; leave open
V_{BAT2}	12	P	n/a	battery supply voltage; must be connected to V_{BAT}

Symbol	Pin	Type[1]	Refer	Description
V_{BAT1}	13	P	n/a	TXLDO input supply voltage
$V_{DD(TX)}$	14	P	n/a	transmitter supply voltage
RXN	15	I	V_{DD}	negative receiver input
RXP	16	I	V_{DD}	positive receiver input
$V_{DD(MID)}$	17	P	n/a	receiver reference input supply voltage
TX2	18	O	$V_{DD(TX)}$	antenna driver output
$V_{SS(TX)}$	19	G	n/a	contactless transmitter ground
n.c.	20	-	-	not connected
TX1	21	O	$V_{DD(TX)}$	antenna driver output
$V_{DD(TX\_IN)}$	22	P	n/a	transmitter input supply voltage; must be connected to $V_{DD(TX)}$
i.c.	23	-	-	internally connected; leave open
i.c.	24	-	-	internally connected; leave open
i.c.	25	-	-	internally connected; leave open
V_{BAT}	26	P	n/a	battery supply voltage
V_{SS}	27	G	n/a	ground
V_{DDA}	28	P	n/a	analog supply voltage; must be connected to V_{DD}
V_{DD}	29	P	n/a	supply voltage
V_{DDD}	30	P	n/a	digital supply voltage; must be connected to V_{DD}
n.c.	31	-	-	not connected
n.c.	32	-	-	not connected
n.c.	33	-	-	not connected
n.c.	34	-	-	not connected
n.c.	35	-	-	not connected
NFC_CLK_XTAL1	36	I	V_{DD}	oscillator input/PLL input
NFC_CLK_XTAL2	37	O	V_{DD}	oscillator output
i.c.	38	-	-	internally connected; leave open
i.c.	39	-	-	internally connected; leave open
CLK_REQ	40	O	$V_{DD(PAD)}$	clock request pin

[1] P = power supply
G = ground
I = input
O = output
I/O = input/output

10.2 Pinning WLCSP42

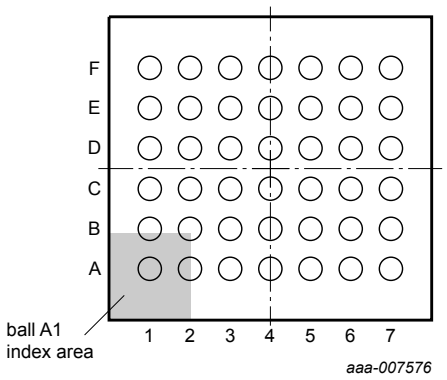

Figure 4. WLCSP42 pinning (bottom view)

Table 6. WLCSP package marking (top view)

Symbol	Pin	Type[1]	Refer	Description
V_{BAT2}	A1	P	n/a	battery supply voltage; to be connected to V_{BAT}
i.c.	A2	-	-	internally connected; leave open
V_{BAT1}	A3	P	n/a	TXLDO input supply voltage
RXN	A4	I	V_{DD}	negative receiver input
$V_{DD(MID)}$	A5	P	n/a	receiver reference input supply voltage
TX2	A6	O	$V_{DD(TX)}$	antenna driver output
TX1	A7	O	$V_{DD(TX)}$	antenna driver output
V_{SS}	B1	G	n/a	ground
V_{SS}	B2	G	n/a	ground
$V_{DD(TX)}$	B3	P	n/a	transmitter supply voltage
RXP	B4	I	V_{DD}	positive receiver input
V_{SS}	B5	G	n/a	ground
$V_{SS(TX)}$	B6	G	n/a	contactless transmitter ground
$V_{DD(TX\_IN)}$	B7	P	n/a	transmitter input supply voltage; must be connected to $V_{DD(TX)}$
IRQ	C1	O	$V_{DD(PAD)}$	interrupt request output
$V_{DD(PAD)}$	C2	P	n/a	pad supply voltage
VEN	C3	I	V_{BAT}	reset pin. Set the device in Hard Power Down
V_{SS}	C4	G	n/a	power ball. Shall be connected to ground for dissipation
V_{SS}	C5	G	n/a	power ball. Shall be connected to ground for dissipation
i.c.	C6	-	-	internally connected; leave open
i.c.	C7	-	-	internally connected; leave open
I2CSCL	D1	I	$V_{DD(PAD)}$	I^2C-bus clock line
I2CSDA	D2	I/O	$V_{DD(PAD)}$	I^2C-bus data line
CLK_REQ	D3	O	$V_{DD(PAD)}$	clock request pin

Symbol	Pin	Type[1]	Refer	Description
i.c.	D4	-	-	internally connected; leave open
i.c.	D5	-	-	internally connected; leave open
V_{DDD}	D6	P	n/a	digital supply voltage; must be connected to V_{DD}
V_{BAT}	D7	P	n/a	battery supply voltage
$V_{SS(PAD)}$	E1	G	n/a	pad ground
I2CADR1	E2	I	$V_{DD(PAD)}$	I^2C-bus address 1
i.c.	E3	-	-	internally connected; leave open
NFC_CLK_XTAL1	E4	I	V_{DD}	oscillator input/PLL input
i.c.	E5	-	-	internally connected; leave open
i.c.	E6	-	-	internally connected; leave open
V_{DD}	E7	P	n/a	LDO output supply voltage
I2CADR0	F1	I	$V_{DD(PAD)}$	I^2C-bus address 0
i.c.	F2	-	-	internally connected; must be connected to GND
NFC_CLK_XTAL2	F3	O	V_{DD}	oscillator output
i.c.	F4	-	-	internally connected; leave open
i.c.	F5	-	-	internally connected; must be connected to GND
i.c.	F6	-	-	internally connected; leave open
i.c.	F7	-	-	internally connected; leave open

[1] P = power supply
G = ground
I = input
O = output
I/O = input/output

11 Functional description

PN7150 can be connected on a host controller through I^2C-bus. The logical interface towards the host baseband is NCI-compliant [2] with additional command set for NXP-specific product features. This IC is fully user controllable by the firmware interface described in [5].

Moreover, PN7150 provides flexible and integrated power management unit in order to preserve energy supporting Power Off mode.

In the following chapters you will find also more details about PN7150 with references to very useful application note such as:

- PN7150 User Manual ([5]):
  User Manual describes the software interfaces (API) based on the NFC forum NCI standard. It does give full description of all the NXP NCI extensions coming in addition to NCI standard ([2]).
- PN7150 Hardware Design Guide ([6]):
  Hardware Design Guide provides an overview on the different hardware design options offered by the IC and provides guidelines on how to select the most appropriate ones for a given implementation. In particular, this document highlights the different chip power states and how to operate them in order to minimize the average NFC-related power consumption so to enhance the battery lifetime.
- PN7150 Antenna and Tuning Design Guide ([7]):
  Antenna and Tuning Design Guide provides some guidelines regarding the way to design an NFC antenna for the PN7150 chip.
  It also explains how to determine the tuning/matching network to place between this antenna and the PN7150.
  Standalone antenna performances evaluation and final RF system validation (PN7150 + tuning/matching network + NFC antenna within its final environment) are also covered by this document.
- PN7150 Low-Power Mode Configuration ([10]):
  Low-Power Mode Configuration documentation provides guidance on how PN7150 can be configured in order to reduce current consumption by using Low-power polling mode.

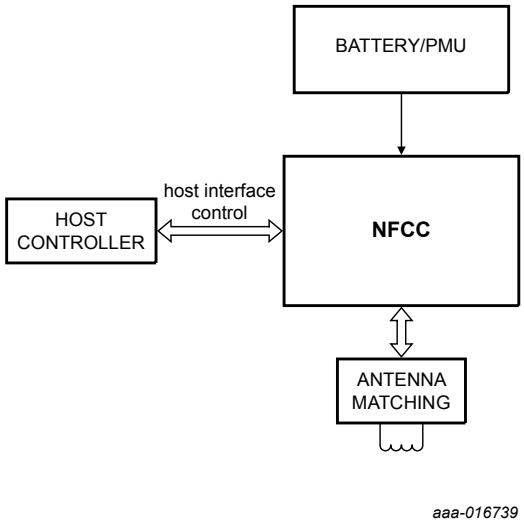

Fig 5. PN7150 connection

11.1 System modes

11.1.1 System power modes

PN7150 is designed in order to enable the different power modes from the system.

2 power modes are specified: Full power mode and Power Off mode.

Table 7. System power modes description

System power mode	Description
Full power mode	the main supply (V_{BAT}) as well as the host interface supply ($V_{DD(PAD)}$) is available, all use cases can be executed
Power Off mode	the system is kept Hard Power Down (HPD)

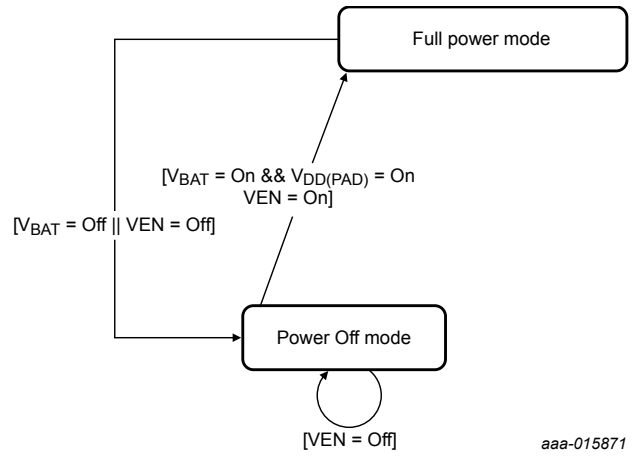

Fig 6. System power mode diagram

Table 6 summarizes the system power mode of the PN7150 depending on the status of the external supplies available in the system:

Table 8. System power modes configuration

V_{BAT}	VEN	Power mode
Off	X	Power Off mode
On	Off	Power Off mode
On	On	Full power mode

Depending on power modes, some application states are limited:

Table 9. System power modes description

System power mode	Allowed communication modes
Power Off mode	no communication mode available
Full power mode	Reader/Writer, Card Emulation, P2P modes

11.1.2 PN7150 power states

Next to system power modes defined by the status of the power supplies, the power states include the logical status of the system thus extend the power modes.

4 power states are specified: Monitor, Hard Power Down (HPD), Standby, Active.

Table 10. PN7150 power states

Power state name	Description
Monitor	The PN7150 is supplied by V_{BAT} which voltage is below its programmable critical level, VEN voltage > 1.1 V and the Monitor state is enabled. The system power mode is Power Off mode.

Power state name	Description
Hard Power Down	The PN7150 is supplied by V_{BAT} which voltage is above its programmable critical level when Monitor state is enabled and PN7150 is kept in Hard Power Down (VEN voltage is kept low by host or SW programming) to have the minimum power consumption. The system power mode is in Power Off.
Standby	The PN7150 is supplied by V_{BAT} which voltage is above its programmable critical level when the Monitor state is enabled, VEN voltage is high (by host or SW programming) and minimum part of PN7150 is kept supplied to enable configured wake-up sources which allow to switch to Active state; RF field,Host interface. The system power mode is Full power mode.
Active	The PN7150 is supplied by V_{BAT} which voltage is above its programmable critical level when Monitor state is enabled, VEN voltage is high (by host or SW programming) and the PN7150 internal blocks are supplied. 3 functional modes are defined: Idle, Target and Initiator. The system power mode is Full power mode.

At application level, the PN7150 will continuously switch between different states to optimize the current consumption (polling loop mode). Refer to Table 1 for targeted current consumption in here described states.

The PN7150 is designed to allow the host controller to have full control over its functional states, thus of the power consumption of the PN7150 based NFC solution and possibility to restrict parts of the PN7150 functionality.

11.1.2.1 Monitor state

In Monitor state, the PN7150 will exit it only if the battery voltage recovers over the critical level. Battery voltage monitor thresholds show hysteresis behavior as defined in Table 27.

11.1.2.2 Hard Power Down (HPD) state

The Hard Power Down state is entered when $V_{DD(PAD)}$ and V_{BAT} are high by setting VEN voltage < 0.4 V. As these signals are under host control, the PN7150 has no influence on entering or exiting this state.

11.1.2.3 Standby state

Active state is PN7150's default state after boot sequence in order to allow a quick configuration of PN7150. It is recommended to change the default state to Standby state after first boot in order to save power. PN7150 can switch to Standby state autonomously (if configured by host).

In this state, PN7150 most blocks including CPU are no more supplied. Number of wake-up sources exist to put PN7150 into Active state:

- I^2C-bus interface wake-up event
- Antenna RF level detector
- Internal timer event when using polling loop (380 kHz Low-power oscillator is enabled)

If wake-up event occurs, PN7150 will switch to Active state. Any further operation depends on software configuration and/or wake-up source.

11.1.2.4 Active state

Within the Active state, the system is acting as an NFC device. The device can be in 3 different functional modes: Idle, Poller and Target.

Table 11. Functional modes in active state

Functional modes	Description
Idle	the PN7150 is active and allows host interface communication. The RF interface is not activated.
Listener	the PN7150 is active and is configured for listening to external device.
Poller	the PN7150 is active and is configured in Poller mode. It polls external device

Poller mode

In this mode, PN7150 is acting as Reader/Writer or NFC Initiator, searching for or communicating with passive tags or NFC target. Once RF communication has ended, PN7150 will switch to active battery mode (that is, switch off RF transmitter) to save energy. Poller mode shall be used with 2.7 V < V_{BAT} < 5.5 V and VEN voltage > 1.1 V. Poller mode shall not be used with V_{BAT} < 2.7 V. $V_{DD(PAD)}$ is within its operational range (see Table 1).

Listener mode

In this mode, PN7150 is acting as a card or as an NFC Target. Listener mode shall be used with 2.3 V < V_{BAT} < 5.5 V and VEN voltage > 1.1 V.

11.1.2.5 Polling loop

The polling loop will sequentially set PN7150 in different power states (Active or Standby). All RF technologies supported by PN7150 can be independently enabled within this polling loop.

There are 2 main phases in the polling loop:

- Listening phase. The PN7150 can be in Standby power state or Listener mode
- Polling phase. The PN7150 is in Poller mode

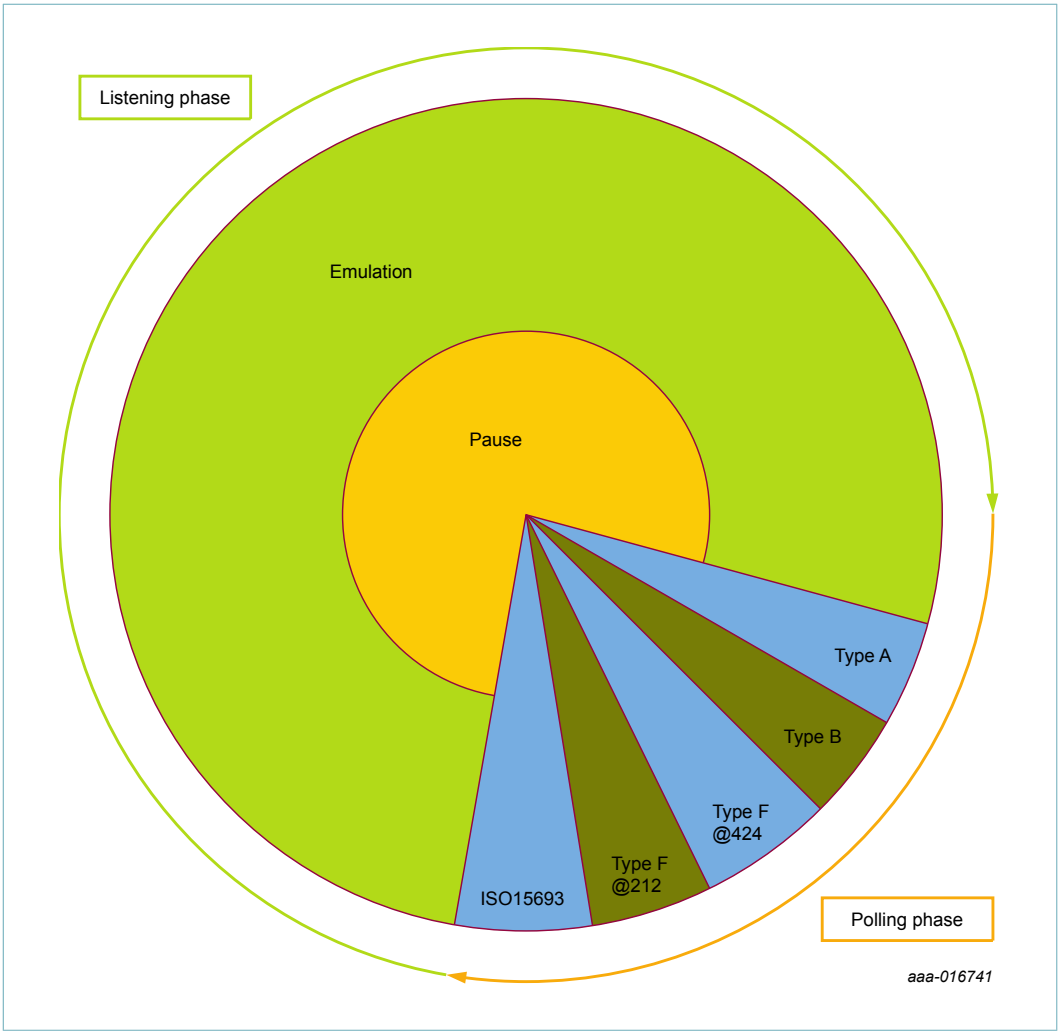

Fig 7. Polling loop: all phases enabled

Listening phase uses Standby power state (when no RF field) and PN7150 goes to Listener mode when RF field is detected. When in Polling phase, PN7150 goes to Poller mode.

To further decrease the power consumption when running the polling loop, PN7150 features a low-power RF polling. When PN7150 is in Polling phase instead of sending regularly RF command, PN7150 senses with a short RF field duration if there is any NFC Target or card/tag present. If yes, then it goes back to standard polling loop. With 500 ms (configurable duration, see [5]) listening phase duration, the average power consumption is around 150 µA.

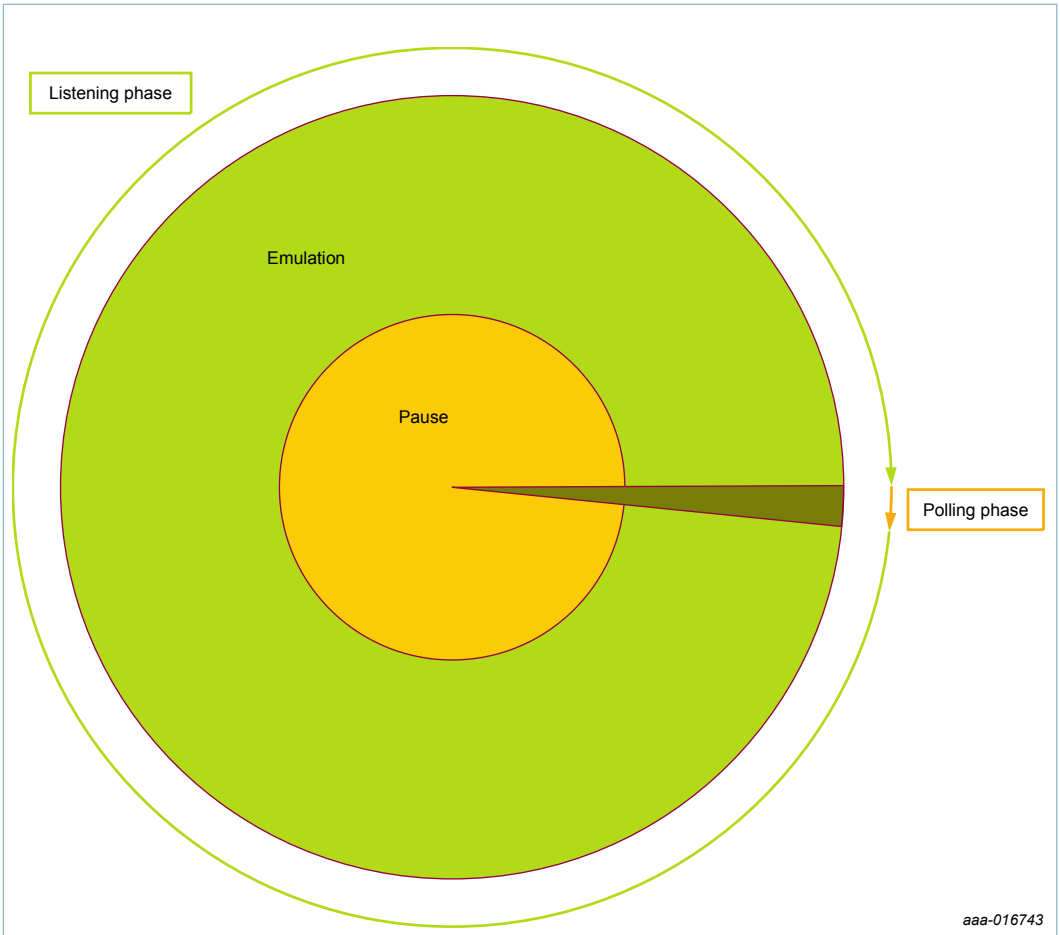

Fig 8. Polling loop: low-power RF polling

Detailed description of polling loop configuration options is given in [5].

11.2 Microcontroller

PN7150 is controlled via an embedded ARM Cortex-M0 microcontroller core.

PN7150 features integrated in firmware are referenced in [5].

11.3 Host interface

PN7150 provides the support of an I^2C-bus Slave Interface, up to 3.4 MBaud.

The host interface is waken-up on I^2C-bus address.

To enable and ensure data flow control between PN7150 and host controller, additionally a dedicated interrupt line IRQ is provided which Active state is programmable. See [5] for more information.

11.3.1 I²C-bus interface

The I²C-bus interface implements a slave I²C-bus interface with integrated shift register, shift timing generation and slave address recognition.

I²C-bus Standard mode (100 kHz SCL), Fast mode (400 kHz SCL) and High-speed mode (3.4 MHz SCL) are supported.

The mains hardware characteristics of the I²C-bus module are:

- Support slave I²C-bus
- Standard, Fast and High-speed modes supported
- Wake-up of PN7150 on its address only
- Serial clock synchronization can be used by PN7150 as a handshake mechanism to suspend and resume serial transfer (clock stretching)

The I²C-bus interface module meets the I²C-bus specification [4] except General call, 10-bit addressing and Fast mode Plus (Fm+).

11.3.1.1 I²C-bus configuration

The I²C-bus interface shares four pins with I²C-bus interface also supported by PN7150. When I²C-bus is configured in EEPROM settings, functionality of interface pins changes to one described in Table 10.

Table 12. Functionality for I²C-bus interface

Pin name	Functionality
I2CADR0	I²C-bus address 0
I2CADR1	I²C-bus address 1
I2CSCL[1]	I²C-bus clock line
I2CSDA[1]	I²C-bus data line

[1] I2CSCL and I2CSDA are not fail-safe and $V_{DD(pad)}$ shall always be available when using the SCL and SDA lines connected to these pins.

PN7150 supports 7-bit addressing mode. Selection of the I²C-bus address is done by 2-pin configurations on top of a fixed binary header: 0, 1, 0, 1, 0, I2CADR1, I2CADR0, R/W.

Table 13. I²C-bus interface addressing

I2CADR1	I2CADR0	I²C-bus address (R/W = 0, write)	I²C-bus address (R/W = 1, read)
0	0	0x50	0x51
0	1	0x52	0x53
1	0	0x54	0x55
1	1	0x56	0x57

11.4 PN7150 clock concept

There are 4 different clock sources in PN7150:

- 27.12 MHz clock coming either/or from:

- Internal oscillator for 27.12 MHz crystal connection
- Integrated PLL unit which includes a 1 GHz VCO, taking is reference clock on pin NFC_CLK_XTAL1

- 13.56 MHz RF clock recovered from RF field
- Low-power oscillator 40 MHz
- Low-power oscillator 380 kHz

11.4.1 27.12 MHz quartz oscillator

When enabled, the 27.12 MHz quartz oscillator applied to PN7150 is the time reference for the RF front end when PN7150 is behaving in Reader mode or NFCIP-1 initiator.

Therefore stability of the clock frequency is an important factor for reliable operation. It is recommended to adopt the circuit shown in Figure 9.

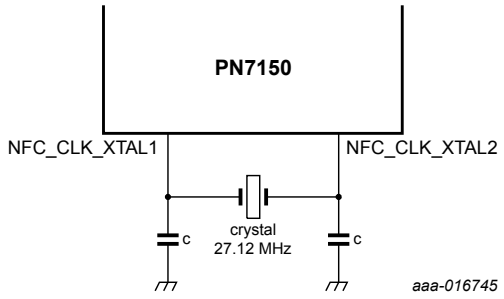

Fig 9. 27.12 MHz crystal oscillator connection

Table 12 describes the levels of accuracy and stability required on the crystal.

Table 14. Crystal requirements

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{xtal}	crystal frequency	ISO/IEC and FCC compliancy		-	27.12	-	MHz
Δf_{xtal}	crystal frequency accuracy	full operating range	[1]	-100	-	+100	ppm
		all V_{BAT} range;T = 20 °C	[1]	-50	-	+50	ppm
		all temperature range;V_{BAT} = 3.6 V	[1]	-50	-	+50	ppm
ESR	equivalent series resistance			-	50	100	Ω
C_L	load capacitance			-	10	-	pF
P_{xtal}	crystal power dissipation			-	-	100	µW

[1] This requirement is according to FCC regulations requirements. To meet only ISO/IEC 14443 and ISO/IEC 18092, then ± 14 kHz apply.

11.4.2 Integrated PLL to make use of external clock

When enabled, the PLL is designed to generate a low noise 27.12 MHz for an input clock 13 MHz, 19.2 MHz, 24 MHz, 26 MHz, 38.4 MHz and 52 MHz.

The 27.12 MHz of the PLL is used as the time reference for the RF front end when PN7150 is behaving in Reader mode or ISO/IEC 18092 Initiator as well as in Target when configured in Active Communication mode.

The input clock on NFC_CLK_XTAL1 shall comply with the.following phase noise requirements for the following input frequency: 13 MHz, 19.2 MHz, 24 MHz, 26 MHz, 38.4 MHz and 52 MHz:

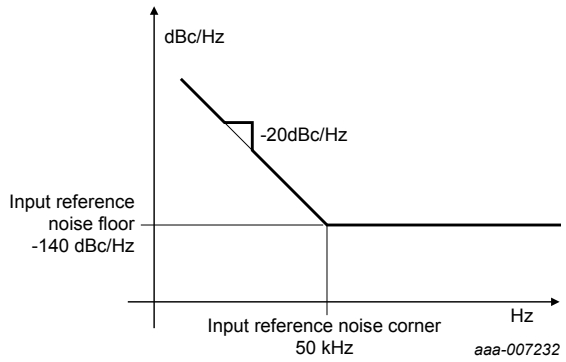

Fig 10. Input reference phase noise characteristics

This phase noise is equivalent to an RMS jitter of 6.23 ps from 10 Hz to 1 MHz. For configuration of input frequency, refer to [9]. There are 6 pre-programmed and validated frequencies for the PLL: 13 MHz, 19.2 MHz, 24 MHz, 26 MHz, 38.4 MHz and 52 MHz.

Table 15. PLL input requirements

Coupling: single-ended, AC coupling;

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency	ISO/IEC and FCC compliancy		-	13	-	MHz
				-	19.2	-	MHz
				-	24	-	MHz
				-	26	-	MHz
				-	38.4	-	MHz
				-	52	-	MHz
$f_{i(ref)acc}$	reference input frequency accuracy	full operating range;frequencies typical values:13 MHz, 26 MHz and 52 MHz	[1]	-25	-	+25	ppm
		full operating range;frequencies typical values:19.2 MHz, 24 MHz and 38.4 MHz	[1]	-50	-	+50	ppm

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
φ_n	phase noise	input noise floor at 50 kHz		-140	-	-	dB/Hz
Sinusoidal shape							
$V_{i(p-p)}$	peak-to-peak input voltage			0.2	-	1.8	V
$V_{i(clk)}$	clock input voltage			0	-	1.8	V
Square shape							
$V_{i(clk)}$	clock input voltage			0	-	1.8 ± 10 %	V

[1] This requirement is according to FCC regulations requirements. To meet only ISO/IEC 14443 and ISO/IEC 18092, then ± 400 ppm limits apply.

For detailed description of clock request mechanisms, refer to [5] and [6].

11.4.3 Low-power 40 MHz ± 2.5 % oscillator

Low-power OSC generates a 40 MHz internal clock. This frequency is divided by two to make the system clock.

11.4.4 Low-power 380 kHz oscillator

A Low Frequency Oscillator (LFO) is implemented to drive a counter (WUC) waking-up PN7150 from Standby state. This allows implementation of low-power reader polling loop at application level. Moreover, this 380 kHz is used as the reference clock for write access to EEPROM memory.

11.5 Power concept

11.5.1 PMU functional description

The Power Management Unit of PN7150 generates internal supplies required by PN7150 out of V_{BAT} input supply voltage:

- V_{DD}: internal supply voltage
- $V_{DD(TX)}$: output supply voltage for the RF transmitter

The Figure 11 describes the main blocks available in PMU:

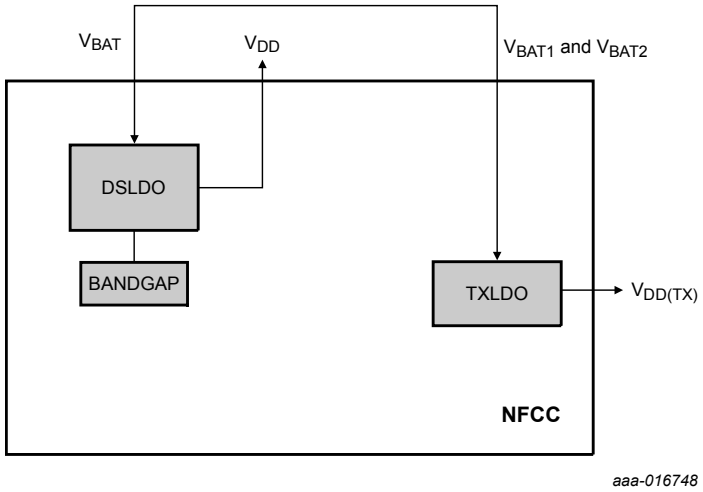

Fig 11. PMU functional diagram

11.5.2 DSLDO: Dual Supply LDO

The input pin of the DSLDO is V_{BAT}.

The Low drop-out regulator provides V_{DD} required in PN7150.

11.5.3 TXLDO

Transmitter voltage can be generated by internal LDO ($V_{DD(TX)}$) or come from an external supply source $V_{DD(TX)}$.

The regulator has been designed to work in 2 configurations:

11.5.3.1 Configuration 1: supply connection in case the battery is used to generate RF field

The Low drop Out Regulator has been designed to generate a 3.0 V, 3.3 V or 3.6 V supply voltage to a transmitter with a current load up to 180 mA.

The output is called $V_{DD(TX)}$. The input supply voltage of this regulator is a battery voltage connected to V_{BAT1} pin.

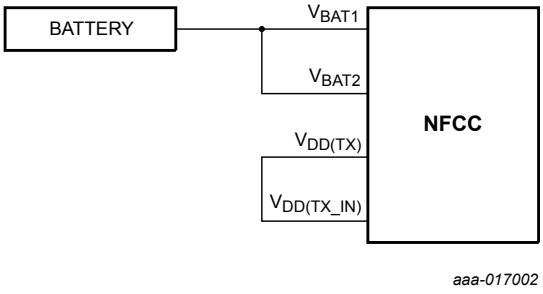

Fig 12. $V_{BAT1} = V_{BAT2}$ (between 2.3 V and 5.5 V)