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PN7462 family

NFC Cortex-M0 microcontroller

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406342

Product data sheet
COMPANY PUBLIC

1 General description

The PN7462 family is a family of 32-bit ARM Cortex-M0-based NFC microcontrollers offering high performance and low power consumption. It has a simple instruction set and memory addressing along with a reduced code size compared to existing architectures. PN7462 family offers an all in one solution, with features such as NFC, supporting all NFC Forum modes, microcontroller, optional contact smart card reader, and software in a single chip. It operates at CPU frequencies of up to 20 MHz.

Table 1. Comparison of the PN7462 family members

	PN7462AUHN	PN7462AUEV	PN7412AUHN	PN7362AUHN	PN7362AUEV	PN7360AUHN	PN7360AUEV
Contact smart card reader	Class A, B, C	No	Class A, B, C	No	No	No	No
ISO/IEC 7816 UART	Yes	Yes	Yes	No	No	No	No
Contactless interface	Yes	Yes	No	Yes	Yes	Yes	Yes
Available Flash memory	160 kB	160 kB	160 kB	160 kB	160 kB	80 kB	80 kB
SRAM data memory	12 kB	12 kB	12 kB	12 kB	12 kB	12 kB	12 kB
General purposes I/O	12 up-to 21	14 up-to 21	12 up-to 21	14 up-to 21	14 up-to 21	14 up-to 21	14 up-to 21
Package type	HVQFN64	VFBGA64	HVQFN64	HVQFN64	VFBGA64	HVQFN64	VFBGA64

Having the differences listed in the table above, all products within the PN7462 family are equipped with 12 kB of SRAM data memory and 4 kB EEPROM. All products within the family also include one host interface with either high-speed mode I^2C-bus, SPI, USB or high-speed UART, and two master interfaces, SPI and Fast-mode Plus I^2C-bus. Four general-purpose counter/timers, a random number generator, one CRC coprocessor and up to 21 general-purpose I/O pins.

The PN7462 family NFC microcontroller offers a one chip solution to build contactless, or contact and contactless applications. It is equipped with a highly integrated high-power output NFC-IC for contactless communication at 13.56 MHz enabling EMV-compliance on RF level, without additional external active components.

By integrating a contact ISO/IEC 7816 interface on a single chip, the PN7462AUHN provides a solution for dual interface smart card readers. Whereas the PN7412AUHN offers a solution for a contact reader only. The PN7462AUHN and PN7412AUHN contact interfaces offer a high level of security for the card by performing current limiting, short-

circuit detection, ESD protection as well as supply supervision. On PN7462AUHN, PN7412AUHN and PN7462AUEV, an additional UART output is also implemented to address applications where more than one contact card slot is needed. It enables an easy connection to multiple smart card slot interfaces like TDA8026.

PN7462AUHN and PN7412AUHN provide thermal and short-circuit protection on all card contacts. It also provides automatic activation and deactivation sequences initiated by software or hardware.

2 Features and benefits

2.1 Integrated contact interface frontend

This chapter applies to the products with contact interface only.

- Class A, B, and C cards can work on 1.8 V, 3 V, and 5 V supply
- Specific ISO UART, variable baud rate through frequency or division ratio programming, error management at character level for T = 0, and extra guard time register
- DC-to-DC converter for class A support starting at 3 V, and class B support starting at 2.7 V
- Thermal and short-circuit protection on contact cards
- Automatic activation and deactivation sequence, initiated by software or by hardware in case of short-circuit, card removal, overheating, and V_{DD} or V_{DD} drop-out
- Enhanced ESD protection (> 12 kV)
- ISO/IEC 7816 compliant
- Compliance with EMV contact protocol specification
- Clock generation up to 13.56 MHz
- Synchronous card support
- Possibility to extend the number of contact interfaces, with the addition of slot extenders such as TDA8026

2.2 Integrated ISO/IEC 7816-3&4 UART interface

This chapter applies to the products with Integrated ISO/IEC 7816 UART interface only.

The PN7462 family offers the possibility to extend the number of contact interfaces available. It uses an I/O auxiliary interface to connect a slot extension (TDA8035 - 1 slot, TDA8020 - 2 slots, and TDA8026 - 5 slots).

- Class A (5 V), class B (3 V), and class C (1.8 V) smart card supply
- Protection of smart card
- Three protected half-duplex bidirectional buffered I/O lines (C4, C7, and C8)
- Compliant with ISO/IEC 7816 and EMVCo standards

2.3 Integrated contactless interface frontend

This chapter applies to the products with integrated contactless interface only.

- High RF output power frontend IC for transfer speed up to 848 kbit/s
- NFC IP1 and NFC IP2 support
- Full NFC Forum tag support (type 1, type 2, type 3, type 4A, type 4B and type 5)
- P2P active and passive, target, and initiator
- Card emulation ISO14443 type A
- ISO/IEC 14443 type A and type B
- MIFARE products using Crypto 1
- ISO/IEC 15693, and ISO/IEC 18000-3 mode 3
- Low-power card detection

- Dynamic Power Control (DPC)
- Adaptive Wave Control (AWC)
- Adaptive Range Control (ARC)
- Compliance with EMV contactless protocol specification

2.4 Cortex-M0 microcontroller

- Processor core
  - ARM Cortex: 32-bit M0 processor
  - Built-in Nested Vectored Interrupt Controller (NVIC)
  - Non-maskable interrupt
  - 24-bit system tick timer
  - Running frequency of up to 20 MHz
  - Clock management to enable low power consumption
- Memory
  - Flash: 160 kB / 80 kB
  - SRAM: 12 kB
  - EEPROM: 4 kB
  - 40 kB boot ROM included, including USB mass storage primary boot loader for code download
- Debug option
  - Serial Wire Debug (SWD) interface
- Peripherals
  - *Host interface:*
  - USB 2.0 full speed with USB 3.0 hub connection capability
  - HSUART for serial communication, supporting standards speeds from 9600 bauds to 115200 bauds, and faster speed up to 1.288 Mbit/s
  - SPI with half-duplex and full duplex capability with speeds up to 7 Mbit/s
  - I^2C supporting standard mode, fast mode, and high-speed mode with multiple address supports
  - *Master interface:*
  - SPI with half-duplex capability from 1 Mbit/s to 6.78 Mbit/s
  - I^2C supporting standard mode, fast mode, fast mode plus, and clock stretching
- Up to 21 General-Purpose I/O (GPIO) with configurable pull-up/pull-down resistors
- GPIO1 to GPIO12 can be used as edge and level sensitive interrupt sources
- Power
  - Two reduced power modes: standby mode and hard power-down mode
  - Supports suspend mode for USB host interface
  - Processor wake-up from hard power-down mode, standby mode, suspend mode via host interface, GPIOs, RF field detection
  - Integrated PMU to adjust internal regulators automatically, to minimize the power consumption during all possible power modes
  - Power-on reset
  - RF supply: external, or using an integrated LDO (TX LDO, configurable with 3 V, 3.3 V, 3.6 V, 4.5 V, and 4.75 V)
  - Pad voltage supply: external 3.3 V or 1.8 V, or using an integrated LDO (3.3 V supply)
- Timers

  - Four general-purpose timers
  - Programmable Watchdog Timer (WDT)
- CRC coprocessor
- Random number generator
- Clocks
  - Crystal oscillator at 27.12 MHz
  - Dedicated PLL at 48 MHz for the USB
  - Integrated HFO 20 MHz and LFO 365 kHz
- General
  - HVQFN64 package
  - VFBGA64 package
  - Temperature range: -40 °C to +85 °C

3 Applications

- Physical access control
- Gaming
- USB NFC reader, including dual interface smart card readers
- Home banking, payment readers EMVCo compliant
- High integration devices
- NFC applications

4 Quick reference data

Table 2. Quick reference data

Operating range: -40 °C to +85 °C unless specified; contact interface: $V_{DDP(VBUSP)}$ = $V_{DDP(VBUS)}$; contactless interface: internal LDO not used

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DDP(VBUS)}$	power supply voltage on pin VBUS	card emulation, passive target (PLM)	2.3	-	5.5	V
		all RF modes; class B and class C contact interface support	2.7	-	5.5	V
		all RF modes; class A, class B and class C contact interface support	3	-	5.5	V
$V_{DD(PVDD)}$	PVDD supply voltage	1.8 V	1.65	1.8	1.95	V
		3.3 V	3	3.3	3.6	V
$I_{DDP(VBUS)}$	power supply current on pin VBUS	in hard power-down mode; T = 25 °C; $V_{DDP(VBUS)}$ = 5.5 V; RST_N = 0	-	12	18	µA
		stand by mode; T = 25 °C; $V_{DDP(VBUS)}$ = 3.3 V; external PVDD LDO used	-	18	-	µA
		stand by mode; T = 25 °C; $V_{DDP(VBUS)}$ = 5.5 V; internal PVDD LDO used	-	55	-	µA
		suspend mode, USB interface; $V_{DDP(VBUS)}$ = 5.5 V; external PVDD supply; T = 25 °C	-	120	250	µA
$I_{DD(TVDD)}$	TVDD supply current	on pin TVDD_IN; maximum supported current by the contactless interface	-	-	250	mA
P_{max}	maximum power dissipation		-	-	1050	mW
T_{amb}	ambient temperature	JEDEC PCB	-40	-	+85	°C

5 Ordering information

The table below lists the ordering information of the PN7462 family.

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PN7462AUHN	HVQFN64	160 kB memory; contact interface; ISO/IEC 7816-3&4 UART interface; plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-4
PN7462AUEV	VFBGA64	160 kB memory; no contact interface; ISO/IEC 7816-3&4 UART interface; plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm	SOT1307-2
PN7412AUHN	HVQFN64	160 kB memory; contact interface; ISO/IEC 7816-3&4 UART interface; no contactless interface plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-4
PN7362AUHN	HVQFN64	160 kB memory; no contact interface; no ISO/IEC 7816-3&4 UART interface; plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-4
PN7362AUEV	VFBGA64	160 kB memory; no contact interface; no ISO/IEC 7816-3&4 UART interface; plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm	SOT1307-2
PN7360AUHN	HVQFN64	80 kB memory; no contact interface; no ISO/IEC 7816-3&4 UART interface; plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-4
PN7360AUEV	VFBGA64	80 kB memory; no contact interface; no ISO/IEC 7816-3&4 UART interface; plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm	SOT1307-2

6 Block diagram

6.1 Block diagram PN7462 HVQFN64

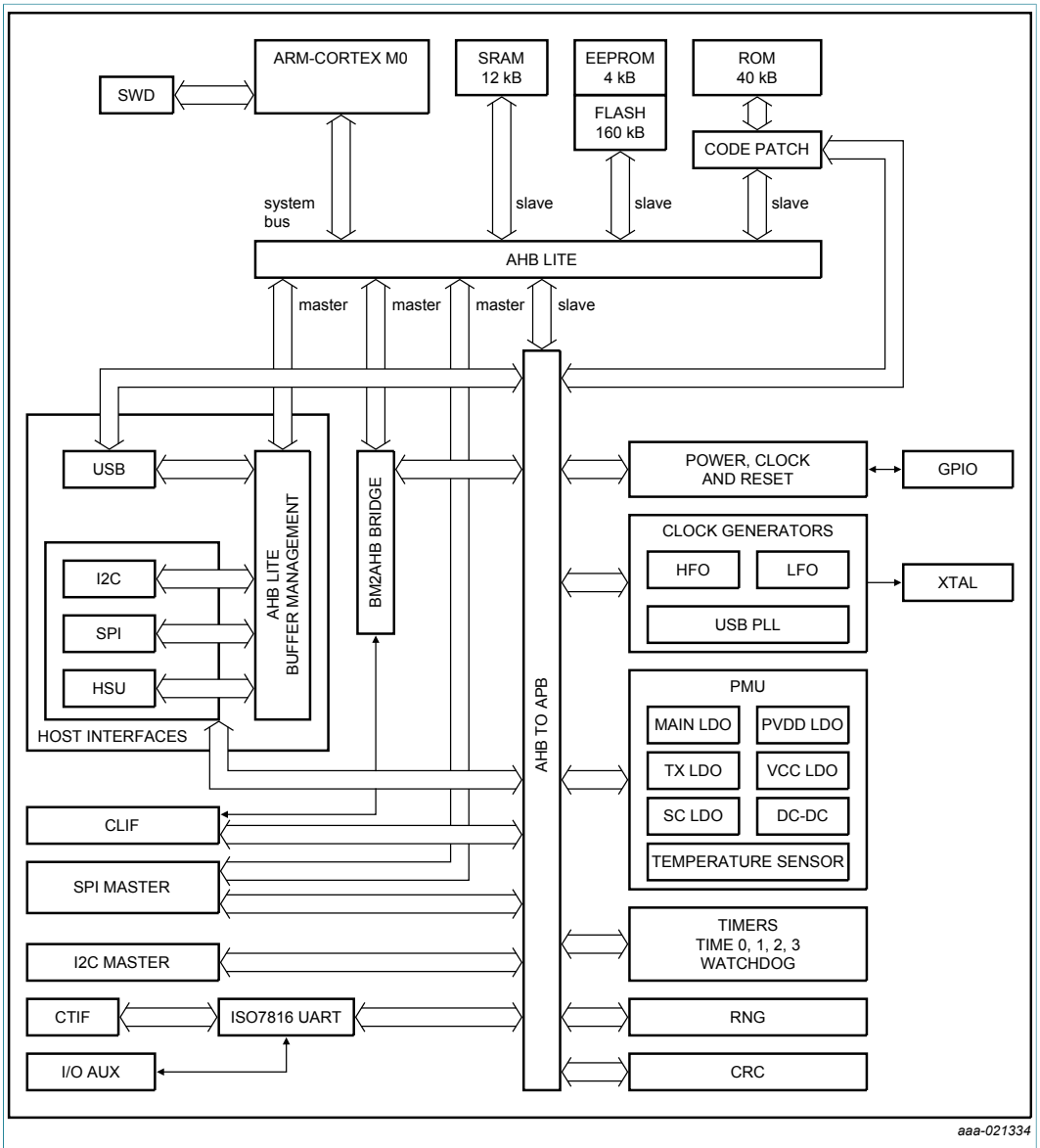


Figure 1. Block diagram

6.2 Block diagram PN7462 VFBGA64

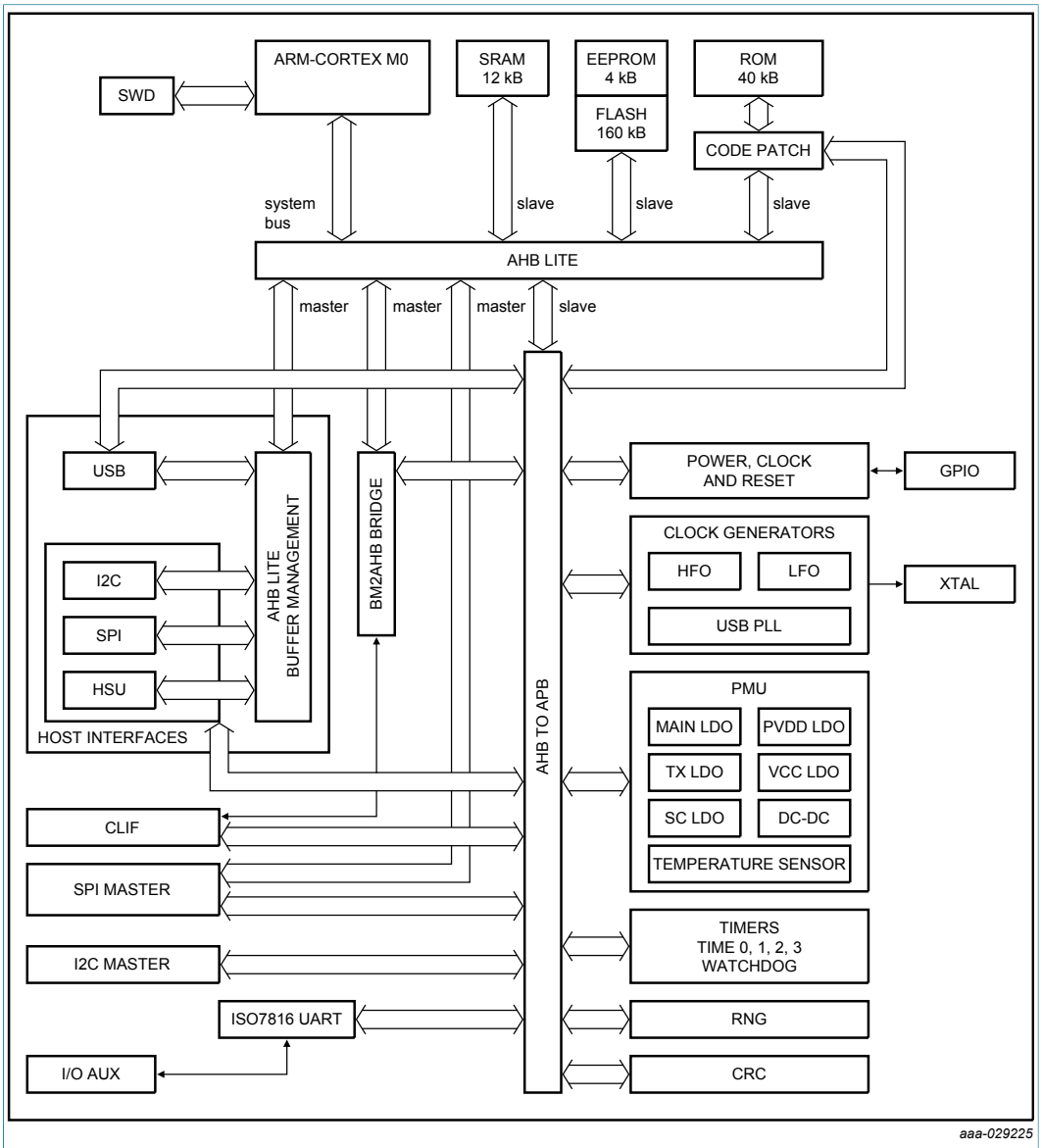


Figure 2. Block diagram

6.3 Block diagram PN7412 HVQFN64

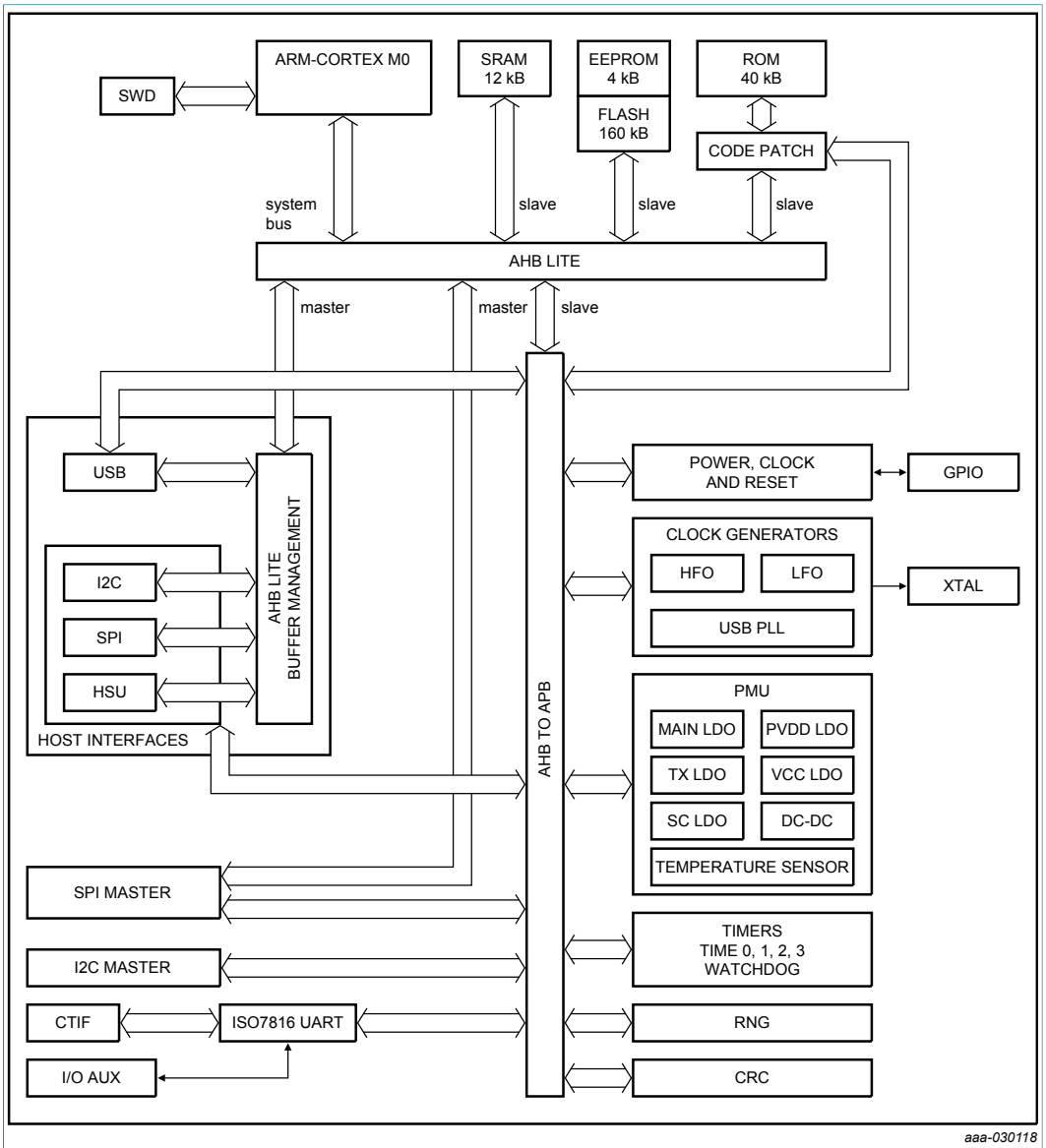


Figure 3. Block diagram

6.4 Block diagram PN736X

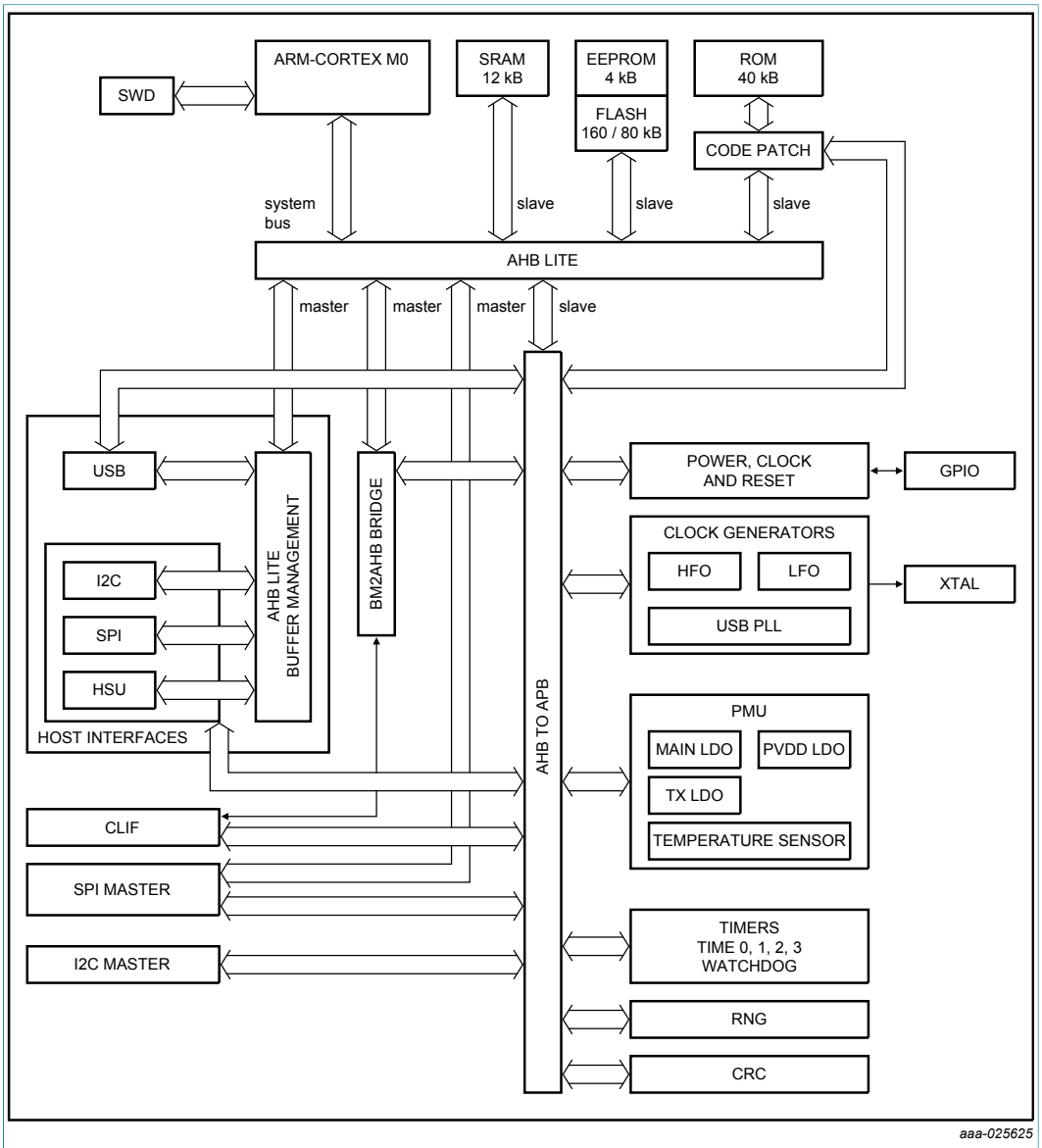
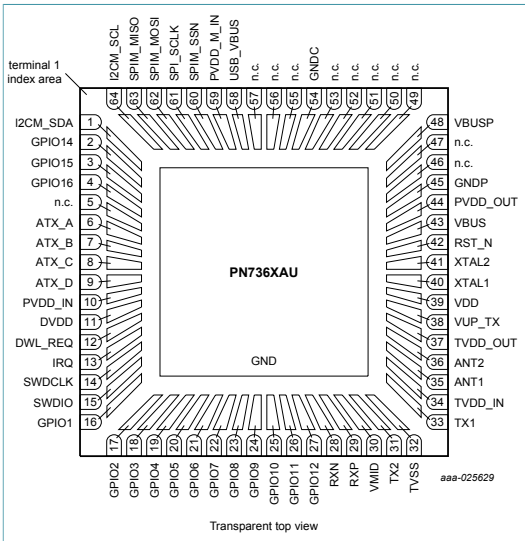


Figure 4. Block diagram

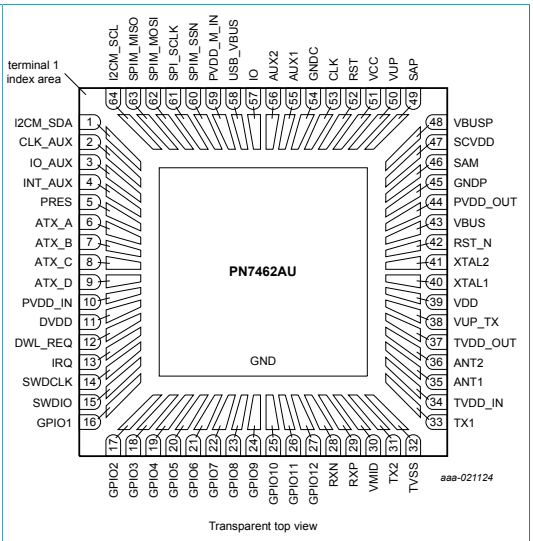
7 Pinning information

7.1 Pinning HVQFN64



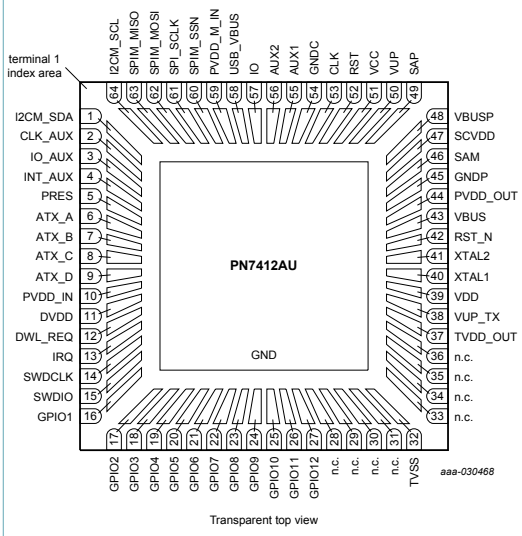
Transparent top view

Figure 5. Pin configuration PN736X



Transparent top view

Figure 6. Pin configuration PN7462



Transparent top view

Figure 7. Pin configuration PN7412

Important note: the inner leads below the package are internally connected to the PIN. Special care needs to be taken during the design so that no conductive part is present under these PINs, which could cause short cuts.

7.2 Pin description HVQFN64

Table 4. Pin description

Pin	Symbol PN736X	Description PN736X	Symbol PN7462	Description PN7462	Symbol PN7412	Description PN7412
1	I2CM_SDA	I^2C-bus serial data I/O master/GPIO13	I2CM_SDA	I^2C-bus serial data I/O master/GPIO13	I2CM_SDA	I^2C-bus serial data I/O master/GPIO13
2	CLK_AUX	GPIO14	CLK_AUX	auxiliary card contact clock/ GPIO14	CLK_AUX	auxiliary card contact clock/ GPIO14
3	IO_AUX	GPIO15	IO_AUX	auxiliary card contact I/O/ GPIO15	IO_AUX	auxiliary card contact I/O/ GPIO15
4	INT_AUX	GPIO16	INT_AUX	auxiliary card contact interrupt/GPIO16	INT_AUX	auxiliary card contact interrupt/GPIO16
5	n.c.	not connected	PRES	card presence	PRES	card presence
6	ATX_A	SPI slave select input (NSS_S)/I^2C-bus serial clock input (SCL_S)/ HSUART RX	ATX_A	SPI slave select input (NSS_S)/I^2C-bus serial clock input (SCL_S)/ HSUART RX	ATX_A	SPI slave select input (NSS_S)/I^2C-bus serial clock input (SCL_S)/ HSUART RX
7	ATX_B	SPI slave data input (MOSI_S)/I^2C-bus serial data I/O (SDA_S)/HSUART TX	ATX_B	SPI slave data input (MOSI_S)/I^2C-bus serial data I/O (SDA_S)/HSUART TX	ATX_B	SPI slave data input (MOSI_S)/I^2C-bus serial data I/O (SDA_S)/HSUART TX
8	ATX_C	USB D+/SPI slave data output (MISO_S)/I^2C-bus address bit0 input/HSUART RTS	ATX_C	USB D+/SPI slave data output (MISO_S)/I^2C-bus address bit0 input/HSUART RTS	ATX_C	USB D+/SPI slave data output (MISO_S)/I^2C-bus address bit0 input/HSUART RTS
9	ATX_D	USB D-/SPI clock input (SCK_S)/I^2C-bus address bit1 input/HSUART CTS	ATX_D	USB D-/SPI clock input (SCK_S)/I^2C-bus address bit1 input/HSUART CTS	ATX_D	USB D-/SPI clock input (SCK_S)/I^2C-bus address bit1 input/HSUART CTS
10	PVDD_IN	pad supply voltage input	PVDD_IN	pad supply voltage input	PVDD_IN	pad supply voltage input
11	DVDD	digital core logic supply voltage input	DVDD	digital core logic supply voltage input	DVDD	digital core logic supply voltage input
12	DWL_REQ	entering in download mode	DWL_REQ	entering in download mode	DWL_REQ	entering in download mode
13	IRQ	interrupt request output	IRQ	interrupt request output	IRQ	interrupt request output
14	SWDCLK	SW serial debug line clock	SWDCLK	SW serial debug line clock	SWDCLK	SW serial debug line clock
15	SWDIO	SW serial debug line input/ output	SWDIO	SW serial debug line input/ output	SWDIO	SW serial debug line input/ output
16	GPIO1	general-purpose I/O/SPI master select2 output	GPIO1	general-purpose I/O/SPI master select2 output	GPIO1	general-purpose I/O/SPI master select2 output
17	GPIO2	general-purpose I/O	GPIO2	general-purpose I/O	GPIO2	general-purpose I/O
18	GPIO3	general-purpose I/O	GPIO3	general-purpose I/O	GPIO3	general-purpose I/O
19	GPIO4	general-purpose I/O	GPIO4	general-purpose I/O	GPIO4	general-purpose I/O
20	GPIO5	general-purpose I/O	GPIO5	general-purpose I/O	GPIO5	general-purpose I/O

Pin	Symbol PN736X	Description PN736X	Symbol PN7462	Description PN7462	Symbol PN7412	Description PN7412
21	GPIO6	general-purpose I/O	GPIO6	general-purpose I/O	GPIO6	general-purpose I/O
22	GPIO7	general-purpose I/O	GPIO7	general-purpose I/O	GPIO7	general-purpose I/O
23	GPIO8	general-purpose I/O	GPIO8	general-purpose I/O	GPIO8	general-purpose I/O
24	GPIO9	general-purpose I/O	GPIO9	general-purpose I/O	GPIO9	general-purpose I/O
25	GPIO10	general-purpose I/O	GPIO10	general-purpose I/O	GPIO10	general-purpose I/O
26	GPIO11	general-purpose I/O	GPIO11	general-purpose I/O	GPIO11	general-purpose I/O
27	GPIO12	general-purpose I/O	GPIO12	general-purpose I/O	GPIO12	general-purpose I/O
28	RXN	receiver input	RXN	receiver input	n.c.	See UM10858 for connection details
29	RXP	receiver input	RXP	receiver input	n.c.	See UM10858 for connection details
30	VMID	receiver reference voltage input	VMID	receiver reference voltage input	n.c.	See UM10858 for connection details
31	TX2	antenna driver output	TX2	antenna driver output	n.c.	keep unconnected
32	TVSS	ground for antenna power supply	TVSS	ground for antenna power supply	TVSS	ground for antenna power supply
33	TX1	antenna driver output	TX1	antenna driver output	n.c.	keep unconnected
34	TVDD_IN	antenna driver supply voltage input	TVDD_IN	antenna driver supply voltage input	n.c.	Connect to GND
35	ANT1	antenna connection for load modulation in card emulation and P2P passive target modes	ANT1	antenna connection for load modulation in card emulation and P2P passive target modes	n.c.	See UM10858 for connection details
36	ANT2	antenna connection for load modulation in card emulation and P2P passive target modes	ANT2	antenna connection for load modulation in card emulation and P2P passive target modes	n.c.	See UM10858 for connection details
37	TVDD_OUT	antenna driver supply, output of TX_LDO	TVDD_OUT	antenna driver supply, output of TX_LDO	TVDD_OUT	antenna driver supply, output of TX_LDO
38	VUP_TX	supply of the contactless TX_LDO	VUP_TX	supply of the contactless TX_LDO	VUP_TX	supply of the contactless TX_LDO
39	VDD	1.8 V regulator output for digital blocks	VDD	1.8 V regulator output for digital blocks	VDD	1.8 V regulator output for digital blocks
40	XTAL1	27.12 MHz clock input for crystal	XTAL1	27.12 MHz clock input for crystal	XTAL1	27.12 MHz clock input for crystal
41	XTAL2	27.12 MHz clock input for crystal	XTAL2	27.12 MHz clock input for crystal	XTAL2	27.12 MHz clock input for crystal
42	RST_N	reset pin	RST_N	reset pin	RST_N	reset pin
43	VBUS	main supply voltage input of microcontroller	VBUS	main supply voltage input of microcontroller	VBUS	main supply voltage input of microcontroller
44	PVDD_OUT	output of PVDD_LDO for pad voltage supply	PVDD_OUT	output of PVDD_LDO for pad voltage supply	PVDD_OUT	output of PVDD_LDO for pad voltage supply
45	GNDP	Ground	GNDP	Ground	GNDP	Ground

Pin	Symbol PN736X	Description PN736X	Symbol PN7462	Description PN7462	Symbol PN7412	Description PN7412
46	n.c.	not connected	SAM	DC-to-DC converter connection	SAM	DC-to-DC converter connection
47	n.c.	not connected	SCVDD	input LDO for DC-to-DC converter	SCVDD	input LDO for DC-to-DC converter
48	VBUSP	Connected to VBUS	VBUSP	main supply for the contact interface	VBUSP	main supply for the contact interface
49	n.c.	not connected	SAP	DC-to-DC converter connection	SAP	DC-to-DC converter connection
50	n.c.	not connected	VUP	reserved; connected to GND through a decoupling capacitance	VUP	reserved; connected to GND through a decoupling capacitance
51	n.c.	not connected	VCC	card supply output of contact interface	VCC	card supply output of contact interface
52	n.c.	not connected	RST	reset pin of contact interface	RST	reset pin of contact interface
53	n.c.	not connected	CLK	clock pin of contact interface	CLK	clock pin of contact interface
54	GNDC	connected to the ground	GNDC	connected to the ground	GNDC	connected to the ground
55	n.c.	not connected	AUX1	C4 card I/O pin of contact interface	AUX1	C4 card I/O pin of contact interface
56	n.c.	not connected	AUX2	C8 card I/O pin of contact interface	AUX2	C8 card I/O pin of contact interface
57	n.c.	not connected	IO	card I/O	IO	card I/O
58	USB_VBUS	used for USB VBUS detection	USB_VBUS	used for USB VBUS detection	USB_VBUS	used for USB VBUS detection
59	PVDD_M_IN	pad supply voltage input for master interfaces	PVDD_M_IN	pad supply voltage input for master interfaces	PVDD_M_IN	pad supply voltage input for master interfaces
60	SPIM_SSN	SPI master select 1 output/ GPIO17	SPIM_SSN	SPI master select 1 output/ GPIO17	SPIM_SSN	SPI master select 1 output/ GPIO17
61	SPI_SCLK	SPI master clock output/ GPIO18	SPI_SCLK	SPI master clock output/ GPIO18	SPI_SCLK	SPI master clock output/ GPIO18
62	SPIM_MOSI	SPI master data output/ GPIO19	SPIM_MOSI	SPI master data output/ GPIO19	SPIM_MOSI	SPI master data output/ GPIO19
63	SPIM_MISO	SPI master data input/ GPIO20	SPIM_MISO	SPI master data input/ GPIO20	SPIM_MISO	SPI master data input/ GPIO20
64	I2CM_SCL	I^2C-bus serial clock output master/GPIO21	I2CM_SCL	I^2C-bus serial clock output master/GPIO21	I2CM_SCL	I^2C-bus serial clock output master/GPIO21
Die pad	GND	Ground	GND	Ground	GND	Ground

7.3 Pinning VFBGA64

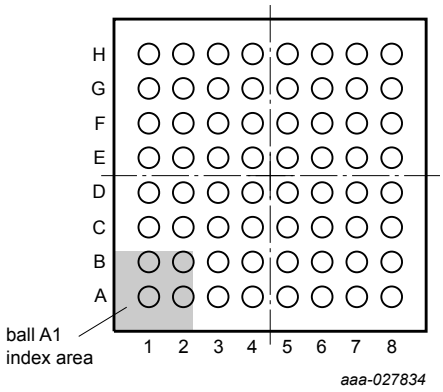


Figure 8. Pin configuration VFBGA64

7.4 Pin description VFBGA64

Table 5. Pin description

Pin	Symbol PN736X	Description PN736X	Symbol PN7462	Description PN7462
A1	I2CM_SDA	I^2C-bus serial data I/O master/GPIO13	I2CM_SDA	I^2C-bus serial data I/O master/GPIO13
A2	SPIM_MISO	SPI master data input/GPIO20	SPIM_MISO	SPI master data input/GPIO20
A3	PVDD_M_IN	pad supply voltage input for master interfaces	PVDD_M_IN	pad supply voltage input for master interfaces
A4	VBUSP	Connected to VBUS	VBUSP	Connected to VBUS
A5	VBUS	main supply voltage input of microcontroller	VBUS	main supply voltage input of microcontroller
A6	PVSS	Pad ground	PVSS	Pad ground
A7	PVDD_OUT	output of PVDD_LDO for pad voltage supply	PVDD_OUT	output of PVDD_LDO for pad voltage supply
A8	XTAL2	27.12 MHz clock input for crystal	XTAL2	27.12 MHz clock input for crystal
B1	INT_AUX	GPIO16	INT_AUX	auxiliary card contact interrupt/GPIO16
B2	ATX_A	SPI slave select input (NSS_S)/I^2C-bus serial clock input (SCL_S)/HSUART RX	ATX_A	SPI slave select input (NSS_S)/I^2C-bus serial clock input (SCL_S)/HSUART RX
B3	SPIM_MOSI	SPI master data output/GPIO19	SPIM_MOSI	SPI master data output/GPIO19
B4	SPIM_SSN	SPI master select 1 output/GPIO17	SPIM_SSN	SPI master select 1 output/GPIO17
B5	USB_VBUS	used for USB VBUS detection	USB_VBUS	used for USB VBUS detection
B6	PVSS	Pad ground	PVSS	Pad ground
B7	PVSS	Pad ground	PVSS	Pad ground
B8	XTAL1	27.12 MHz clock input for crystal	XTAL1	27.12 MHz clock input for crystal
C1	CLK_AUX	GPIO14	CLK_AUX	auxiliary card contact clock/GPIO14
C2	ATX_B	SPI slave data input (MOSI_S)/I^2C-bus serial data I/O (SDA_S)/HSUART TX	ATX_B	SPI slave data input (MOSI_S)/I^2C-bus serial data I/O (SDA_S)/HSUART TX

Pin	Symbol PN736X	Description PN736X	Symbol PN7462	Description PN7462
C3	I2CM_SCL	I^2C-bus serial clock output master/ GPIO21	I2CM_SCL	I^2C-bus serial clock output master/ GPIO21
C4	SPI_SCLK	SPI master clock output/GPIO18	SPI_SCLK	SPI master clock output/GPIO18
C5	DVSS	Digital ground	DVSS	Digital ground
C6	PVSS	Pad ground	PVSS	Pad ground
C7	RST_N	reset pin	RST_N	reset pin
C8	VDD	1.8 V regulator output for digital blocks	VDD	1.8 V regulator output for digital blocks
D1	PVDD_IN	pad supply voltage input	PVDD_IN	pad supply voltage input
D2	ATX_C	USB D+/SPI slave data output (MISO_S)/I^2C-bus address bit0 input/ HSUART RTS	ATX_C	USB D+/SPI slave data output (MISO_S)/I^2C-bus address bit0 input/ HSUART RTS
D3	IRQ	interrupt request output	IRQ	interrupt request output
D4	IO_AUX	GPIO15	IO_AUX	auxiliary card contact I/O/GPIO15
D5	DVSS	Digital ground	DVSS	Digital ground
D6	PVSS	Pad ground	PVSS	Pad ground
D7	PVSS	Pad ground	PVSS	Pad ground
D8	VUP_TX	supply of the contactless TX_LDO	VUP_TX	supply of the contactless TX_LDO
E1	DVDD	digital core logic supply voltage input	DVDD	digital core logic supply voltage input
E2	ATX_D	USB D-/SPI clock input (SCK_S)/I^2C-bus address bit1 input/HSUART CTS	ATX_D	USB D-/SPI clock input (SCK_S)/I^2C-bus address bit1 input/HSUART CTS
E3	GPIO1	general-purpose I/O/SPI master select2 output	GPIO1	general-purpose I/O/SPI master select2 output
E4	GPIO5	general-purpose I/O	GPIO5	general-purpose I/O
E5	DVSS	Digital ground	DVSS	Digital ground
E6	AVSS	Analog ground	AVSS	Analog ground
E7	ANT2	antenna connection for load modulation in card emulation and P2P passive target modes	ANT2	antenna connection for load modulation in card emulation and P2P passive target modes
E8	TVDD_OUT	antenna driver supply, output of TX_LDO	TVDD_OUT	antenna driver supply, output of TX_LDO
F1	DWL_REQ	entering in download mode	DWL_REQ	entering in download mode
F2	SWDIO	SW serial debug line input/output	SWDIO	SW serial debug line input/output
F3	GPIO6	general-purpose I/O	GPIO6	general-purpose I/O
F4	GPIO9	general-purpose I/O	GPIO9	general-purpose I/O
F5	GPIO12	general-purpose I/O	GPIO12	general-purpose I/O
F6	AVSS	Analog ground	AVSS	Analog ground
F7	ANT1	antenna connection for load modulation in card emulation and P2P passive target modes	ANT1	antenna connection for load modulation in card emulation and P2P passive target modes
F8	TVDD_IN	antenna driver supply voltage input	TVDD_IN	antenna driver supply voltage input

Pin	Symbol PN736X	Description PN736X	Symbol PN7462	Description PN7462
G1	SWDCLK	SW serial debug line clock	SWDCLK	SW serial debug line clock
G2	GPIO4	general-purpose I/O	GPIO4	general-purpose I/O
G3	GPIO7	general-purpose I/O	GPIO7	general-purpose I/O
G4	GPIO8	general-purpose I/O	GPIO8	general-purpose I/O
G5	GPIO10	general-purpose I/O	GPIO10	general-purpose I/O
G6	GPIO11	general-purpose I/O	GPIO11	general-purpose I/O
G7	AVSS	Analog ground	AVSS	Analog ground
G8	TX1	antenna driver output	TX1	antenna driver output
H1	GPIO3	general-purpose I/O	GPIO3	general-purpose I/O
H2	GPIO2	general-purpose I/O	GPIO2	general-purpose I/O
H3	VMID	receiver reference voltage input	VMID	receiver reference voltage input
H4	RXN	receiver input	RXN	receiver input
H5	RXP	receiver input	RXP	receiver input
H6	TVSS	Antenna driver ground	TVSS	Antenna driver ground
H7	TX2	antenna driver output	TX2	antenna driver output
H8	TVSS	Antenna driver ground	TVSS	Antenna driver ground

8 Functional description

8.1 ARM Cortex-M0 microcontroller

The PN7462 family is an ARM Cortex-M0-based 32-bit microcontroller, optimized for low-cost designs, high energy efficiency, and simple instruction set.

The CPU operates on an internal clock, which can be configured to provide frequencies such as 20 MHz, 10 MHz, and 5 MHz.

The peripheral complement of the PN7462 family includes a 160 kB flash memory, a 12 kB SRAM, and a 4 kB EEPROM. It also includes one configurable host interface (Fast-mode Plus and high-speed I^2C, SPI, HSUART, and USB), two master interfaces (Fast-mode Plus I^2C, SPI), 4 timers, 12 general-purpose I/O pins, one ISO/IEC 7816 contact card interface (PN7462AUHN only), one ISO/IEC 7816-3&4 UART (PN7462AUHN and PN7462AUEV only) and one 13.56 MHz contactless interface.

8.2 Memories

8.2.1 On-chip flash programming memory

The PN7462 family contains160 / 80 kB on-chip flash program memory depending on the version. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip boot loader software.

The flash memory is divided into two instances of 80 kB each, with each sector consisting of individual pages of 64 bytes.

8.2.1.1 Memory mapping

The flash memory mapping is described in Figure 9.

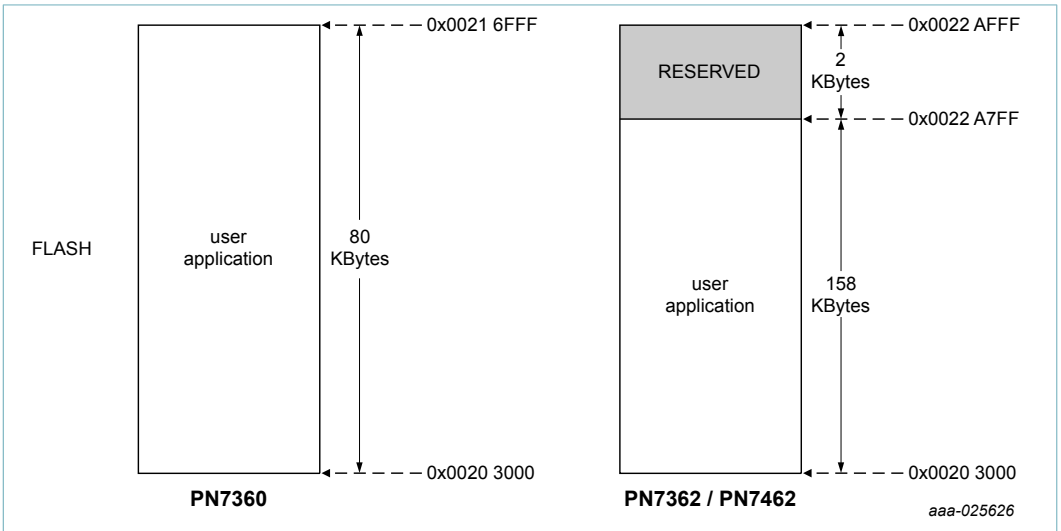


Figure 9. Flash memory mapping

8.2.2 EEPROM

The PN7462 family embeds 4 kB of on-chip byte-erasable and byte-programmable EEPROM data memory.

The EEPROM can be programmed using In-System Programming (ISP).

8.2.2.1 Memory mapping

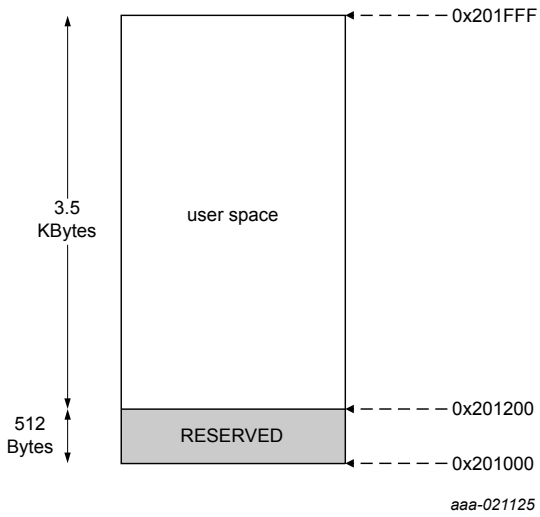


Figure 10. EEPROM memory mapping

8.2.3 SRAM

The PN7462 family contains a total of 12 kB on-chip static RAM memory.

8.2.3.1 Memory mapping

The SRAM memory mapping is shown in Figure 11.

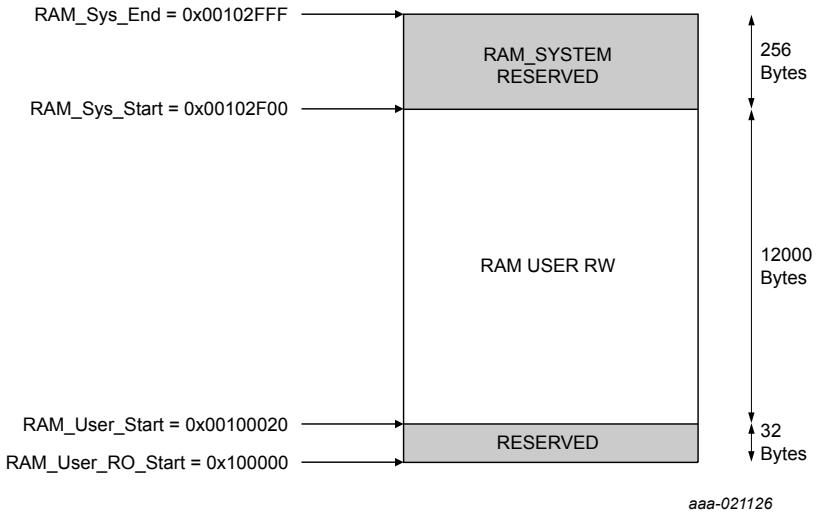


Figure 11. SRAM memory mapping

8.2.4 ROM

The PN7462 family contains 40 kB of on-chip ROM memory. The on-chip ROM contains boot loader, USB mass storage primary download, and the following Application Programming Interfaces (APIs):

- In-Application Programming (IAP) support for flash
- Lifecycle management of debug interface, code write protection of flash memory and USB mass storage primary download
- USB descriptor configuration
- Configuration of timeout and source of pad supply

8.2.5 Memory map

The PN7462 family incorporates several distinct memory regions. Figure 12 shows the memory map, from the user program perspective, following reset.

The APB peripheral area is 512 kB in size, and is divided to allow up to 32 peripherals. Only peripherals from 0 to 15 are accessible. Each peripheral allocates 16 kB, which simplifies the address decoding for the peripherals. APB memory map is described in Figure 13 and Figure 14.

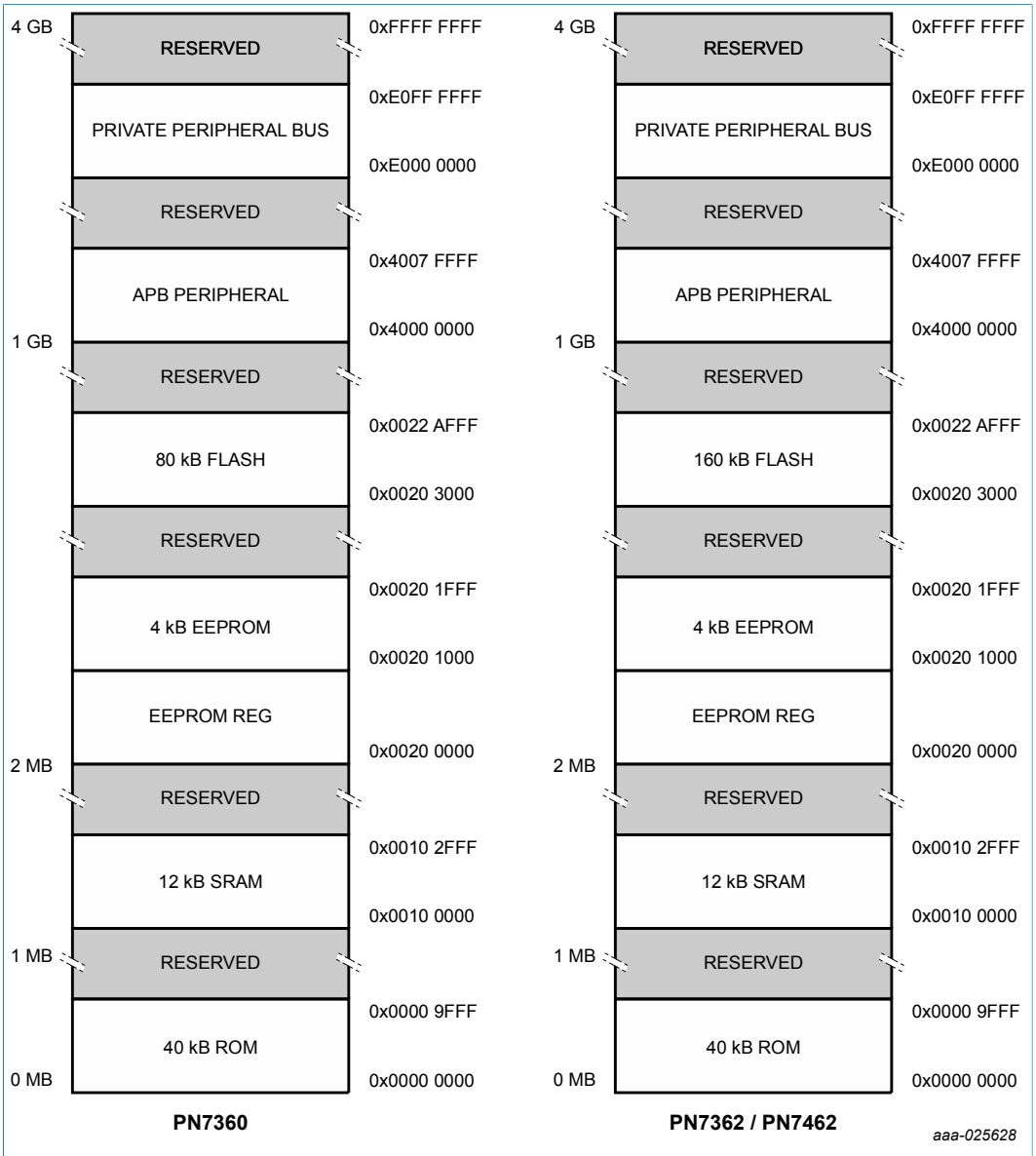


Figure 12. PN7462 family memory map

APB ID	APB IF name	Connected IP	
16 to 31	Reserved		0x4004 8000
15	Reserved		0x4004 0000
14	Reserved		0x4003 C000
13	SPIMASTER_APB	SPI Master IF	0x4003 8000
12	I2CMASTER_APB	I2C Master IF	0x4003 4000
11	Reserved		0x4003 0000
10	USB_APB	HostIF (USB) IP	0x4002 C000
9	PCR_APB	PowerClockResetModule IP	0x4002 8000
8	HOST_APB	HostIF (I2C/SPI/HSU/BufMgt) IP	0x4002 4000
7	TIMERS_APB	Timer IP	0x4002 0000
6	RNG_APB	RNG IP	0x4001 C000
5	Reserved		0x4001 8000
4	CLOCKGEN_APB	Clock Gen module	0x4001 4000
3	CRC_APB	CRC IP	0x4001 0000
2	PMU_APB	PMU modules	0x4000 C000
1	CL_APB	Contactless IP	0x4000 8000
0	Reserved		0x4000 4000
			0x4000 0000

aaa-021127

Figure 13. APB memory map PN736X

APB ID	APB IF name	Connected IP	
16 to 31	Reserved		0x4004 8000
15	Reserved		0x4004 0000
14	Reserved		0x4003 C000
13	SPIMASTER_APB	SPI Master IF	0x4003 8000
12	I2CMASTER_APB	I2C Master IF	0x4003 4000
11	Reserved		0x4003 0000
10	USB_APB	HostIF (USB) IP	0x4002 C000
9	PCR_APB	PowerClockResetModule IP	0x4002 8000
8	HOST_APB	HostIF (I2C/SPI/HSU/BufMgt) IP	0x4002 4000
7	TIMERS_APB	Timer IP	0x4002 0000
6	RNG_APB	RNG IP	0x4001 C000
5	CTUART_APB	Contact UART IP	0x4001 8000
4	CLOCKGEN_APB	Clock Gen module	0x4001 4000
3	CRC_APB	CRC IP	0x4001 0000
2	PMU_APB	PMU modules	0x4000 C000
1	CL_APB	Contactless IP	0x4000 8000
0	Reserved		0x4000 4000
			0x4000 0000

aaa-028697

Figure 14. APB memory map PN7462

APB ID	APB IF name	Connected IP	
16 to 31	Reserved		0x4004 8000
15	Reserved		0x4004 0000
14	Reserved		0x4003 C000
13	SPIMASTER_APB	SPI Master IF	0x4003 8000
12	I2CMASTER_APB	I2C Master IF	0x4003 4000
11	Reserved		0x4003 0000
10	USB_APB	HostIF (USB) IP	0x4002 C000
9	PCR_APB	PowerClockResetModule IP	0x4002 8000
8	HOST_APB	HostIF (I2C/SPI/HSU/BufMgt) IP	0x4002 4000
7	TIMERS_APB	Timer IP	0x4002 0000
6	RNG_APB	RNG IP	0x4001 C000
5	CTUART_APB	Contact UART IP	0x4001 8000
4	CLOCKGEN_APB	Clock Gen module	0x4001 4000
3	CRC_APB	CRC IP	0x4001 0000
2	PMU_APB	PMU modules	0x4000 C000
1	Reserved		0x4000 8000
0	Reserved		0x4000 4000
			0x4000 0000

aaa-030119

Figure 15. APB memory map PN7412

8.3 Nested Vectored Interrupt Controller (NVIC)

Cortex-M0 includes a Nested Vectored Interrupt Controller (NVIC). The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.3.1 NVIC features

- System exceptions and peripheral interrupts control
- Support 32 vectored interrupts
- Four interrupt priority levels with hardware priority level masking
- One Non-Maskable Interrupt (NMI) connected to the watchdog interrupt
- Software interrupt generation

8.3.2 Interrupt sources

The following table lists the interrupt sources available in the PN7462 family microcontroller.

Table 6. Interrupt sources

EIRQ#	Source	Description
0	timer 0/1/2/3	general-purpose timer 0/1/2/3 interrupt
1	-	reserved
2	CLIF	contactless interface module interrupt
3	EECTRL	EEPROM controller
4	-	reserved
5	-	reserved
6	host IF	TX or RX buffer from I^2C, SPI, HSU, or USB module