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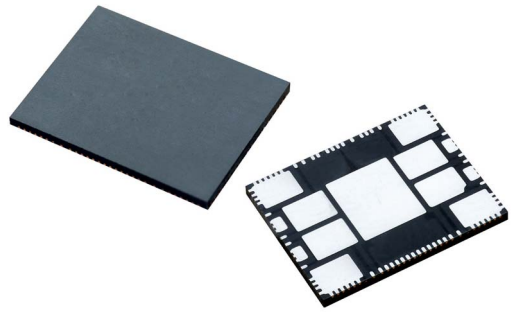
powerSTEP01

System-in-package integrating microstepping controller and 10 A power MOSFETs

Datasheet - production data



VFQFPN 11 x 14 mm

Features

- Power system-in-package integrating a programmable microstepping controller and 8 N-channel power MOSFETs.
- Operating voltage: 7.5 V - 85 V
- Dual full bridge with $R_{DS(on)}$ = 16 mΩ
- 10 $A_{r.m.s.}$ maximum output current
- Adjustable output slew rate
- Programmable speed profile
- Up to 1/128 microstepping
- Sensorless stall detection
- Integrated voltage regulators
- SPI interface
- Low quiescent standby currents
- Programmable non-dissipative overcurrent protection
- Overtemperature protection

Applications

- High power bipolar stepper motor
  - Stage lighting
  - Surveillance systems
  - Textile and sewing machines
  - Pick and place machines

Description

The powerSTEP01 is a a system-in-package integrating 8 N-channel 16 mΩ MOSFETs for stepper applications up to 85 V with a SPI programmable controller, providing fully digital control of the motion through a speed profile generation and positioning calculations.

It integrates a dual low $R_{DS(on)}$ full bridge with embedded non-dissipative overcurrent protection. The device can operate with both voltage mode driving and advanced current control fitting different application needs. The digital control core can generate user defined motion profiles with acceleration, deceleration, speed or a target position easily programmed through a dedicated register set. All application commands and data registers, including those used to set analog values (i.e. current protection trip point, deadtime, PWM frequency, etc.) are sent through a standard 5-Mbit/s SPI. A very rich set of protections (thermal, low bus voltage, overcurrent and motor stall) make the powerSTEP01 “bullet proof”, as required by the most demanding motor control applications.

Table 1. Device summary

Order code	Package	Packing
POWERSTEP01	VFQFPN 11 x 14 x 1.0 mm	Tray
POWERSTEP01TR	VFQFPN 11 x 14 x 1.0 mm	Tape and reel

Contents

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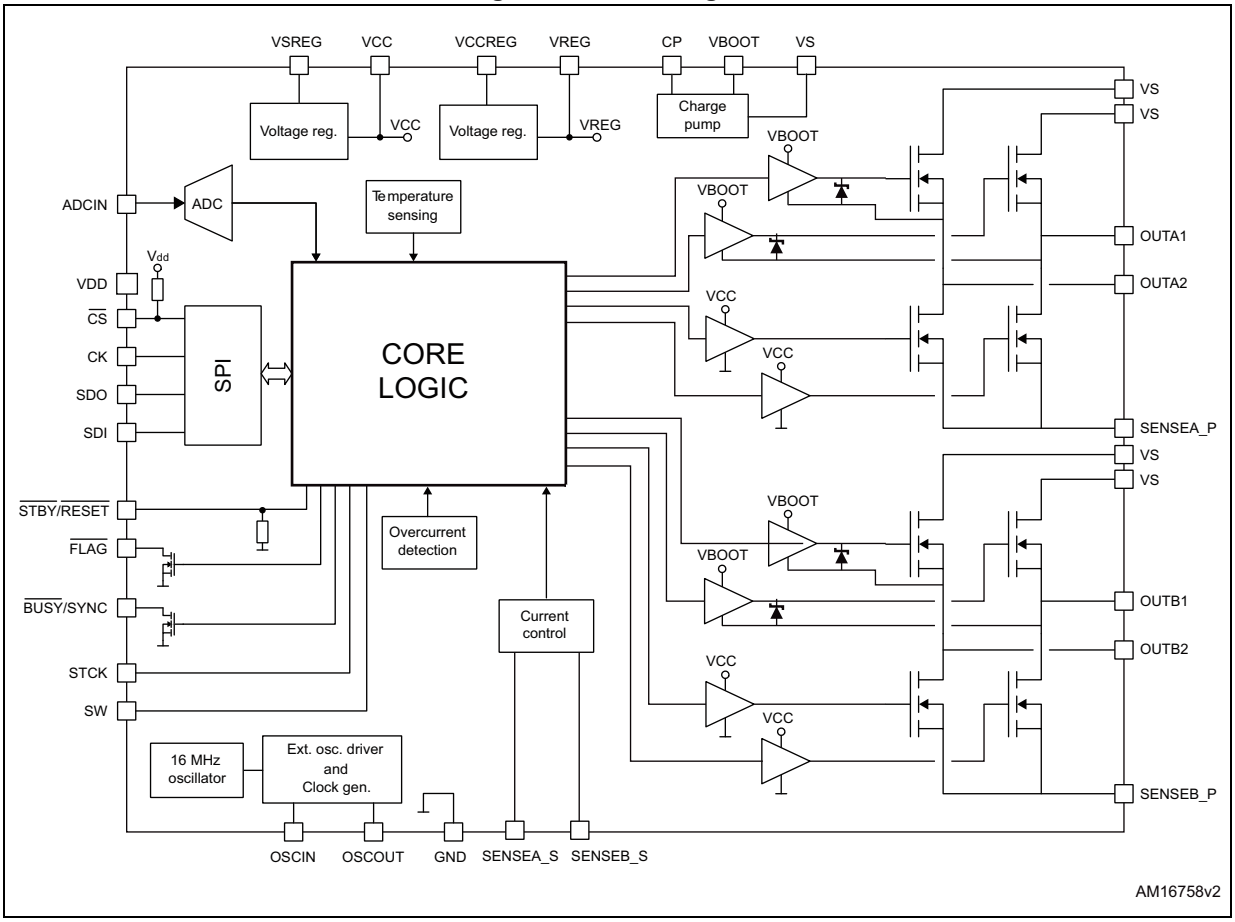
1 Block diagram

Figure 1. Block diagram



2 Electrical data

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Test conditions	Value	Unit
V_{DD}	Logic interface supply voltage		5.5	V
V_{REG}	Logic supply voltage		3.6	
V_S	Motor supply voltage		95	V
V_{CC}	Low-side gate driver supply voltage		18	V
V_{BOOT}	Boot voltage		100	V
ΔV_{BOOT}	High-side gate driver supply voltage (V_{BOOT} - V_S)		0 to 20	V
V_{SREG}	Internal V_{CC} regulator supply voltage		95	V
V_{CCREG}	Internal V_{REG} regulator supply voltage		18	V
V_{OUT1A} V_{OUT2A} V_{OUT1B} V_{OUT2B}	Output voltage	DC	-5 to V_{BOOT}	V
		AC	-15 to V_{BOOT}	
I_{OUT1A} I_{OUT2A} I_{OUT1B} I_{OUT2B}	Output current	DC	10	$A_{r.m.s.}$
SR_{out}	Full bridge output slew rate (10% - 90%)		10	V/ns
V_{ADCIN}	Integrated ADC input voltage range (ADCIN pin)		-0.3 to 3.6	V
V_{out_diff}	Differential voltage between VBOOT, VS, OUT1A, OUT2A, PGND and VBOOT, VS, OUT1B, OUT2B, PGND pins		100	V
V_{in}	Logic input voltage range		-0.3 to 5.5	V
T_{OP} T_s	Storage and operating junction temperature		-40 to 150	°C

2.2 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Logic interface supply voltage	3.3 V logic outputs		3.3		V
		5 V logic outputs		5		
V_{REG}	Logic supply voltage			3.3		V
V_S	Motor supply voltage		V_{SREG}		85	V
V_{SREG}	Internal V_{CC} voltage regulator supply voltage	V_{CC} voltage internally generated	V_{CC} +3		V_s	V
$V_{CC, ext}$	Gate driver supply voltage	V_{CC} voltage imposed by external source (V_{SREG} = V_{CC})	7.5		15	V
V_{CCREG}	Internal V_{REG} voltage regulator supply voltage	V_{REG} voltage internally generated	6.3		V_{CC}	V
V_{ADC}	Integrated ADC input voltage (ADCIN pin)		0		V_{REG}	V

3 Electrical characteristics

V_S = 48 V; V_{CC} = 7.5 V; V_{DD} = 3.3 V; T_j = 25 °C, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
General						
V_{CCthOn}	V_{CC} UVLO turn-on threshold	UVLO_VAL set high(1)	9.9	10.4	10.9	V
		UVLO_VAL set low(1)	6.5	6.9	7.3	V
$V_{CCthOff}$	V_{CC} UVLO turn-off threshold	UVLO_VAL set high(1)	9.5	10	10.5	V
		UVLO_VAL set low(1)	5.9	6.3	6.7	V
$\Delta V_{BOOTthOn}$	V_{BOOT} - V_S UVLO turn-on threshold	UVLO_VAL set high(1)	8.6	9.2	9.94	V
		UVLO_VAL set low(1)	5.7	6	6.35	V
$\Delta V_{BOOTthOff}$	V_{BOOT} - V_S UVLO turn-off threshold	UVLO_VAL set high(1)	8.2	8.8	9.65	V
		UVLO_VAL set low(1)	5.3	5.5	5.9	V
$V_{REGthOn}$	V_{REG} turn-on threshold	(1)	2.8	3	3.18	V
$V_{REGthOff}$	V_{REG} turn-off threshold	(1)	2.2	2.4	2.5	V
I_{VREGqu}	Undervoltage V_{REG} quiescent supply current	V_{CCREG} = V_{REG} < 2.2 V(1)		40		µA
I_{VREGq}	Quiescent V_{REG} supply current	V_{CCREG} = V_{REG} = 3.3 V internal oscillator selected(1)		3.8		mA
I_{VSREGq}	Quiescent V_{SREG} supply current	V_{CCREG} = V_{CC} = 15 V		6.5		mA
Thermal protection						
$T_{j(WRN)Set}$	Thermal warning temperature			135		°C
$T_{j(WRN)Rec}$	Thermal warning recovery temperature			125		°C
$T_{j(OFF)Set}$	Thermal bridge shutdown temperature			155		°C
$T_{j(OFF)Rec}$	Thermal bridge shutdown recovery temperature			145		°C
$T_{j(SD)Set}$	Thermal device shutdown temperature			170		°C
$T_{j(SD)Rec}$	Thermal device shutdown recovery temperature			130		°C
Charge pump						
V_{pump}	Voltage swing for charge pump oscillator			V_{CC}		V
$f_{pump,min}$	Minimum charge pump oscillator frequency(2)			660		kHz
$f_{pump,max}$	Maximum charge pump oscillator frequency(2)			800		kHz

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{pumpHS}	Charge pump high-side $R_{DS(on)}$ resistance			10		Ω
R_{pumpLS}	Charge pump low-side $R_{DS(on)}$ resistance			10		Ω
I_{boot}	Average boot current			2.6		mA
Power outputs						
$R_{DS(on)}$	High-side and low-side on resistance	V_{CC} = 15 V at 25 °C		16	21	mΩ
		At 125 °C		23		
SR_{OUT}	Output slew rate	IGATE = 96 mA		980		V/µs
		IGATE = 32 mA		520		
I_{DSS}	Leakage current	OUT = V_S			0.1	mA
		OUT = GND	-0.1			mA
Deadtime and blanking						
t_{DT}	Programmable deadtime[2]	TDT = '00000'		125		ns
		TDT =’11111’		4000		
t_{blank}	Programmable blanking time[2]	TBLANK = '000'		125		ns
		TBLANK =’111’		1000		
Logic						
V_{IL}	Low level logic input voltage				0.8	V
V_{IH}	High level logic input voltage		2			V
I_{IH}	High level logic input current	V_{IN} = 5 V, V_{DD} = 5 V			1	µA
I_{IL}	Low level logic input current	V_{IN} = 0 V, V_{DD} = 5 V	-1			µA
V_{OL}	Low level logic output voltage[(3)]	V_{DD} = 3.3 V, I_{OL} = 4 mA			0.3	V
		V_{DD} = 5 V, I_{OL} = 4 mA			0.3	
V_{OH}	High level logic output voltage	V_{DD} = 3.3 V, I_{OH} = 4 mA	2.4			V
		V_{DD} = 5 V, I_{OH} = 4 mA	4.7			
R_{PUCS}	CS pull-up resistor			430		kΩ
R_{PDRST}	STBY/RESET pull-down resistor			450		
R_{PUSW}	CS pull-up resistor			80		
$t_{high,STCK}$	Step-clock input high time		300			ns
$t_{low,STCK}$	Step-clock input low time		300			ns
Internal oscillator and external oscillator driver						
$f_{osc,int}$	Internal oscillator frequency	T_j = 25 °C	-5%	16	+5%	MHz
$f_{osc,ext}$	Programmable external oscillator frequency		8		32	MHz

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{OSCOUTH}$	OSCOUT clock source high level voltage	Internal oscillator	2.4			V
$V_{OSCOUTL}$	OSCOUT clock source low level voltage	Internal oscillator			0.3	V
$t_{rOSCOUT}$ $t_{fOSCOUT}$	OSCOUT clock source rise and fall time	Internal oscillator			10	ns
t_{high}	OSCOUT clock source high time	Internal oscillator		31.25		ns
t_{extosc}	Internal to external oscillator switching delay			3		ms
t_{intosc}	External to internal oscillator switching delay				100	µs
SPI						
$f_{CK,MAX}$	Maximum SPI clock frequency(4)		5			MHz
t_{rCK} t_{fCK}	SPI clock rise and fall time(4)				1	µs
t_{hCK} t_{lCK}	SPI clock high and low time(4)		90			ns
t_{setCS}	Chip select setup time(4)		30			ns
t_{holCS}	Chip select hold time(4)		30			ns
t_{disCS}	Deselect time(4)		625			ns
t_{setSDI}	Data input setup time(4)		20			ns
t_{holSDI}	Data input hold time(4)		30			ns
t_{enSDO}	Data output enable time(4)				95	ns
t_{disSDO}	Data output disable time(4)				95	ns
t_{vSDO}	Data output valid time(4)				35	ns
t_{holSDO}	Data output hold time(4)		0			ns
PWM modulators						
f_{PWM}	Programmable PWM frequency(2)	f_{osc} = 32 MHz F_PWM_INT='11X' F_PWM_DEC='000'		5.6		kHz
		f_{osc} = 32 MHz F_PWM_INT='000' F_PWM_DEC='111'		125		kHz
N_{PWM}	PWM resolution			8		bit
Current control						
$V_{REF, MAX}$	Maximum reference voltage			1000		mV
$V_{REF, MIN}$	Minimum reference voltage			7.8		mV

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Overcurrent protection						
V_{OCD}	Programmable overcurrent detection voltage V_{DS} threshold	OCD_TH = ‘00000’	27	31	35	mV
		OCD_TH = ‘01001’	270	312.5	344	mV
		OCD_TH = ‘10011’	500	625	688	mV
		OCD_TH = '11111'	800	1000	1100	mV
$t_{OCD,Comp}$	OCD comparator delay			100	200	ns
$t_{OCD,Flag}$	OCD to flag signal delay time			230	530	ns
$t_{OCD,SD}$	OCD to shutdown delay time	I_{gate} = 4 mA, t_{CC} = maximum		4200	6000	ns
Stall detection						
V_{STALL}	Programmable stall detection V_{DS} voltage threshold	STALL_TH = '11111'		1000		mV
		STALL_TH = '00000'		31		
Standby						
I_{STBY}	Standby mode supply current (VSREG pin)	V_{CC} = V_{CCREG} = 7.5 V V_{SREG} = 48 V		42		µA
		V_{CC} = V_{CCREG} = 7.5 V V_{SREG} = 18 V		37.5		
$I_{STBY,reg}$	Standby mode supply current (VREG pin)			6		µA
$t_{STBY,min}$	Minimum standby time			0.5		ms
$t_{logicwu}$	Logic power-on and wake-up time			500		µs
t_{cpwu}	Charge pump power-on and wake-up time	Power bridges disabled, C_p = 10 nF, C_{boot} = 220 nF, V_{CC} = 15 V		1		ms
Internal voltage regulators						
V_{CCOUT}	Internal V_{CC} voltage regulator output voltage	Low (default), I_{CC} = 10 mA	7.3	7.5		V
		High, I_{CC} = 10 mA	14	15		
$V_{SREG, drop}$	$V_{SREG\ to}$ V_{CC} dropout voltage	I_{CC} = 50 mA			3	V
P_{CC}	Internal V_{CC} voltage regulator power dissipation				2.5	W
V_{REGOUT}	Internal V_{REG} voltage regulator output voltage	I_{REG} = 10 mA	3.135	3.3		V
$V_{CCREG, drop}$	V_{CCREG} to V_{REG} dropout voltage	I_{REG} = 50 mA			3	V
I_{REGOUT}	Internal V_{REG} voltage regulator output current			125		mA

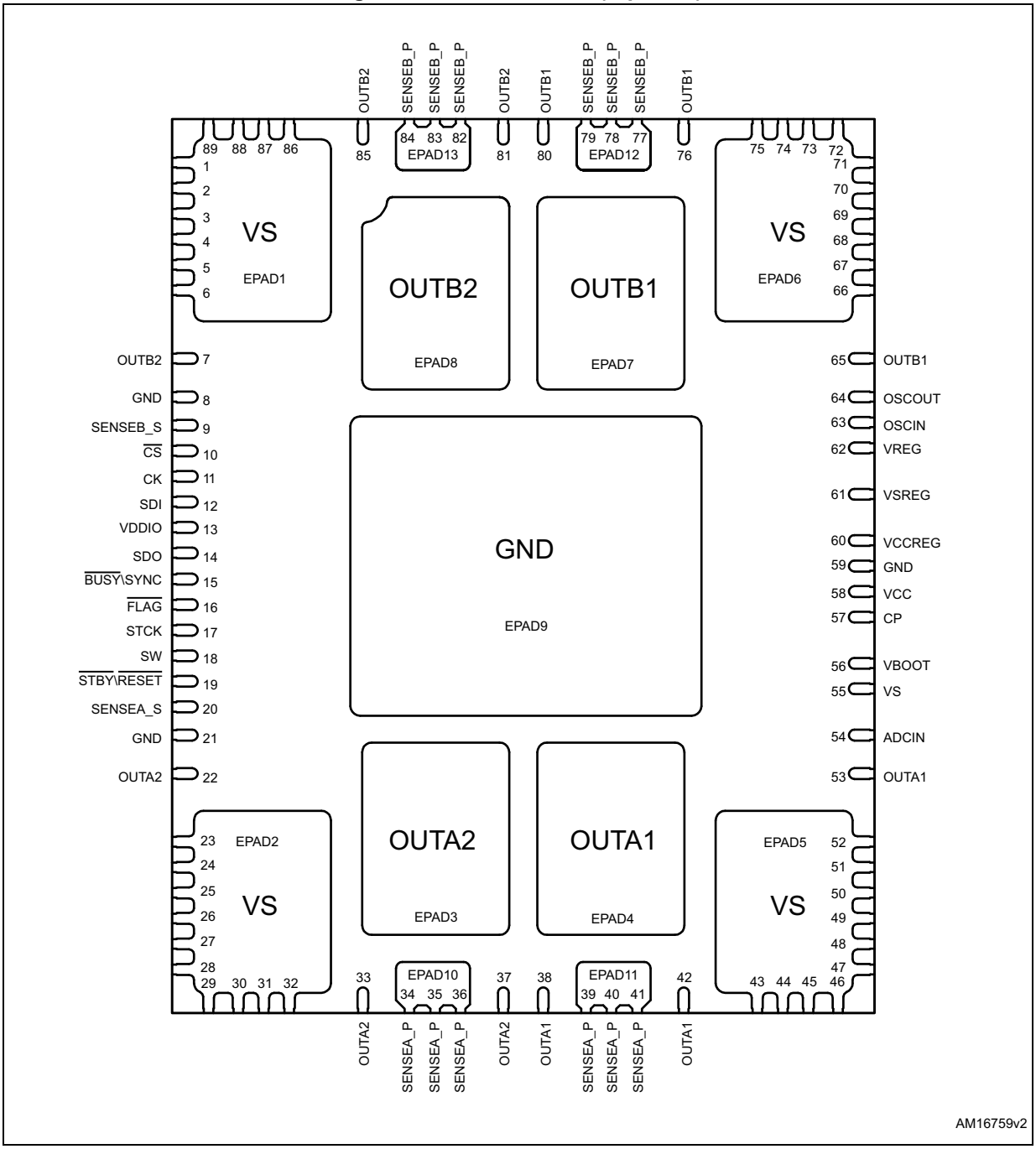
Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{REGOUT,STBY}$	Internal V_{REG} voltage regulator output standby current			55		mA
P_{REG}	Internal V_{REG} voltage regulator power dissipation				0.5	W
Integrated analog to digital converter						
N_{ADC}	Analog to digital converter resolution			5		bit
$V_{ADC,ref}$	Analog to digital converter reference voltage			3.3		V
f_S	Analog to digital converter sampling frequency	Voltage mode(2)		f_{PWM}		kHz
		Current mode(2)		$f_{OSC}/512$		kHz
$V_{ADC,UVLO}$	ADCIN UVLO threshold		1.05	1.16	1.35	V

1. Guaranteed in the temperature range -25 to 125 °C.
2. The value accuracy is dependent on oscillator frequency accuracy (*Section 7.8 on page 29*).
3. $\overline{\text{FLAG}}$ and $\overline{\text{BUSY}}$ open-drain outputs included.
4. See *Figure 25 on page 49*.

4 Pin connection

Figure 2. Pin connection (top view)



5 Pin list

Table 5. Pin description

No.	Name	Type	Function
1, 2, 3, 4, 5, 6, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 86, 87, 88, 89, EPAD1, EPAD2, EPAD5, EPAD6	VS	Supply	Motor supply voltage (drain of the high-side MOSFETs)
38, 42, 53, EPAD4	OUTA1	Power output	Half-bridge A1 output
22, 33, 37, EPAD3	OUTA2	Power output	Half-bridge A2 output
65, 76, 80, EPAD7	OUTB1	Power output	Half-bridge B1 output
7, 81, 85, EPAD8	OUTB2	Power output	Half-bridge B2 output
8, 21, 59, EPAD9	GND	Ground	Ground
34, 35, 36, 39, 40, 41, EPAD10, EPAD11	SENSEA_P	Sense (power)	Tail of full bridge A (source of the respective low-side MOSFETs)
20	SENSEA_S	Analog input	Current control comparator input
77, 78, 79, 82, 83, 84, EPAD12, EPAD13	SENSEB_P	Sense (power)	Tail of full bridge B (source of the respective low-side MOSFETs)
9	SENSEB_S	Analog input	Current control comparator input
60	VCCREG	Power supply	Internal V_{REG} voltage regulator supply voltage
62	VREG	Power supply	Logic supply voltage
13	VDDIO	Power supply	Logic interface supply voltage
61	VSREG	Power supply	Internal V_{CC} voltage regulator supply voltage
58	VCC	Power supply	Gate driver supply voltage
63	OSCIN	Analog input	Oscillator pin 1. To connect an external oscillator or clock source.
64	OSCOUT	Analog output	Oscillator pin 2. To connect an external oscillator. When the internal oscillator is used this pin can supply a 2/4/8/16 MHz clock.
57	CP	Output	Charge pump oscillator output
56	VBOOT	Power supply	Bootstrap voltage needed for driving the high-side power DMOS of both bridges (A and B).
54	ADCIN	Analog input	Internal analog to digital converter input
55	VS	Power supply	Motor supply voltage
18	SW	Logical input	External switch input pin
14	SDO	Logic output	Data output pin for serial interface

Table 5. Pin description (continued)

No.	Name	Type	Function
12	SDI	Logic input	Data input pin for serial interface
11	CK	Logic input	Serial interface clock
10	CS	Logic input	Chip select input pin for serial interface
15	BUSY /SYNC	Open-drain output	By default BUSY/SYNC pin is forced low when the device is performing a command. The pin can be programmed in order to generate a synchronization signal.
16	FLAG	Open-drain output	Status flag pin. An internal open-drain transistor can pull the pin to GND when a programmed alarm condition occurs (step loss, OCD, thermal pre-warning or shutdown, UVLO, wrong command, non performable command).
19	STBY /RESET	Logic input	Standby and reset pin. LOW logic level puts the device in standby mode and reset logic. If not used, should be connected to V_{REG}
17	STCK	Logic input	Step clock input.

6 Typical applications

Table 6. Typical application values

Name	Value
C_{VSPOL}	220 µF
C_{VS}	220 nF
C_{BOOT}	470 nF
C_{FLY}	47 nF
C_{VSREG}	100 nF
C_{VCC}	470 nF
C_{VCCREG}	100 nF
C_{VREG}	100 nF
$C_{VREGPOL}$	22 µF
C_{VDD}	100 nF
D1	Charge pump diodes
R_{PU}	39 kΩ
R_A	1.8 kΩ (V_S = 85 V)
R_B	91 kΩ (V_S = 85 V)
R_{SENSEA}	0.1 Ω (maximum I_{peak} = 10 A)
R_{SENSEB}	0.1 Ω (maximum I_{peak} = 10 A)

Figure 3. Typical application schematic - voltage mode

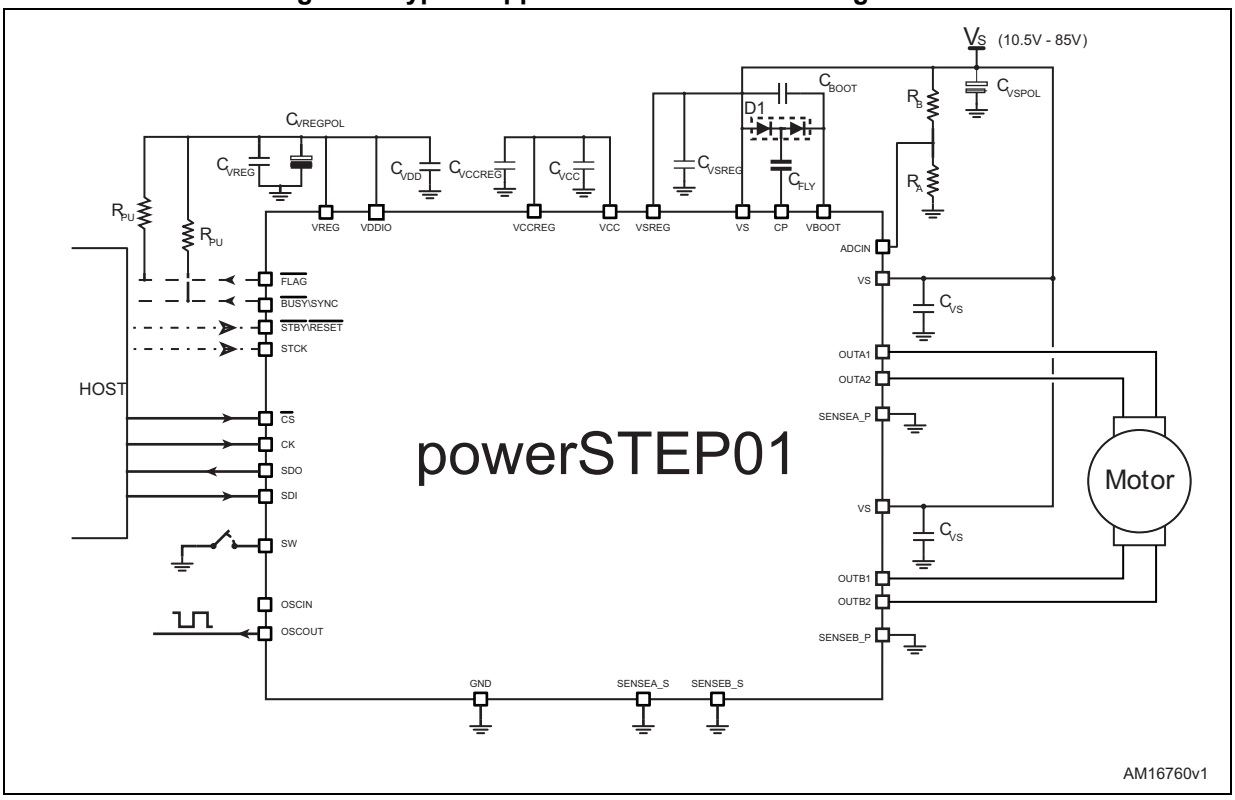
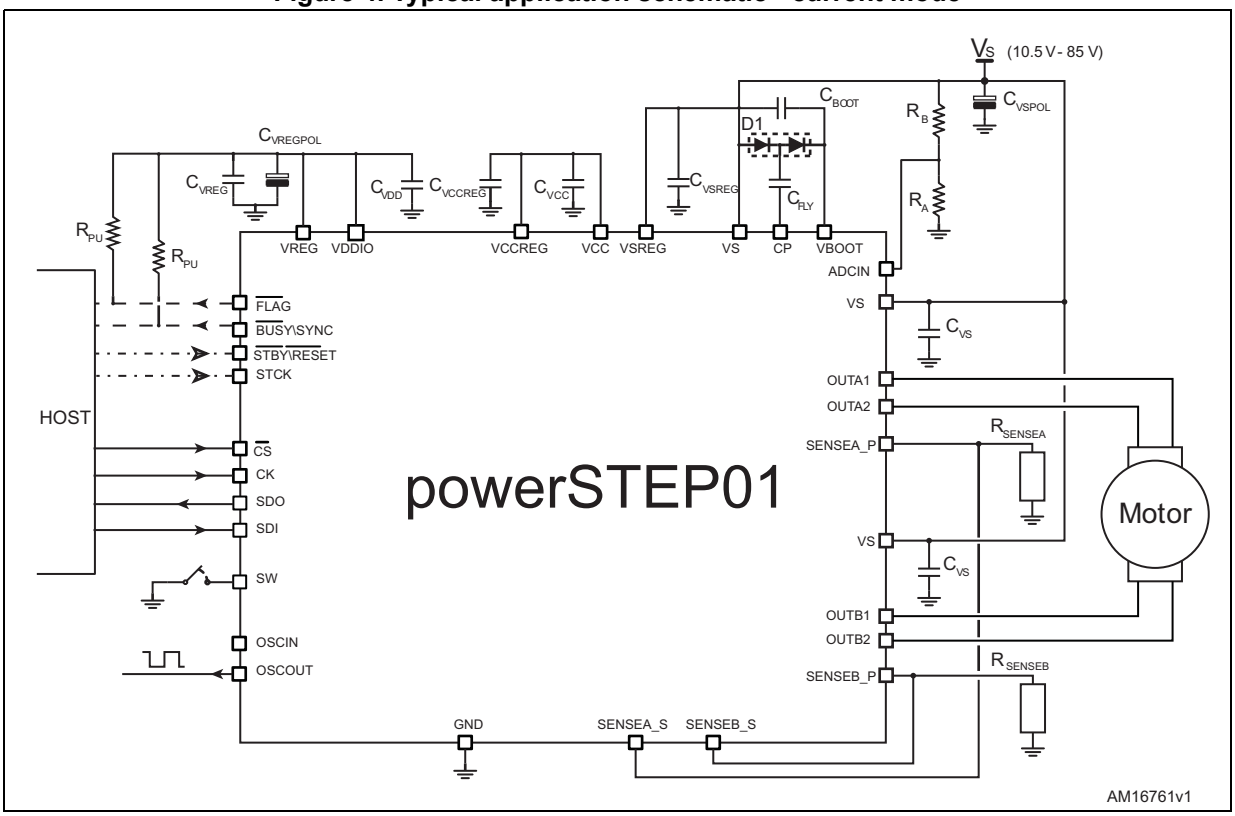


Figure 4. Typical application schematic - current mode



7 Functional description

7.1 Device power-up

During power-up, the device is under reset (all logic IOs disabled and power bridges in high impedance state) until the following conditions are satisfied:

- V_{REG} is greater than $V_{REGthOn}$
- Internal oscillator is operative
- $\overline{STBY}/\overline{RESET}$ input is forced high.

After power-up, the device state is the following:

- Parameters are set to default
- Internal logic is driven by internal oscillator and a 2-MHz clock is provided by the OSCOUT pin
- Bridges are disabled (high impedance).
- FLAG output is forced low (UVLO failure indication).

After power-up, a period of $t_{logicwu}$ must pass before applying a command to allow proper oscillator and logic startup.

Any movement command makes the device exit from High Z state (HardStop and SoftStop included).

7.2 Logic I/O

Pins $\overline{CS}$, CK, SDI, STCK, SW and $\overline{STBY}/\overline{RESET}$ are TTL/CMOS 3.3 V to 5 V compatible logic inputs.

Pin SDO is a TTL/CMOS compatible logic output. VDD pin voltage imposes logical output voltage range.

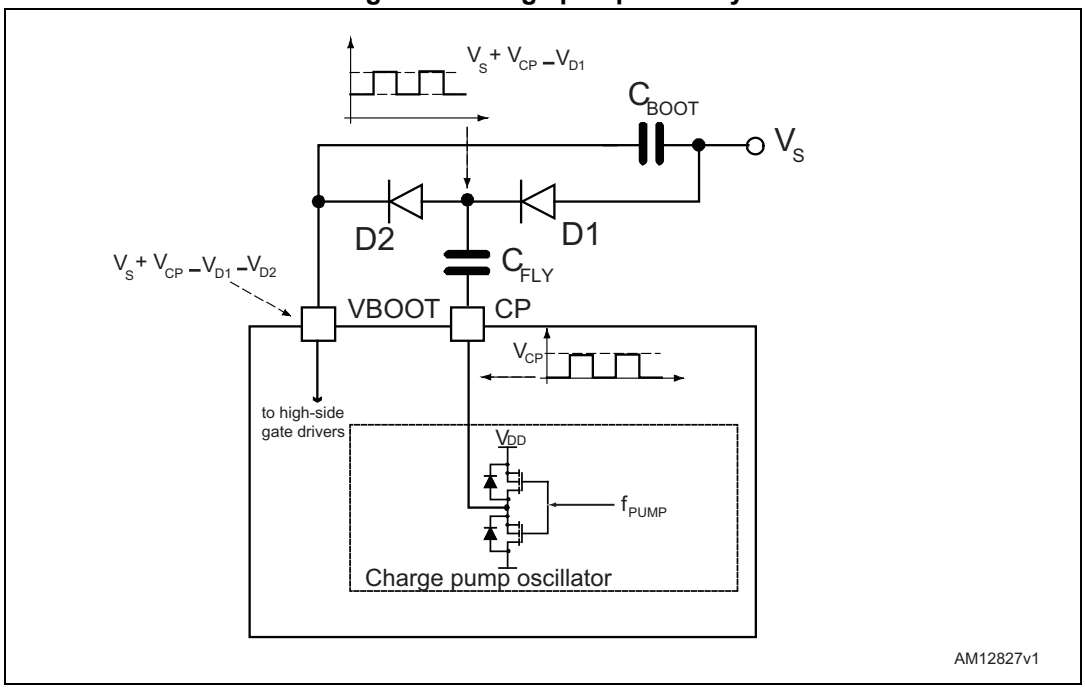
Pins $\overline{FLAG}$ and $\overline{BUSY}$/SYNC are open-drain outputs.

SW and $\overline{CS}$ inputs are internally pulled up to V_{DD} and $\overline{STBY}/\overline{RESET}$ input is internally pulled down to ground.

7.3 Charge pump

To ensure the correct driving of the high-side integrated MOSFETs, a voltage higher than the motor power supply voltage needs to be applied to the VBOOT pin. The high-side gate driver supply voltage V_{BOOT} is obtained through an oscillator and a few external components realizing a charge pump (see *Figure 5*).

Figure 5. Charge pump circuitry

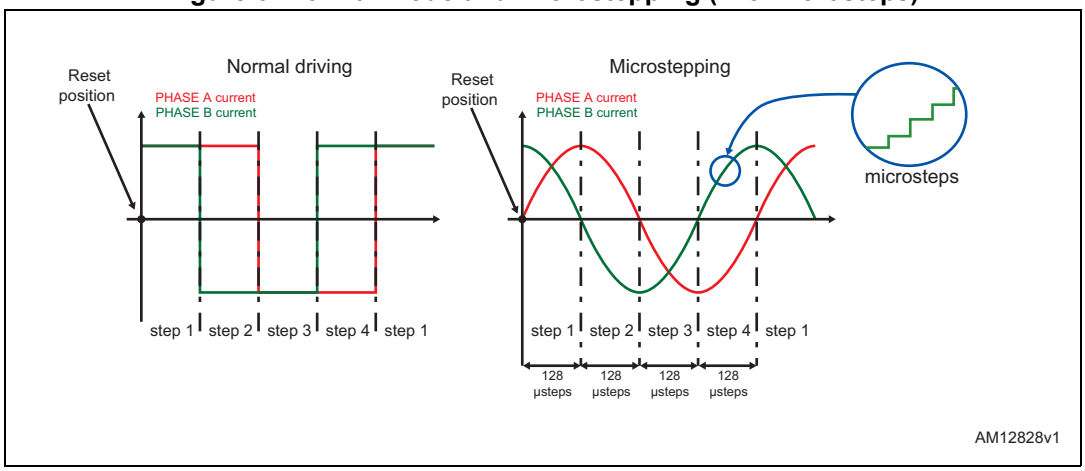


7.4 Microstepping

The driver is able to divide the single step into up to 128 microsteps. Stepping mode can be programmed by the STEP_SEL parameter in the STEP_MODE register (*Table 27 on page 61*). In current mode driving the maximum microstepping resolution is 1/16th of the step.

Step mode can only be changed when bridges are disabled. Every time the step mode is changed, the electrical position (i. e. the point of microstepping sinewave that is generated) is reset to zero and the absolute position counter value (*Section 7.5*) becomes meaningless.

Figure 6. Normal mode and microstepping (128 microsteps)



Automatic Full-step and Boost modes

When motor speed is greater than a programmable full-step speed threshold, the device switches automatically to Full-step mode; the driving mode returns to microstepping when motor speed decreases below the full-step speed threshold.

The switching between the microstepping and Full-step mode and vice-versa is always performed at an electrical position multiple of π/4 (*Figure 7* and *Figure 8*).

Full-step speed threshold is set through the related parameter in the FS_SPD register (*Section 11.1.9 on page 55*).

When the BOOST_MODE bit of the FS_SPD register is low (default), the amplitude of the voltage squarewave in Full-step mode is equal to the peak of the voltage sinewave multiplied by sine(π/4) (*Figure 7*). This avoids the current drop between the two driving modes.

When the BOOST_MODE bit of the FS_SPD register is high, the amplitude of the voltage squarewave in Full-step mode is equal to the peak of the voltage sinewave (*Figure 8*). That improves the output current increasing the maximum motor torque.

Figure 7. Automatic Full-step switching in Normal mode

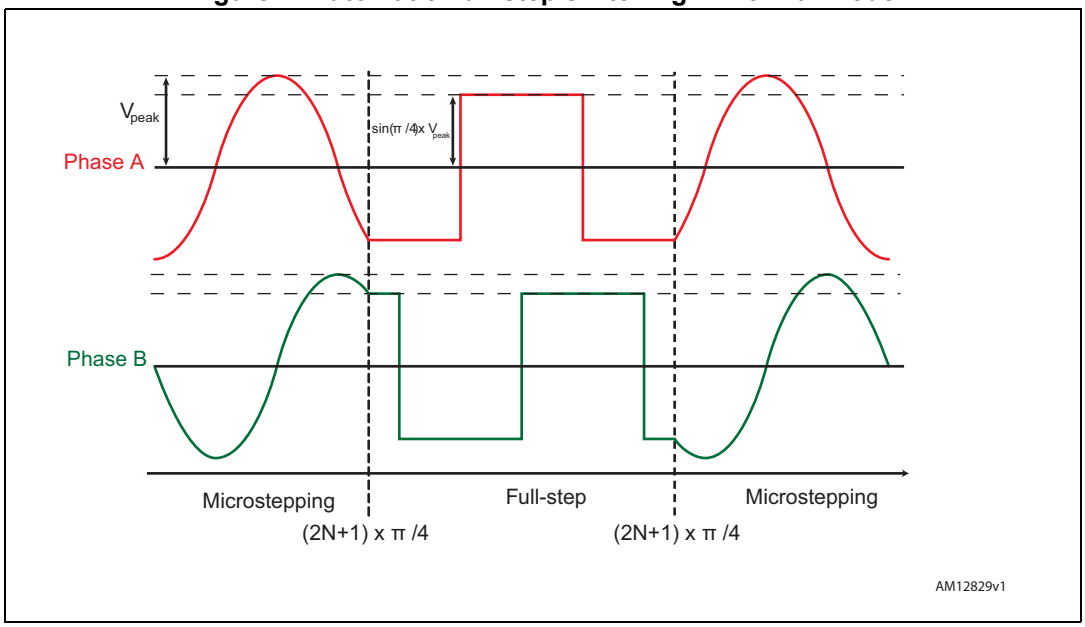
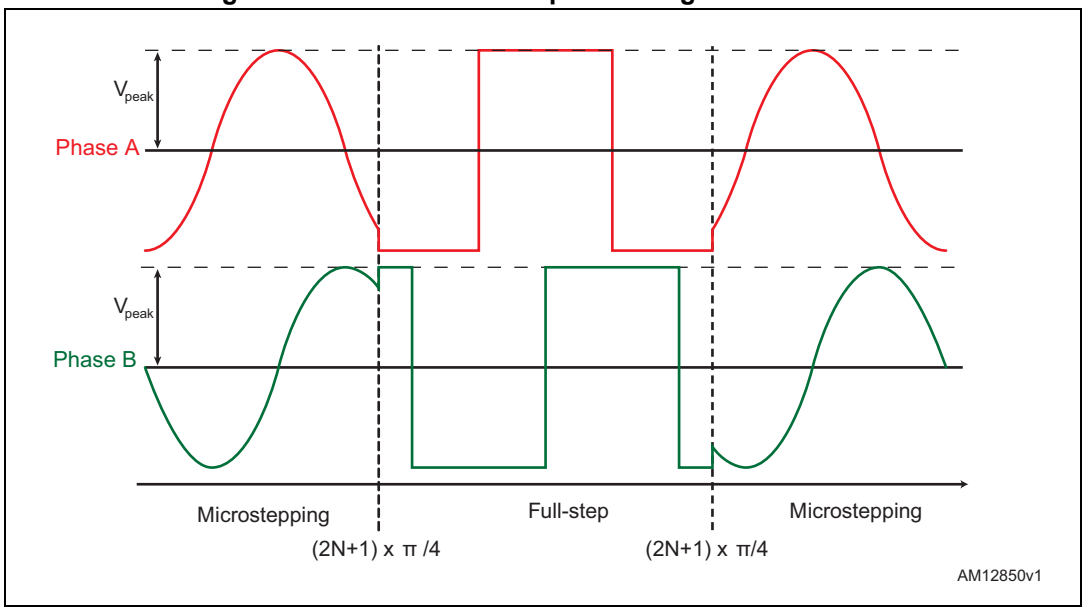


Figure 8. Automatic Full-step switching in Boost mode



7.5 Absolute position counter

An internal 22-bit register (ABS_POS) records all the motor motions according to the selected step mode; the stored value unit is equal to the selected step mode (full, half, quarter, etc.). The position range is from -2^{21} to $+2^{21}-1$ steps (see *Section 11.1.1 on page 53*).

7.6 Programmable speed profiles

The user can easily program a customized speed profile defining independently acceleration, deceleration, maximum and minimum speed values by ACC, DEC, MAX_SPEED and MIN_SPEED registers respectively (see *Section 11.1.5 on page 54*, *11.1.6 on page 54*, *11.1.7 on page 54* and *11.1.8 on page 55*).

When a command is sent to the device, the integrated logic generates the microstep frequency profile that performs a motor motion compliant to speed profile boundaries.

All acceleration parameters are expressed in step/tick^2 and all speed parameters are expressed in step/tick; the unit of measurement does not depend on the selected step mode. Acceleration and deceleration parameters range from 2^{-40} to $(2^{12}-2) \cdot 2^{-40}$ step/tick^2 (equivalent to 14.55 to 59590 step/s^2).

Minimum speed parameter ranges from 0 to $(2^{12}-1) \cdot 2^{-24}$ step/tick (equivalent to 0 to 976.3 step/s).

Maximum speed parameter ranges from 2^{-18} to $(2^{10}-1) \cdot 2^{-18}$ step/tick (equivalent to 15.25 to 15610 step/s).