



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



MPC8306S

PowerQUICC II Pro Integrated Communications Processor Family Hardware Specifications

This document provides an overview of the *MPC8306S* *PowerQUICC II Pro* processor features. The MPC8306S is a cost-effective, highly integrated communications processor that addresses the requirements of several networking applications, including residential gateways, modem/routers, industrial control, and test and measurement applications. The MPC8306S extends current PowerQUICC offerings, adding higher CPU performance, additional functionality, and faster interfaces, while addressing the requirements related to time-to-market, price, power consumption, and board real estate. This document describes the electrical characteristics of MPC8306S.

To locate published errata or updates for this document, refer to the MPC8306S product summary page on our website listed on the back cover of this document or contact your local Freescale sales office.

Contents

1. Overview	2
2. Electrical Characteristics	6
3. Power Characteristics	10
4. Clock Input Timing	11
5. RESET Initialization	12
6. DDR2 SDRAM	13
7. Local Bus	18
8. Ethernet and MII Management	21
9. TDM/SI	28
10. HDLC	29
11. USB	31
12. DUART	33
13. I ² C	34
14. Timers	36
15. GPIO	37
16. IPIC	38
17. SPI	38
18. JTAG	40
19. Package and Pin Listings	44
20. Clocking	54
21. Thermal	61
22. System Design Information	64
23. Ordering Information	67
24. Document Revision History	69

1 Overview

The MPC8306S incorporates the e300c3 (MPC603e-based) core built on Power Architecture® technology, which includes 16 Kbytes of each L1 instruction and data caches, dual integer units, and on-chip memory management units (MMUs). The MPC8306S also includes two DMA engines and a 16-bit DDR2 memory controller.

A new communications complex based on QUICC Engine technology forms the heart of the networking capability of the MPC8306S. The QUICC Engine block contains several peripheral controllers and a 32-bit RISC controller. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). A block diagram of the MPC8306S is shown in the following figure.

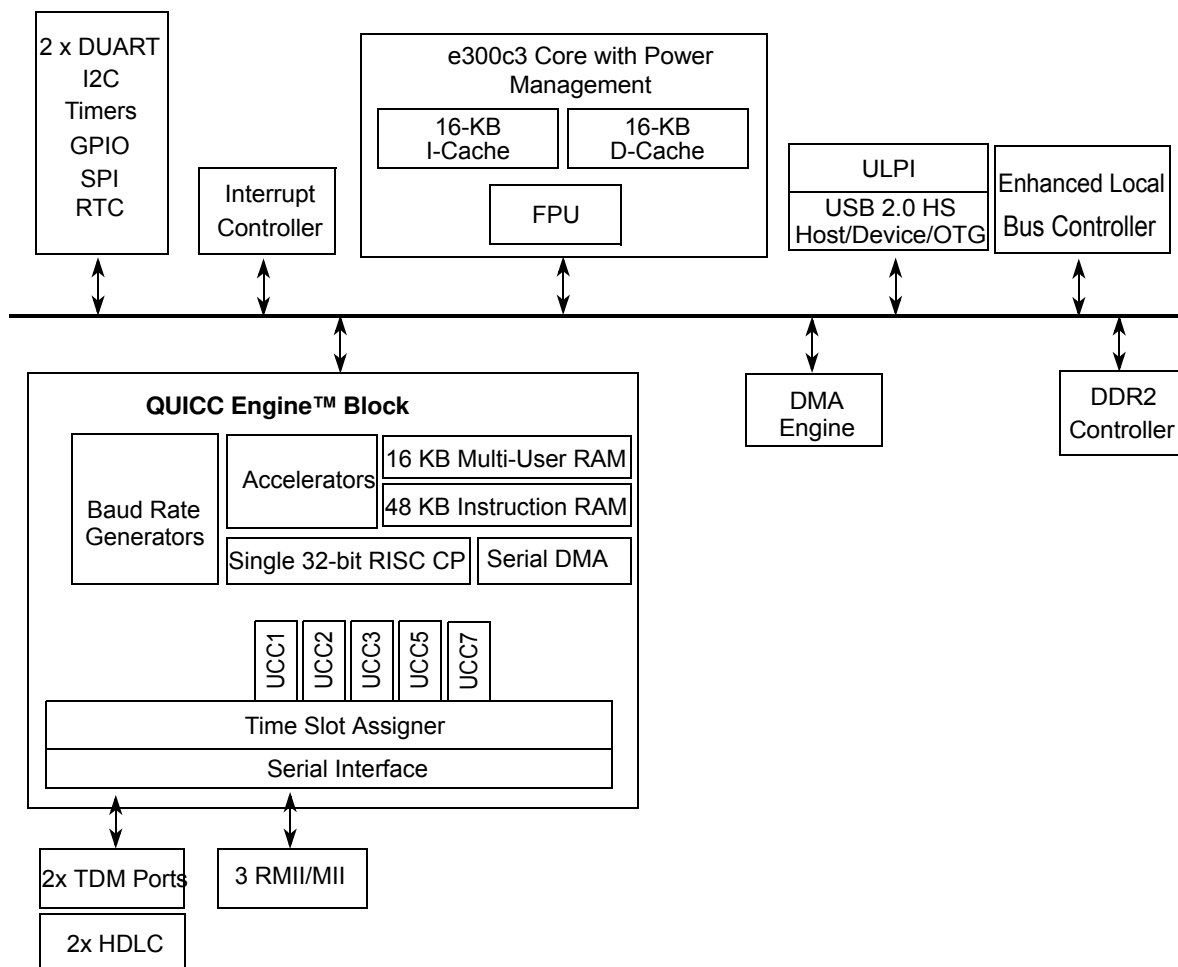


Figure 1. MPC8306S Block Diagram

Each of the five UCCs can support a variety of communication protocols such as 10/100 Mbps MII/RMII Ethernet, HDLC and TDM.

In summary, the MPC8306S provides users with a highly integrated, fully programmable communications processor. This helps to ensure that a low-cost system solution can be quickly developed and offers flexibility to accommodate new standards and evolving system requirements.

1.1 Features

The major features of the device are as follows:

- e300c3 Power Architecture processor core
 - Enhanced version of the MPC603e core
 - High-performance, superscalar processor core with a four-stage pipeline and low interrupt latency times
 - Floating-point, dual integer units, load/store, system register, and branch processing units
 - 16-Kbyte instruction cache and 16-Kbyte data cache with lockable capabilities
 - Dynamic power management
 - Enhanced hardware program debug features
 - Software-compatible with Freescale processor families implementing Power Architecture technology
 - Separate PLL that is clocked by the system bus clock
 - Performance monitor
- QUICC Engine block
 - 32-bit RISC controller for flexible support of the communications peripherals with the following features:
 - One clock per instruction
 - Separate PLL for operating frequency that is independent of system's bus and e300 core frequency for power and performance optimization
 - 32-bit instruction object code
 - Executes code from internal IRAM
 - 32-bit arithmetic logic unit (ALU) data path
 - Modular architecture allowing for easy functional enhancements
 - Slave bus for CPU access of registers and multiuser RAM space
 - 48 Kbytes of instruction RAM
 - 16 Kbytes of multiuser data RAM
 - Serial DMA channel for receive and transmit on all serial channels
 - Five unified communication controllers (UCCs) supporting the following protocols and interfaces:
 - 10/100 Mbps Ethernet/IEEE Std. 802.3® through MII and RMII interfaces.
 - HDLC/Transparent (bit rate up to QUICC Engine operating frequency / 8)
 - HDLC Bus (bit rate up to 10 Mbps)
 - Asynchronous HDLC (bit rate up to 2 Mbps)

- Two TDM interfaces supporting up to 128 QUICC multichannel controller channels, each running at 64 kbps

For more information on QUICC Engine sub-modules, see *QUICC Engine Block Reference Manual with Protocol Interworking*.

- DDR SDRAM memory controller
 - Programmable timing supporting DDR2 SDRAM
 - Integrated SDRAM clock generation
 - 16-bit data interface, up to 266-MHz data rate
 - 14 address lines
 - The following SDRAM configurations are supported:
 - Up to two physical banks (chip selects), 256-Mbyte per chip select for 16 bit data interface.
 - 64-Mbit to 2-Gbit devices with x8/x16 data ports (no direct x4 support)
 - One 16-bit device or two 8-bit devices on a 16-bit bus,
 - Support for up to 16 simultaneous open pages for DDR2
 - One clock pair to support up to 4 DRAM devices
 - Supports auto refresh
 - On-the-fly power management using CKE
- Enhanced local bus controller (eLBC)
 - Multiplexed 26-bit address and 8-/16-bit data operating at up to 66 MHz
 - Eight chip selects supporting eight external slaves
 - Four chip selects dedicated
 - Four chip selects offered as multiplexed option
 - Supports boot from parallel NOR Flash and parallel NAND Flash
 - Supports programmable clock ratio dividers
 - Up to eight-beat burst transfers
 - 16- and 8-bit ports, separate $\overline{\text{LWE}}$ for each 8 bit
 - Three protocol engines available on a per chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)
 - NAND Flash control machine (FCM)
 - Variable memory block sizes for FCM, GPCM, and UPM mode
 - Default boot ROM chip select with configurable bus width (8 or 16)
 - Provides two Write Enable signals to allow single byte write access to external 16-bit eLBC slave devices
- Integrated programmable interrupt controller (IPIC)
 - Functional and programming compatibility with the MPC8260 interrupt controller
 - Support for external and internal discrete interrupt sources
 - Programmable highest priority request

- Six groups of interrupts with programmable priority
- External and internal interrupts directed to host processor
- Unique vector number for each interrupt source
- Universal serial bus (USB) dual-role controller
 - Designed to comply with *Universal Serial Bus Revision 2.0 Specification*
 - Supports operation as a stand-alone USB host controller
 - Supports operation as a stand-alone USB device
 - Supports high-speed (480-Mbps), full-speed (12-Mbps), and low-speed (1.5-Mbps) operations. Low speed is only supported in host mode.
- Dual I²C interfaces
 - Two-wire interface
 - Multiple-master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
 - I²C1 can be used as the boot sequencer
- DMA Engine
 - Support for the DMA engine with the following features:
 - Sixteen DMA channels
 - All data movement via dual-address transfers: read from source, write to destination
 - Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
 - Channel activation via one of two methods (for both the methods, one activation per execution of the minor loop is required):
 - Explicit software initiation
 - Initiation via a channel-to-channel linking mechanism for continuous transfers (independent channel linking at end of minor loop and/or major loop)
 - Support for fixed-priority and round-robin channel arbitration
 - Channel completion reported via optional interrupt requests
 - Support for scatter/gather DMA processing
- DUART
 - Two 2-wire interfaces (RxD, TxD)
 - The same can be configured as one 4-wire interface (RxD, TxD, RTS, CTS)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Serial peripheral interface (SPI)
 - Master or slave support
- Power management controller (PMC)
 - Supports core doze/nap/sleep/ power management
 - Exits low power state and returns to full-on mode when
 - The core internal time base unit invokes a request to exit low power state

- The power management controller detects that the system is not idle and there are outstanding transactions on the internal bus or an external interrupt.
- Parallel I/O
 - General-purpose I/O (GPIO)
 - 56 parallel I/O pins multiplexed on various chip interfaces
 - Interrupt capability
- System timers
 - Periodic interrupt timer
 - Software watchdog timer
 - Eight general-purpose timers
- Real time clock (RTC) module
 - Maintains a one-second count, unique over a period of thousands of years
 - Two possible clock sources:
 - External RTC clock (RTC_PIT_CLK)
 - CSB bus clock
- IEEE Std. 1149.1™ compliant JTAG boundary scan

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8306S. The MPC8306S is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings¹

Characteristic	Symbol	Max Value	Unit	Notes
Core supply voltage	V _{DD}	–0.3 to 1.26	V	—
PLL supply voltage	AV _{DD1} AV _{DD2} AV _{DD3}	–0.3 to 1.26	V	—
DDR2 DRAM I/O voltage	GV _{DD}	–0.3 to 1.98	V	—
Local bus, DUART, system control and power management, I ² C, SPI, MII, RMII, MII management, USB and JTAG I/O voltage	OV _{DD}	–0.3 to 3.6	V	2

Table 1. Absolute Maximum Ratings¹ (continued)

Characteristic		Symbol	Max Value	Unit	Notes
Input voltage	DDR2 DRAM signals	MV_{IN}	-0.3 to ($GV_{DD} + 0.3$)	V	3
	DDR2 DRAM reference	MV_{REF}	-0.3 to ($GV_{DD} + 0.3$)	V	3
	Local bus, DUART, SYS_CLK_IN, system control and power management, I ² C, SPI, and JTAG signals	OV_{IN}	-0.3 to ($OV_{DD} + 0.3$)	V	4
Storage temperature range		T_{STG}	-55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in [Table 2](#). Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. OVDD here refers to NVDDA, NVDDB, NVDDC, NVDDF, NVDDG, and NVDDH from the ball map.
3. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
4. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.

2.1.2 Power Supply Voltage Specification

The following table provides the recommended operating conditions for the MPC8306S. Note that these values are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Note
Core supply voltage	V_{DD}	1.0 V \pm 50 mV	V	1
PLL supply voltage	AV_{DD1} AV_{DD2} AV_{DD3}	1.0 V \pm 50 mV	V	1
DDR2 DRAM I/O voltage	GV_{DD}	1.8 V \pm 100 mV	V	1
Local bus, DUART, system control and power management, I ² C, SPI, MII, RMII, MII management, USB and JTAG I/O voltage	OV_{DD}	3.3 V \pm 300 mV	V	1, 3
Junction temperature	T_A/T_J	0 to 105	°C	2

Notes:

1. GV_{DD} , OV_{DD} , AV_{DD} , and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. Minimum temperature is specified with T_A (Ambient Temperature); maximum temperature is specified with T_J (Junction Temperature).
3. OV_{DD} here refers to $NVDDA$, $NVddb$, $NVDDC$, $NVDDF$, $NVDDG$, and $NVDDH$ from the ball map.

The following figure shows the undershoot and overshoot voltages at the interfaces of the MPC8306S

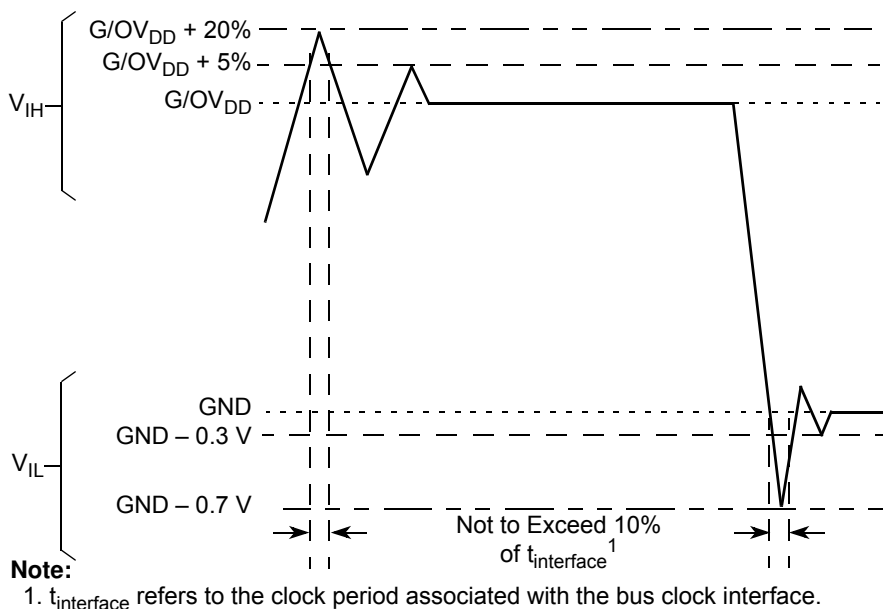


Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/OV_{DD}

2.1.3 Output Driver Characteristics

The following table provides information on the characteristics of the output driver strengths.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage (V)
Local bus interface utilities signals	42	$OV_{DD} = 3.3$
DDR2 signal	18	$GV_{DD} = 1.8$
DUART, system control, I2C, SPI, JTAG	42	$OV_{DD} = 3.3$
GPIO signals	42	$OV_{DD} = 3.3$

2.1.4 Input Capacitance Specification

The following table describes the input capacitance for the SYS_CLK_IN pin in the MPC8306S.

Table 4. Input Capacitance Specification

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input capacitance for all pins except SYS_CLK_IN and QE_CLK_IN	C_I	6	8	pF	—
Input capacitance for SYS_CLK_IN and QE_CLK_IN	$C_{I\text{CLK_IN}}$	10	—	pF	1

Note:

- The external clock generator should be able to drive 10 pF.

2.2 Power Sequencing

The device does not require the core supply voltage (V_{DD}) and I/O supply voltages (GV_{DD} and OV_{DD}) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD} and OV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see [Figure 3](#). Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating $\overline{\text{PORESET}}$.

NOTE

There is no specific power down sequence requirement for the device. I/O voltage supplies (GV_{DD} and OV_{DD}) do not have any ordering requirements with respect to one another.

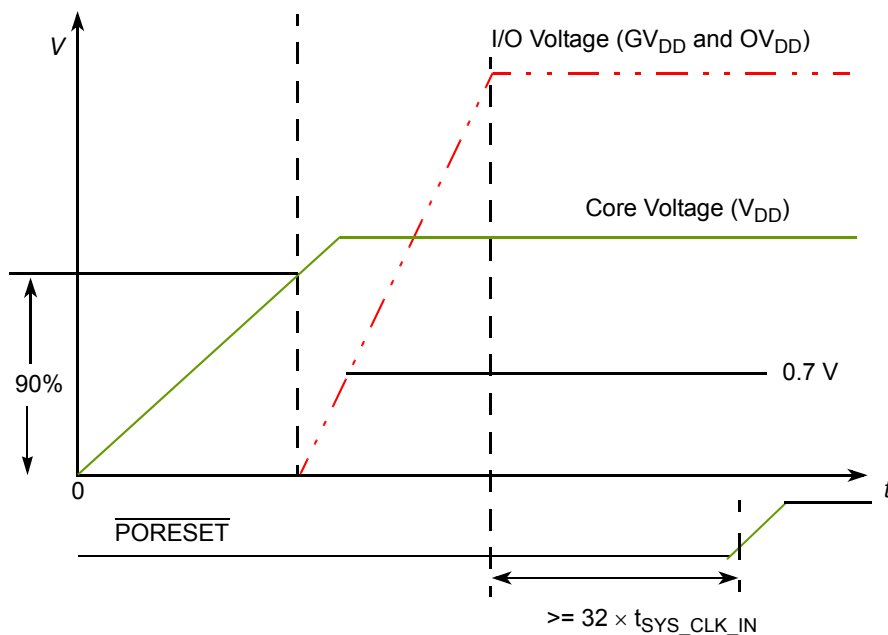


Figure 3. MPC8306S Power-Up Sequencing Example

3 Power Characteristics

The typical power dissipation for this family of MPC8306S devices is shown in the following table.

Table 5. MPC8306S Power Dissipation

Core Frequency (MHz)	QUICC Engine Frequency (MHz)	CSB Frequency (MHz)	Typical	Maximum	Unit	Note
133	133	133	0.272	0.618	W	1, 2, 3
200	233	133	0.291	0.631	W	1, 2, 3
266	233	133	0.451	0.925	W	1, 2, 3
333	233	133	0.471	0.950	W	1, 2, 3

Notes:

1. The values do not include I/O supply power (OV_{DD} and GV_{DD}), but it does include V_{DD} and AV_{DD} power. For I/O power values, see Table 6.
2. Typical power is based on a nominal voltage of $V_{DD} = 1.0$ V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the evaluation board using WC process silicon.
3. Maximum power is based on a voltage of $V_{DD} = 1.05$ V, WC process, a junction $T_J = 105^\circ\text{C}$, and a smoke test code.

The following table shows the estimated typical I/O power dissipation for the device.

Table 6. Typical I/O Power Dissipation

Interface	Parameter	$G_{V_{DD}}$ (1.8 V)	$O_{V_{DD}}$ (3.3 V)	Unit	Comments
DDR I/O 65% utilization 1.8 V $R_s = 20 \Omega$ $R_t = 50 \Omega$ 1 pair of clocks	266 MHz, 1×16 bits	0.141	—	W	—
Local bus I/O load = 25 pF 1 pair of clocks	66 MHz, 26 bits	—	0.150	W	1
QUICC Engine block and other I/Os	TDM serial, HDLC/TRAN serial, DUART, MII, RMII, Ethernet management, USB, SPI, Timer output,				

Note:

1. Typical I/O power is based on a nominal voltage of $V_{DD} = 3.3V$, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the evaluation board using WC process silicon.

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8306S.

NOTE

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of $O_{V_{DD}}$; fall time refers to transitions from 90% to 10% of $O_{V_{DD}}$.

4.1 DC Electrical Characteristics

The following table provides the clock input (SYS_CLK_IN) DC specifications for the MPC8306S. These specifications are also applicable for QE_CLK_IN.

Table 7. SYS_CLK_IN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.4	$O_{V_{DD}} + 0.3$	V
Input low voltage	—	V_{IL}	-0.3	0.4	V
SYS_CLK_IN input current	$0 V \leq V_{IN} \leq O_{V_{DD}}$	I_{IN}	—	± 5	μA
SYS_CLK_IN input current	$0 V \leq V_{IN} \leq 0.5 V$ or $O_{V_{DD}} - 0.5 V \leq V_{IN} \leq O_{V_{DD}}$	I_{IN}	—	± 5	μA
SYS_CLK_IN input current	$0.5 V \leq V_{IN} \leq O_{V_{DD}} - 0.5 V$	I_{IN}	—	± 50	μA

4.2 AC Electrical Characteristics

The primary clock source for the MPC8306S is SYS_CLK_IN. The following table provides the clock input (SYS_CLK_IN) AC timing specifications for the MPC8306S. These specifications are also applicable for QE_CLK_IN.

Table 8. SYS_CLK_IN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
SYS_CLK_IN frequency	$f_{\text{SYS_CLK_IN}}$	24	—	66.67	MHz	1
SYS_CLK_IN cycle time	$t_{\text{SYS_CLK_IN}}$	15	—	41.6	ns	—
SYS_CLK_IN rise and fall time	$t_{\text{KH}}, t_{\text{KL}}$	1.1	—	2.8	ns	2
SYS_CLK_IN duty cycle	$t_{\text{KHK}}/t_{\text{SYS_CLK_IN}}$	40	—	60	%	3
SYS_CLK_IN jitter	—	—	—	±150	ps	4, 5

Notes:

- Caution:** The system, core and QUICC Engine block must not exceed their respective maximum or minimum operating frequencies.
- Rise and fall times for SYS_CLK_IN are measured at 0.33 and 2.97 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- The SYS_CLK_IN driver's closed loop jitter bandwidth should be < 500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.
- Spread spectrum is allowed up to 1% down-spread @ 33kHz (max rate).

5 RESET Initialization

This section describes the AC electrical specifications for the reset initialization timing requirements of the MPC8306S. The following table provides the reset initialization AC timing specifications for the reset component(s).

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ to activate reset flow	32	—	$t_{\text{SYS_CLK_IN}}$	1
Required assertion time of PORESET with stable clock applied to SYS_CLK_IN	32	—	$t_{\text{SYS_CLK_IN}}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{\text{SYS_CLK_IN}}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3]) with respect to negation of $\overline{\text{PORESET}}$	4	—	$t_{\text{SYS_CLK_IN}}$	1, 2
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	1, 2

Notes:

- $t_{\text{SYS_CLK_IN}}$ is the clock period of the input clock applied to SYS_CLK_IN. For more details, see the *MPC8306S PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*.
- POR configuration signals consist of CFG_RESET_SOURCE[0:3].

The following table provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

5.1 Reset Signals DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8306S reset signals mentioned in [Table 9](#).

Table 11. Reset Signals DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Output high voltage	V_{OH}	$I_{OH} = -6.0 \text{ mA}$	2.4	—	V	1
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V	1
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V	1
Input low voltage	V_{IL}	—	-0.3	0.8	V	—
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	±5	μA	—

Note:

1. This specification applies when operating from 3.3 V supply.

6 DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR2 SDRAM interface of the MPC8306S. Note that DDR2 SDRAM is $GV_{DD}(\text{typ}) = 1.8 \text{ V}$.

6.1 DDR2 SDRAM DC Electrical Characteristics

The following table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8306S when $GV_{DD}(\text{typ}) = 1.8 \text{ V}$.

Table 12. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}(\text{typ}) = 1.8 \text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MVREF	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MVREF - 0.04$	$MVREF + 0.04$	V	3
Input high voltage	V_{IH}	$MVREF + 0.125$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MVREF - 0.125$	V	—
Output leakage current	I_{OZ}	-9.9	9.9	μA	4

Table 12. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}(typ) = 1.8\text{ V}$ (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Note
Output high current ($V_{OUT} = 1.35\text{ V}$)	I_{OH}	-13.4	—	mA	—
Output low current ($V_{OUT} = 0.280\text{ V}$)	I_{OL}	13.4	—	mA	—

Notes:

- GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
- MVREF is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed $\pm 2\%$ of the DC value.
- V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
- Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.

The following table provides the DDR2 capacitance when $GV_{DD}(typ) = 1.8\text{ V}$.

Table 13. DDR2 SDRAM Capacitance for $GV_{DD}(typ) = 1.8\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

- This parameter is sampled. $GV_{DD} = 1.8\text{ V} \pm 0.100\text{ V}$, $f = 1\text{ MHz}$, $T_A = 25\text{ }^\circ\text{C}$, $V_{OUT} = GV_{DD} \div 2$, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR2 SDRAM interface.

6.2.1 DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM ($GV_{DD}(typ) = 1.8\text{ V}$).

Table 14. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of $1.8\text{ V} \pm 100\text{ mV}$.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MVREF - 0.25	V	—
AC input high voltage	V_{IH}	MVREF + 0.25	—	V	—

The following table provides the input AC timing specifications for the DDR2 SDRAM interface.

Table 15. DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of $1.8\text{ V} \pm 100\text{ mV}$.

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS—MDQ/MDM	t_{CISKEW}			ps	1, 2

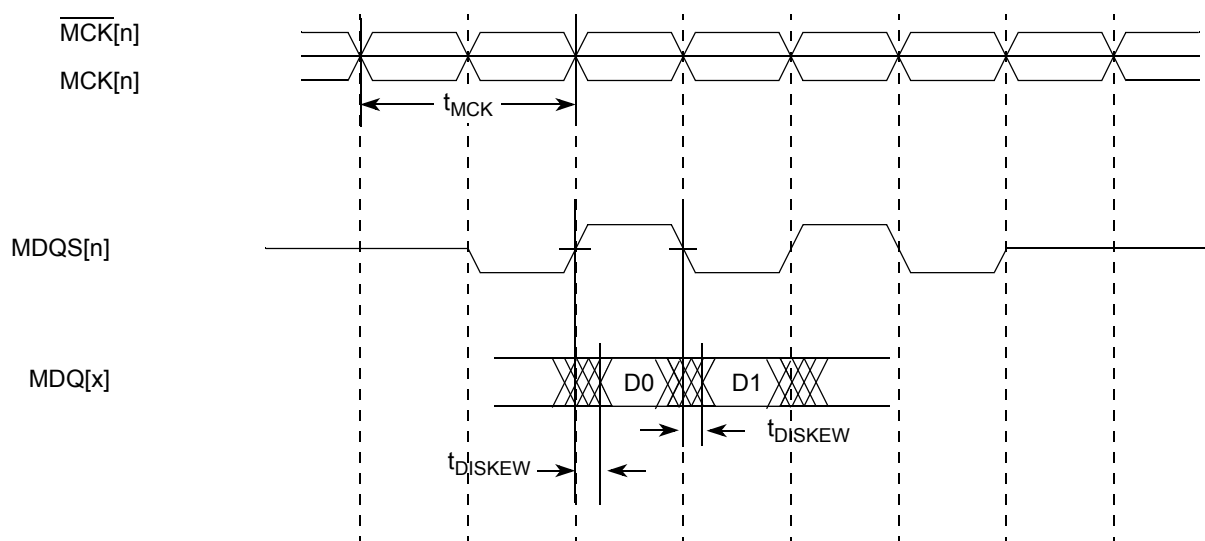
Table 15. DDR2 SDRAM Input AC Timing Specifications (continued)At recommended operating conditions with GV_{DD} of $1.8V \pm 100mV$.

Parameter	Symbol	Min	Max	Unit	Note
266 MHz		-750	750		

Notes:

- t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
- The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the equation: $t_{DISKEW} = \pm(T/4 - \text{abs}(t_{CISKEW}))$ where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} .

The following figure shows the input timing diagram for the DDR controller.

**Figure 4. DDR Input Timing Diagram****6.2.2 DDR2 SDRAM Output AC Timing Specifications**

The following table provides the output AC timing specifications for the DDR2 SDRAM interfaces.

Table 16. DDR2 SDRAM Output AC Timing SpecificationsAt recommended operating conditions with GV_{DD} of $1.8V \pm 100mV$.

Parameter	Symbol ¹	Min	Max	Unit	Note
MCK cycle time, (MCK/ $\overline{\text{MCK}}$ crossing)	t_{MCK}	5.988	8	ns	2
ADDR/CMD output setup with respect to MCK 266 MHz	t_{DDKHAS}	2.5	—	ns	3
ADDR/CMD output hold with respect to MCK 266 MHz	t_{DDKHAX}	2.5	—	ns	3
$\overline{\text{MCS}}$ output setup with respect to MCK 266 MHz	t_{DDKHCS}	2.5	—	ns	3

Table 16. DDR2 SDRAM Output AC Timing Specifications (continued)At recommended operating conditions with GV_{DD} of $1.8V \pm 100mV$.

Parameter	Symbol ¹	Min	Max	Unit	Note
MCS output hold with respect to MCK 266 MHz	t_{DDKHCC}	2.5	—	ns	3
MCK to MDQS Skew	t_{DDKHHM}	-0.6	0.6	ns	4
MDQ/MDM output setup with respect to MDQS 266 MHz	t_{DDKHDS} , t_{DDKLDS}	0.9	—	ns	5
MDQ/MDM output hold with respect to MDQS 266 MHz	t_{DDKHDX} , t_{DDKLDX}	1100	—	ps	5
MDQS preamble start	t_{DDKHMP}	$0.75 \times t_{MCK}$	—	ns	6
MDQS epilogue end	t_{DDKHME}	$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$	ns	6

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/MCK referenced measurements are made from the crossing of the two signals ± 0.1 V.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
- Note that t_{DDKHHM} follows the symbol conventions described in note 1. For example, t_{DDKHHM} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHHM} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjusts in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8306S PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- t_{DDKHMP} follows the symbol conventions described in note 1.

The following figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

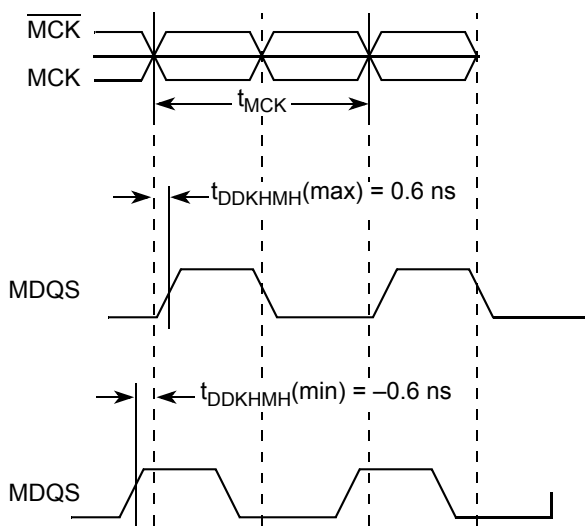


Figure 5. Timing Diagram for t_{DDKHMH}

The following figure shows the DDR2 SDRAM output timing diagram.

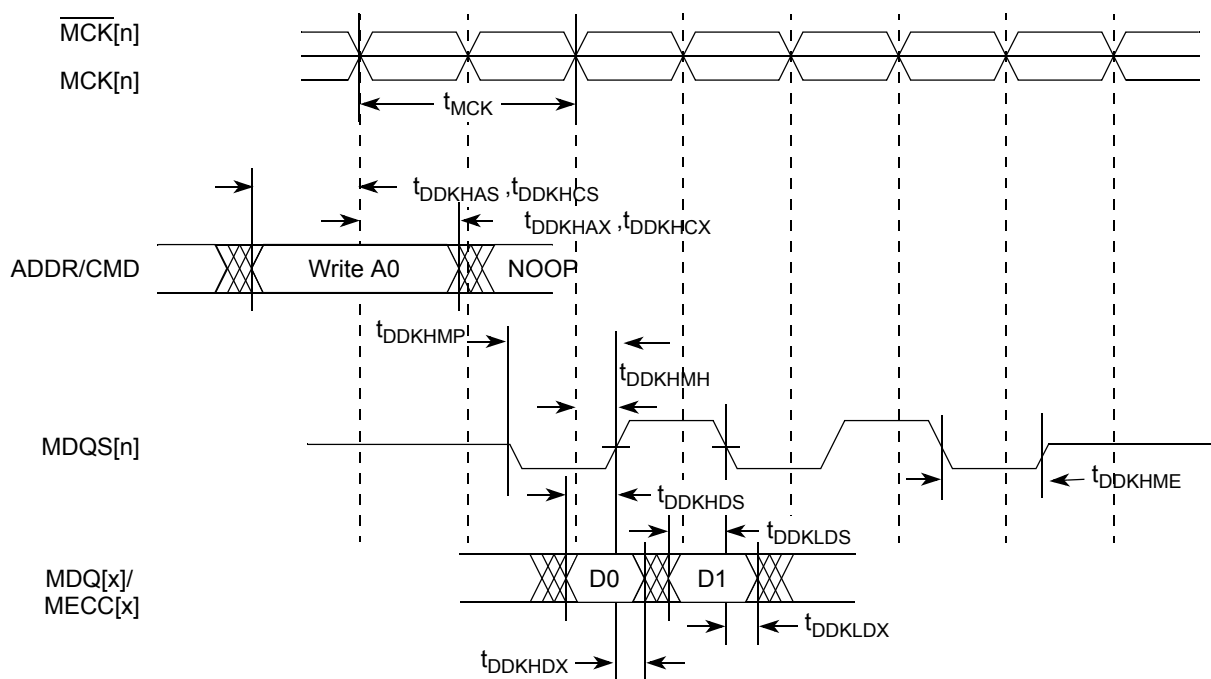


Figure 6. DDR2 SDRAM Output Timing Diagram

7 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8306S.

7.1 Local Bus DC Electrical Characteristics

The following table provides the DC electrical characteristics for the local bus interface.

Table 17. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V
Input current	I_{IN}	—	± 5	μA

7.2 Local Bus AC Electrical Specifications

The following table describes the general timing parameters of the local bus interface of the MPC8306S.

Table 18. Local Bus General Timing Parameters

Parameter	Symbol ¹	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock (LCLK n)	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock (LCLK n)	t_{LBIXKH}	1.0	—	ns	3, 4
Local bus clock (LCLK n) to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock (LCLK n) to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	5

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1).
- All timings are in reference to falling edge of LCLK0 (for all outputs and for \overline{LGTA} and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
- All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
- Input timings are measured at the pin.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

The following figure provides the AC test load for the local bus.

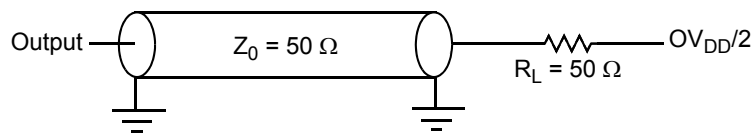


Figure 7. Local Bus AC Test Load

The following figures show the local bus signals. These figures have been given indicate timing parameters only and do not reflect actual functional operation of interface.

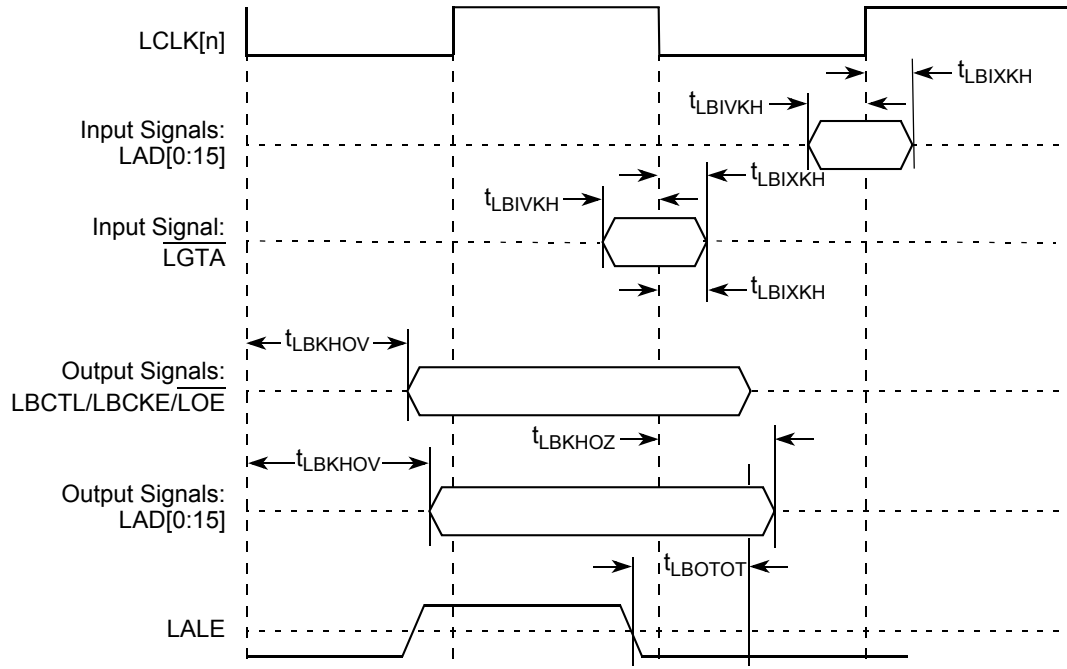


Figure 8. Local Bus Signals

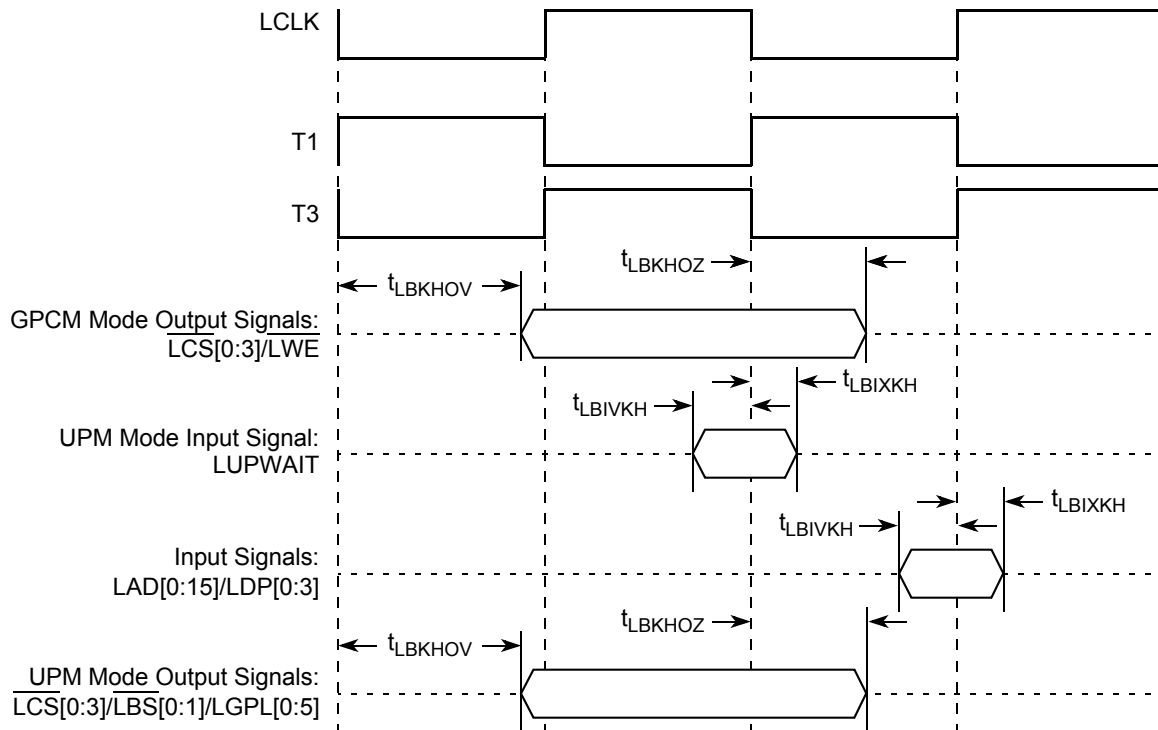


Figure 9. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2

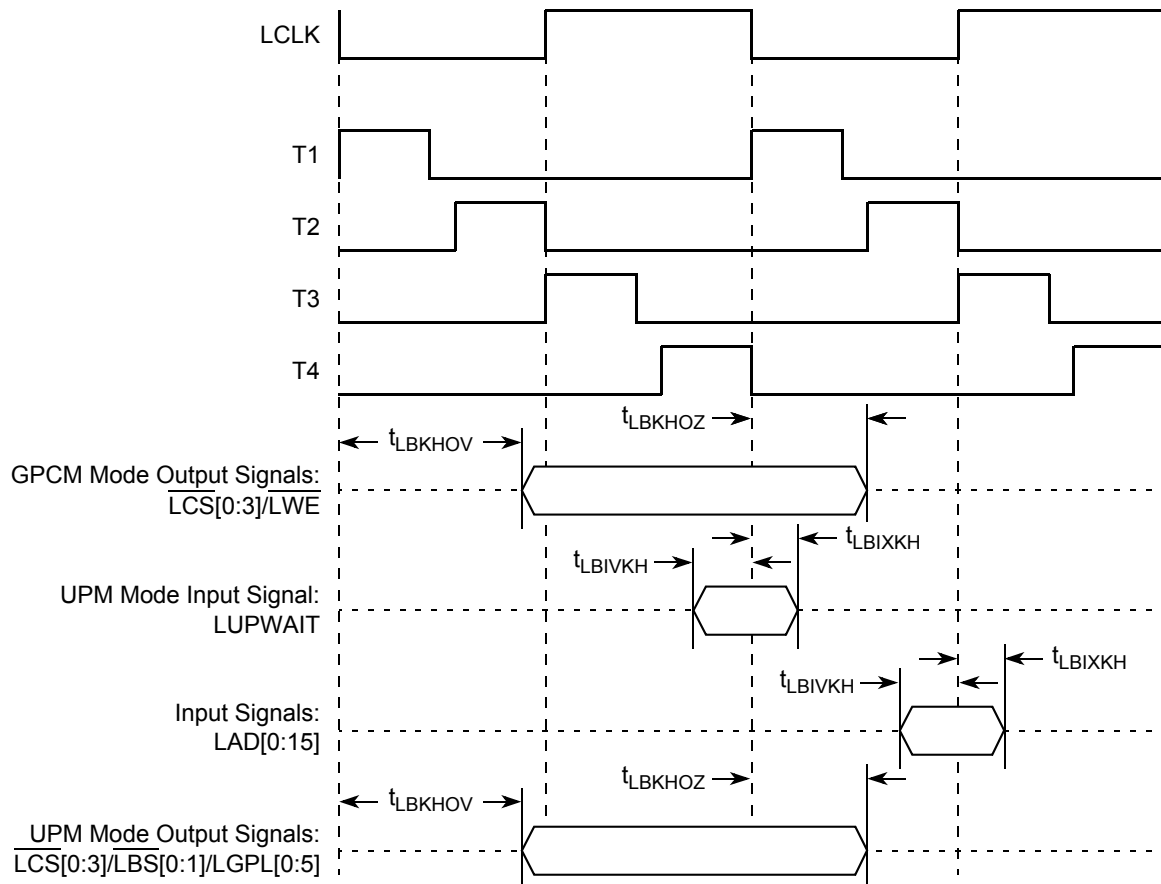


Figure 10. Local Bus Signals, GPCM/UPM Signals for $LCRR[CLKDIV] = 4$

8 Ethernet and MII Management

This section provides the AC and DC electrical characteristics for Ethernet interfaces.

8.1 Ethernet Controller (10/100 Mbps)—MII/RMII Electrical Characteristics

The electrical characteristics specified here apply to all MII (media independent interface) and RMII (reduced media independent interface), except MDIO (management data input/output) and MDC (management data clock). The MII and RMII are defined for 3.3 V. The electrical characteristics for MDIO and MDC are specified in [Section 8.3, “Ethernet Management Interface Electrical Characteristics.”](#)

8.1.1 DC Electrical Characteristics

All MII and RMII drivers and receivers comply with the DC parametric attributes specified in The following table.

Table 19. MII and RMII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	OV_{DD}	—		3	3.6	V
Output high voltage	V_{OH}	$I_{OH} = -4.0 \text{ mA}$	$OV_{DD} = \text{Min}$	2.40	$OV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 4.0 \text{ mA}$	$OV_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	—	-0.3	0.90	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$		—	± 5	μA

8.2 MII and RMII AC Timing Specifications

The AC timing specifications for MII and RMII are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

The following table provides the MII transmit AC timing specifications.

Table 20. MII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of $3.3 \text{ V} \pm 300\text{mV}$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$	t_{MTXF}	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure provides the AC test load.

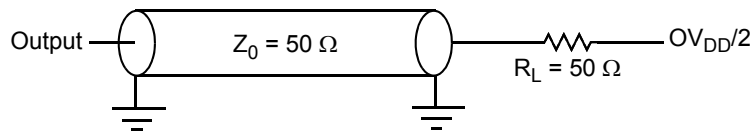


Figure 11. AC Test Load

The following figure shows the MII transmit AC timing diagram.

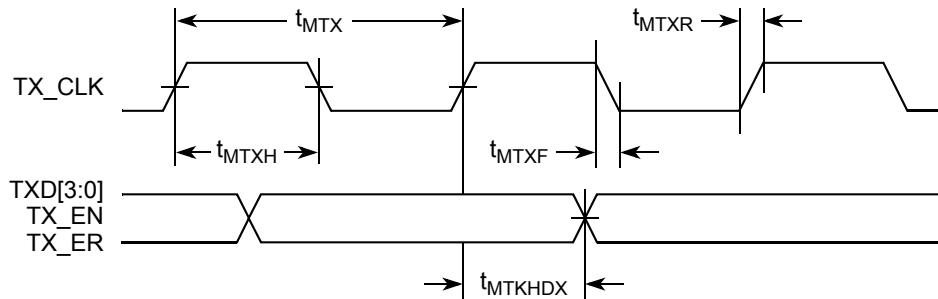


Figure 12. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

The following table provides the MII receive AC timing specifications.

Table 21. MII Receive AC Timing Specifications

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 300\text{mV}$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$	t_{MRXF}	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure shows the MII receive AC timing diagram.

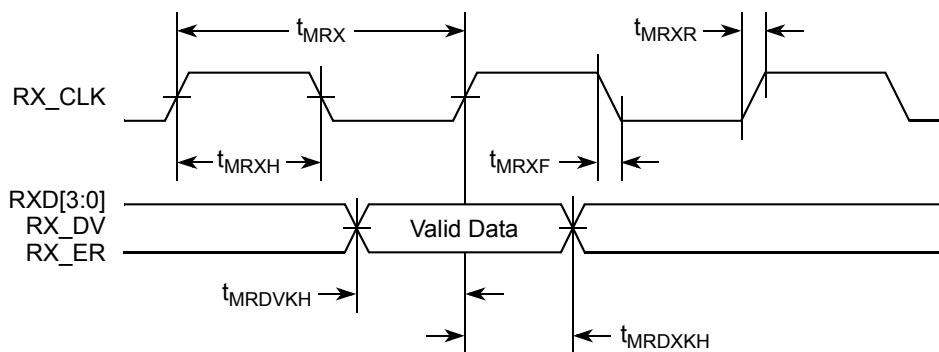


Figure 13. MII Receive AC Timing Diagram

8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.2.1 RMII Transmit AC Timing Specifications

The following table provides the RMII transmit AC timing specifications.

Table 22. RMII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 300\text{mV}$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	13	ns
REF_CLK data clock rise $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$	t_{RMXF}	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first three letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure provides the AC test load.

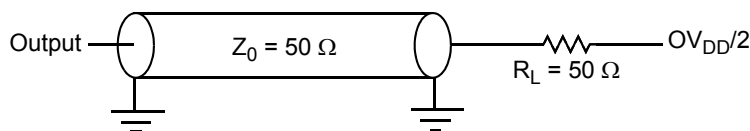


Figure 14. AC Test Load

The following figure shows the RMIITransmit AC timing diagram.

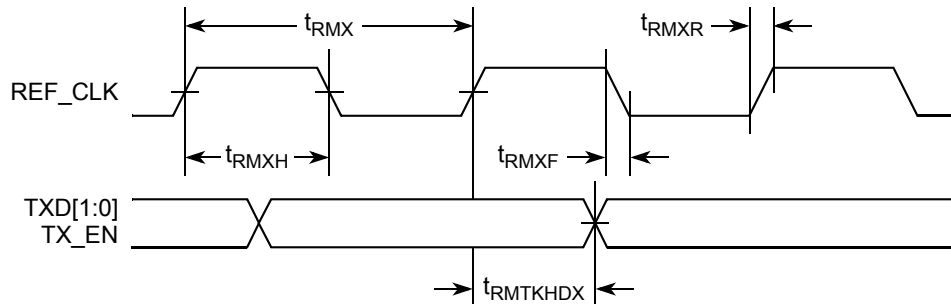


Figure 15. RMIITransmit AC Timing Diagram

8.2.2.2 RMIIReceive AC Timing Specifications

The following table provides the RMIIReceive AC timing specifications.

Table 23. RMIIReceive AC Timing Specifications

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 300\text{mV}$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$	t_{RMXF}	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first three letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMIIReceive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMIIReceive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMIIReference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).