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Freescale Semiconductor
Technical Data

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MPC8568E/MPC8567E PowerQUICC III Integrated Processor Hardware Specifications

Due to feature similarities, this document covers both the MPC8568E and MPC8567E features. For simplicity, MPC8568 may only be mentioned throughout the document.

The MPC8567E feature differences are as follows:

- The MPC8567E PCI-Express supports x1/x2/x4, but does not have x8 support.
- Does not have eTSEC1, eTSEC2, or TLU

Note that both the MPC8568E and MPC8567E have their own pin assignment tables.

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1 MPC8568E Overview

This section provides a high-level overview of MPC8568E features. Figure 1 shows the major functional units within the MPC8568E.

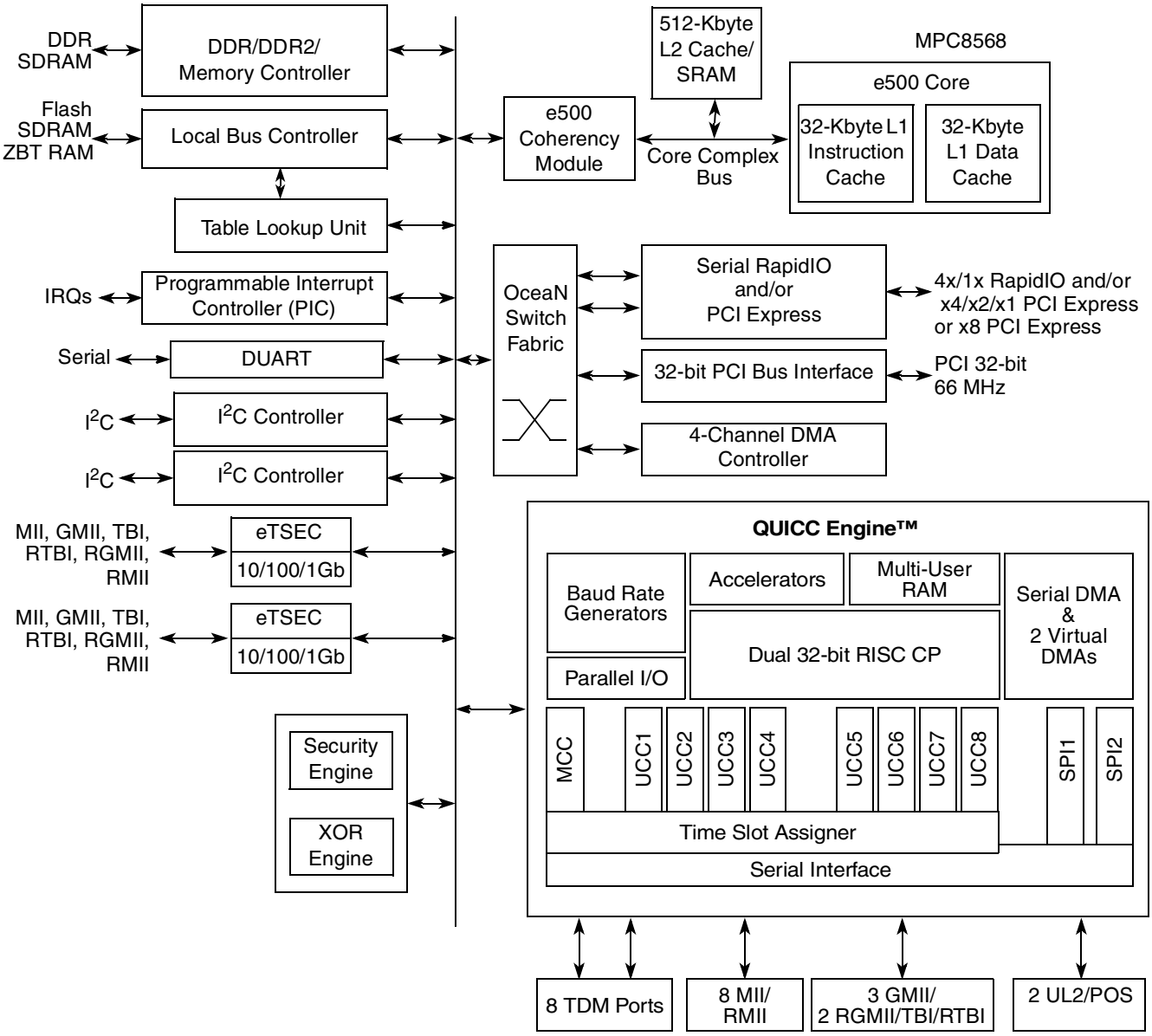


Figure 1. MPC8568E Block Diagram

1.1 MPCP8568E Key Features

- High-performance, Power Architecture® e500v2 core with 36-bit physical addressing
- 512 Kbytes of level-2 cache
- QUICC Engine (QE)
- Integrated security engine with XOR acceleration
- Two integrated 10/100/1Gb enhanced three-speed Ethernet controllers (eTSECs) with TCP/IP acceleration and classification capabilities
- DDR/DDR2 memory controller
- Table lookup unit (TLU) to access application-defined routing topology and control tables
- 32-bit PCI controller
- A 1x/4x Serial RapidIO® and/or x1/x2/x4 PCI Express interface. If x8 PCI Express is needed, then RapidIO is not available due to the limitation of the pin multiplexing.
- Programmable interrupt controller (PIC)
- Four-channel DMA controller, two I^2C controllers, DUART, and local bus controller (LBC)

NOTE

The MPC8568E and MPC8567E are also available without a security engine in a configuration known as the MPC8568 and MPC8567. All specifications other than those relating to security apply to the MPC8568 and MPC8567 exactly as described in this document.

1.2 MPC8568E Architecture Overview

1.2.1 e500 Core and Memory Unit

The MPC8568E contains a high-performance, 32-bit, Book E–enhanced e500v2 Power Architecture core. In addition to 36-bit physical addressing, this version of the e500 core includes the following:

- Double-precision floating-point APU—Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs
- Embedded vector and scalar single-precision floating-point APUs—Provide an instruction set for single-precision (32-bit) floating-point instructions

The MPC8568E also contains 512 Kbytes of L2 cache/SRAM, as follows:

- Eight-way set-associative cache organization with 32-byte cache lines
- Flexible configuration (can be configured as part cache, part SRAM)
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
- SRAM features include the following:
  - I/O devices access SRAM regions by marking transactions as snoopable (global).
  - Regions can reside at any aligned location in the memory map.

— Byte-accessible ECC uses read-modify-write transaction accesses for smaller-than-cache-line accesses.

1.2.2 e500 Coherency Module (ECM) and Address Map

The e500 coherency module (ECM) provides a mechanism for I/O-initiated transactions to snoop the bus between the e500 core and the integrated L2 cache in order to maintain coherency across local cacheable memory. It also provides a flexible switch-type structure for core- and I/O-initiated transactions to be routed or dispatched to target modules on the device.

The MPC8568E supports a flexible 36-bit physical address map. Conceptually, the address map consists of local space and external address space. The local address map is supported by eight local access windows that define mapping within the local 36-bit (64-Gbyte) address space.

The MPC8568E can be made part of a larger system address space through the mapping of translation windows. This functionality is included in the address translation and mapping units (ATMUs). Both inbound and outbound translation windows are provided. The ATMUs allows the MPC8568E to be part of larger address maps such as the PCI or PCI Express 64-bit address environment and the RapidIO environment.

1.2.3 QUICC Engine

- Integrated 8-port L2 Ethernet switch
  - 8 connection ports of 10/100 Mbps MII/RMII & one CPU internal port
  - Each port supports four priority levels
  - Priority levels used with VLAN tags or IP TOS field to implement QoS
  - QoS types of traffic, such as voice, video, and data
- Includes support for the following protocols:
  - ATM SAR up to 622 Mbps (OC-12) full duplex, with ATM traffic shaping (ATF TM4.1) for up to 64K ATM connections
  - ATM AAL1 structured and unstructured Circuit Emulation Service (CES 2.0)
  - IMA and ATM Transmission convergence sub-layer
  - ATM OAM handling features compatible with ITU-T I.610
  - PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686 and 3153
  - IP termination support for IPv4 and IPv6 packets including TOS, TTL and header checksum processing
  - ATM (AAL2/AAL5) to Ethernet (IP) interworking
  - Extensive support for ATM statistics and Ethernet RMON/MIB statistics.
  - 256 channels of HDLC/Transparent or 128 channels of SS#7
- Includes support for the following serial interfaces:
  - Two UL2/POS-PHY interfaces with 124 Multi-PHY addresses on UTOPIA interface each or 31 Multi-PHY addresses on the POS interface each.

— Three 1-Gbps Ethernet interfaces using three GMII, two RGMII/TBI/RTBI
— Up to eight 10/100-Mbps Ethernet interfaces using MII or RMII
— Up to eight T1/E1/J1/E3 or DS-3 serial interfaces

1.2.4 Integrated Security Engine (SEC)

The SEC is a modular and scalable security core optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP. Although it is not a protocol processor, the SEC is designed to perform multi-algorithmic operations (for example, 3DES-HMAC-SHA-1) in a single pass of the data. The version of the SEC used in the MPC8568E is specifically capable of performing single-pass security cryptographic processing for SSL 3.0, SSL 3.1/TLS 1.0, IPSec, SRTP, and 802.11i.

- Optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP
- Compatible with code written for the Freescale MPC8541E and MPC8555E devices
- XOR engine for parity checking in RAID storage applications.
- Four crypto-channels, each supporting multi-command descriptor chains
- Cryptographic execution units:
  — PKEU—public key execution unit
  — DEU—Data Encryption Standard execution unit
  — AESU—Advanced Encryption Standard unit
  — AFEU—ARC four execution unit
  — MDEU—message digest execution unit
  — KEU—Kasumi execution unit
  — RNG—Random number generator

1.2.5 Enhanced Three-Speed Ethernet Controllers

The MPC8568E has two on-chip enhanced three-speed Ethernet controllers (eTSECs). The eTSECs incorporate a media access control (MAC) sublayer that supports 10- and 100-Mbps and 1-Gbps Ethernet/802.3 networks with MII, RMII, GMII, RGMII, TBI, and RTBI physical interfaces. The eTSECs include 2-Kbyte receive and 10-Kbyte transmit FIFOs and DMA functions.

The MPC8568E eTSECs support programmable CRC generation and checking, RMON statistics, and jumbo frames of up to 9.6 Kbytes. Frame headers and buffer descriptors can be forced into the L2 cache to speed classification or other frame processing. They are IEEE Std 802.3™, IEEE 802.3u, IEEE 802.3x, IEEE 802.3z, IEEE 802.3ac, IEEE 802.3ab-compatible.

The buffer descriptors are based on the MPC8260 and MPC860T 10/100 Ethernet programming models. Each eTSEC can emulate a PowerQUICC III TSEC, allowing existing driver software to be re-used with minimal change.

Some of the key features of these controllers include:

- Flexible configuration for multiple PHY interface configurations. Table 1 lists available configurations.

Table 1. Supported eTSEC1 and eTSEC2 Configurations[1]

Mode Option	eTSEC1	eTSEC2
Ethernet standard interfaces	TBI, GMII, or MII	TBI, GMII, or MII
Ethernet reduced interfaces	RTBI, RGMII, or RMII	RTBI, RGMII, or RMII
FIFO and mixed interfaces	8-bit FIFO	TBI, GMII, MII, RTBI, RGMII, RMII, or 8-bit FIFO
	TBI, GMII, MII, RTBI, RGMII, RMII, or 8-bit FIFO	8-bit FIFO
	16-bit FIFO	Not used/not available

1 Both interfaces must use the same voltage (2.5 or 3.3 V).

- TCP/IP acceleration and QoS features:
  - IP v4 and IP v6 header recognition on receive
  - IP v4 header checksum verification and generation
  - TCP and UDP checksum verification and generation
  - Per-packet configurable acceleration
  - Recognition of VLAN, stacked (queue in queue) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
  - Supported in all FIFO modes
  - Transmission from up to eight physical queues
  - Reception to up to eight physical queues
- Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
  - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
- IEEE Std 802.1™ virtual local area network (VLAN) tags and priority
- VLAN insertion and deletion
  - Per-frame VLAN control word or default VLAN for each eTSEC
  - Extracted VLAN control word passed to software separately
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition
- Ability to force allocation of header information and buffer descriptors into L2 cache

1.2.6 DDR SDRAM Controller

The MPC8568E supports DDR SDRAM and DDR2 SDRAM. The memory interface controls main memory accesses and provides for a maximum of 16 Gbytes of main memory.

The MPC8568E supports a variety of SDRAM configurations. SDRAM banks can be built using DIMMs or directly-attached memory devices. Sixteen multiplexed address signals provide for device densities of 64 Mbits, 128 Mbits, 256 Mbits, 512 Mbits, 1 Gbits, 2 Gbits and 4 Gbits. Four chip select signals support

up to four banks of memory. The MPC8568E supports bank sizes from 64 Mbytes to 4 Gbytes. Nine column address strobes (MDM[0:8]) are used to provide byte selection for memory bank writes.

The MPC8568E can be configured to retain the currently active SDRAM page for pipelined burst accesses. Page mode support of up to 16 simultaneously open pages (32 for DDR2) can dramatically reduce access latencies for page hits. Depending on the memory system design and timing parameters, using page mode can save 3 to 4 clock cycles from subsequent burst accesses that hit in an active page.

Using ECC, the MPC8568E detects and corrects all single-bit errors and detects all double-bit errors and all errors within a nibble.

The MPC8568E can invoke a level of system power management by asserting the MCKE SDRAM signal on-the-fly to put the memory into a low-power sleep mode.

1.2.7 Table Lookup Unit (TLU)

The table lookup unit (TLU) provides access to application-defined routing topology and control tables in external memory. It accesses an external memory array attached to the local bus controller (LBC). Communication between the CPU and the TLU occurs via messages passed through the TLU's memory-mapped configuration and status registers.

The TLU provides resources for efficient generation of table entry addresses in memory, hash generation of addresses, and binary table searching algorithms for both exact-match and longest-prefix-match strategies.It supports the following TLU complex table types:

- Hash-Trie-Key table for hash-based exact-match algorithms
- Chained-Hash table for partially indexed and hashed exact-match algorithms
- Longest-prefix-match algorithm
- Flat-Data table for retrieving search results and simple indexed algorithms

1.2.8 PCI Controller

The MPC8568E supports one 32-bit PCI controller, which supports speeds of up to 66 MHz. Other features include:

- Compatible with the *PCI Local Bus Specification, Revision 2.2,* supporting 32- and 64-bit addressing
- Can function as host or agent bridge interface
- As a master, supports read and write operations to PCI memory space, PCI I/O space, and PCI configuration space
- Can generate PCI special-cycle and interrupt-acknowledge commands. As a target, it supports read and write operations to system memory as well as configuration accesses.
- Supports PCI-to-memory and memory-to-PCI streaming, memory prefetching of PCI read accesses, and posting of processor-to-PCI and PCI-to-memory writes
- PCI 3.3-V compatible with selectable hardware-enforced coherency

1.2.9 High Speed I/O Interfaces

The MPC8568E supports two high-speed I/O interface standards: serial RapidIO and PCI Express. It can be configured as x1/x4 SRIO and 1x/2x/4x PCI Express simultaneously with the following limitation:

- Both SRIO and PCI-Express are limited to use the same clock and are limited to 2.5G.
- Spread spectrum clocking can not be used because SRIO doesn't support this (PCI-Express does support it).

If x8 PCI Express is needed, then SRIO is not available due to the pin multiplex limitation.

1.2.10 Serial RapidIO

The serial RapidIO interface is based on the *RapidIO Interconnect Specification, Revision 1.2*. RapidIO is a high-performance, point-to-point, low-pin-count, packet-switched system-level interconnect that can be used in a variety of applications as an open standard. The RapidIO architecture has a rich variety of features including high data bandwidth, low-latency capability, and support for high-performance I/O devices, as well as support for message-passing and software-managed programming models. Key features of the serial RapidIO interface unit include:

- Support for *RapidIO Interconnect Specification, Revision 1.2* (all transaction flows and priorities)
- Both 1x and 4x LP-serial link interfaces, with transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
- Auto detection of 1x or 4x mode operation during port initialization
- 34-bit addressing and up to 256-byte data payload
- Receiver-controlled flow control
- Support for RapidIO error injection

The RapidIO messaging unit supports two inbox/outbox mailboxes (queues) for data and one doorbell message structure. Both chaining and direct modes are provided for the outbox, and messages can hold up to 16 packets of 256 bytes, or a total of 4 Kbytes.

1.2.11 PCI Express Interface

The MPC8568E supports a PCI Express interface compatible with the *PCI Express Base Specification Revision 1.0a*. It is configurable at boot time to act as either root complex or endpoint.The physical layer of the PCI Express interface operates at a 2.5-Gbaud data rate per lane.

Other features of the PCI Express interface include:

- x8, x4, x2, and x1 link widths supported
- Selectable operation as root complex or endpoint
- Both 32- and 64-bit addressing and 256-byte maximum payload size
- Full 64-bit decode with 32-bit wide windows

1.2.12 Programmable Interrupt Controller (PIC)

The MPC8568E PIC implements the logic and programming structures of the OpenPIC architecture, providing for external interrupts (with fully nested interrupt delivery), message interrupts, internal-logic driven interrupts, and global high-resolution timers. Up to 16 programmable interrupt priority levels are supported.

The PIC can be bypassed to allow use of an external interrupt controller.

1.2.13 DMA Controller, I^2C, DUART, and Local Bus Controller

The MPC8568E provides an integrated four-channel DMA controller, which can transfer data between any of its I/O or memory ports or between two devices or locations on the same port. The DMA controller also:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors.
- Scattering, gathering, and misaligned transfers are supported. In addition, stride transfers and complex transaction chaining are supported.
- Local attributes such as snoop and L2 write stashing can be specified.

There are two I^2C controllers. These synchronous, multimaster buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. 16-byte FIFOs are supported for both the transmitter and the receiver.

The MPC8568E local bus controller (LBC) port allows connections with a wide variety of external memories, DSPs, and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The user programmable machine (UPM) can be programmed to interface to synchronous devices or custom ASIC interfaces. The SDRAM controller provides access to standard SDRAM. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM, UPM, or SDRAM controller. All may exist in the same system. The local bus controller supports the following features:

- Multiplexed 32-bit address and data bus operating at up to 133 MHz
- Eight chip selects support eight external slaves
- Up to eight-beat burst transfers
- 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- Three protocol engines available on a per-chip-select basis
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Supports zero-bus-turnaround (ZBT) RAM

1.2.14 Power Management

In addition to low-voltage operation and dynamic power management, which automatically minimizes power consumption of blocks when they are idle, four power consumption modes are supported: full on, doze, nap, and sleep.

1.2.15 System Performance Monitor

The performance monitor facility supports eight 32-bit counters that can count up to 512 counter-specific events. It supports duration and quantity threshold counting and a burstiness feature that permits counting of burst events with a programmable time between bursts.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8568E. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings [1]

Characteristic	Symbol	Max Value	Unit	Notes
Core supply voltage	V_{DD}	–0.3 to 1.21	V	—
PLL supply voltage	AV_{DD_PLAT}, AV_{DD_CORE}, AV_{DD_CE}, AV_{DD_PCI}, AV_{DD_LBIU}, AV_{DD_SRDS}	–0.3 to 1.21	V	—
Core power supply for SerDes transceiver	SCOREVDD	–0.3 to 1.21	V	—
Pad power supply for SerDes transceiver	XV_{DD}	–0.3 to 1.21	V	—
DDR and DDR2 DRAM I/O voltage	GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
eTSEC1, eTSEC2 I/O Voltage	LV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	—
QE UCC1/UCC2 Ethernet Interface I/O Voltage	TV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	—
PCI, DUART, system control and power management, I^2C, and JTAG I/O voltage	OV_{DD}	–0.3 to 3.63	V	3
Local bus I/O voltage	BV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	3

Table 2. Absolute Maximum Ratings [1] (continued)

Characteristic		Symbol	Max Value	Unit	Notes
Input voltage	DDR/DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR/DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	–0.3 to (LV_{DD} + 0.3) –0.3 to (TV_{DD} + 0.3)	V	4, 5
	Local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)		—
	DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	5
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6
Storage temperature range		T_{STG}	–55 to 150	•C	—

Notes:
1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** L/TV_{IN} must not exceed L/TV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. $(M,L,O)V_{IN}$ and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 2.

2.1.2 Recommended Operating Conditions

Table 3 provides the recommended operating conditions for this device. Note that the values in Table 3 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

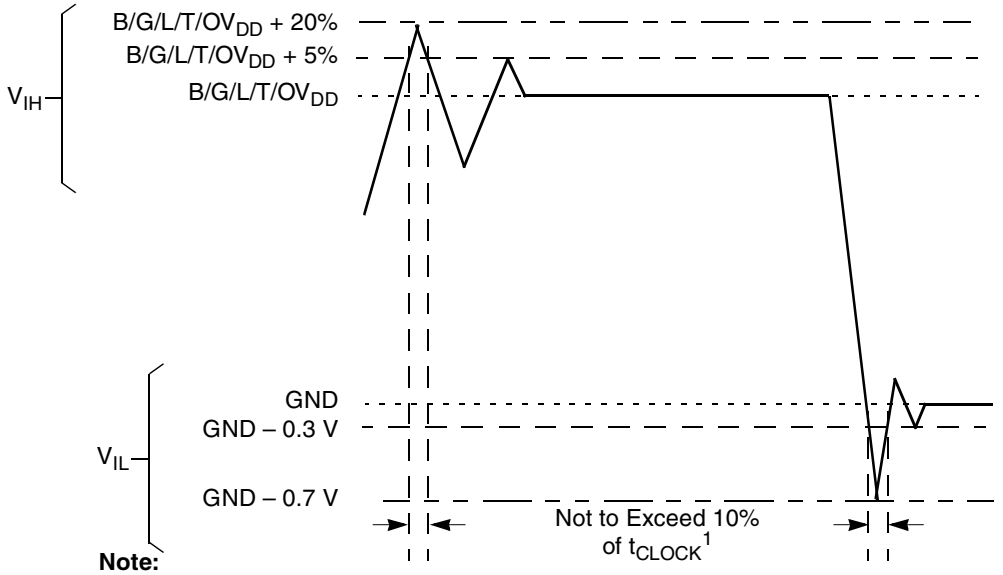
Table 3. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.1 V ± 55 mV	V	—
PLL supply voltage	AV_{DD_PLAT}, AV_{DD_CORE}, AV_{DD_CE}, AV_{DD_PCI}, AV_{DD_LBIU}, AV_{DD_SRDS}	1.1 V ± 55 mV	V	—
Core power supply for SerDes transceiver	SCOREVDD	1.1 V ± 55 mV	V	—
Pad power supply for SerDes transceiver	XV_{DD}	1.1 V ± 55 mV	V	—
DDR and DDR2 DRAM I/O voltage	GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	—

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Three-speed Ethernet I/O voltage		LV_{DD} TV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
PCI, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	—
Local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
Input voltage	DDR and DDR2 DRAM signals	MV_{IN}	GND to GV_{DD}	V	—
	DDR and DDR2 DRAM reference	MV_{REF}	GND to $GV_{DD}/2$	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	—
	Local bus signals	BV_{IN}	GND to BV_{DD}	V	—
	PCI, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	—
Junction temperature range		Tj	0 to105	°C	—

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8568E.



Note:
1. Note that t_{CLOCK} refers to the clock period associated with the respective interface
   For I2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, tCLOCK references EC_GTX_CLK125.
   For LBIU, t_{CLOCK} references LCLK.
   For PCI, t_{CLOCK} references PCI_CLK or SYSCLK.
   For SerDes, t_{CLOCK} references SD_REF_CLK.
2. Note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the PCI rev. 2.2 standard (section 4.2.2.3)

Figure 2. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/TV_{DD}/OV_{DD}$

The core voltage must always be provided at nominal 1.1V. (See Table 3 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

2.1.3 Output Driver Characteristics

Table 4 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 25	BV_{DD} = 3.3 V BV_{DD} = 2.5 V	1
	45(default) 45(default)	BV_{DD} = 3.3 V BV_{DD} = 2.5 V	
PCI signals	25	OV_{DD} = 3.3 V	2
	42 (default)		
DDR signal	20	GV_{DD} = 2.5 V	—
DDR2 signal	16 32 (half strength mode)	GV_{DD} = 1.8 V	—
eTSEC 10/100/1000 signals	42	L/TV_{DD} = 2.5/3.3 V	—
DUART, system control, JTAG	42	OV_{DD} = 3.3 V	—
I2C	150	OV_{DD} = 3.3 V	—

Notes:
1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the $\overline{\text{PCI\_GNT}}[1]$ signal at reset.

2.2 Power Sequencing

The MPC8568E requires its power rails to be applied in specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD}, AV_{DD}_n, BV_{DD}, $SCOREV_{DD}$, LV_{DD}, TV_{DD}, XV_{DD}, OV_{DD}
2. GV_{DD}

All supplies must be at their stable values within 50 ms.

NOTE

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for GVDD is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for GVDD is not required.

3 Power Characteristics

The power dissipation of V_{DD} for various core complex bus (CCB) versus the core and QE frequency for MPC8568E is shown in Table 5. Note that this is based on the design estimate only. More accurate power number will be available after we have done the measurement on the silicon.

Table 5. MPC8568E Power Dissipation

CCB Frequency	Core Frequency	QE Frequency	Typical 65°C	Typical 105°C	Maximum	Unit
400	800	400	8.7	12.0	13.0	W
400	1000	400	8.9	12.3	13.6	W
400	1200	400	11.3	15.7	16.9	W
533	1333	533	12.4	17.2	18.7	W

Notes:
1. CCB Frequency is the SoC platform frequency which corresponds to DDR data rate.
2. Typical 65 °C based on V_{DD}=1.1V, Tj=65.
3. Typical 105 °C based on V_{DD}=1.1V, Tj=105.
4. Maximum based on V_{DD}=1.1V, Tj=105.

Table 6. Typical MPC8568E I/O Power Dissipation

Interface	Parameters	GV_{DD}		BV_{DD}		OV_{DD}	LV_{DD}		TV_{DD}		XV_{DD}	Unit	Comment
		2.5 V	1.8 V	3.3 V	2.5 V		3.3 V	2.5 V	3.3 V	2.5 V			
DDR/DDR2	333 MHz	0.76	0.50									W	Data rate 64-bit with ECC 60% utilization
	400 MHz		0.56									W	
	533 MHz		0.68									W	
Local Bus	33 MHz, 32b			0.07	0.04							W	—
	66 MHz, 32b			0.13	0.07							W	—
	133 MHz, 32b			0.24	0.14							W	—
PCI	33 MHz					0.04						W	—
	66 MHz					0.07						W	—
SRIO	4x, 3.125G										0.49	W	—
PCI Express	8x, 2.5G										0.71	W	—

Table 6. Typical MPC8568E I/O Power Dissipation (continued)

Interface	Parameters	GV_{DD}		BV_{DD}		OV_{DD}	LV_{DD}		TV_{DD}		XV_{DD}	Unit	Comment
		2.5 V	1.8 V	3.3 V	2.5 V		3.3 V	2.5 V	3.3 V	2.5 V			
eTSEC Ethernet	MII						0.01					W	Multiply with number of the interfaces
	GMII/TBI						0.07					W	
	RGMII/RTBI							0.04				W	
eTSEC FIFO I/O	16b, 200 MHz						0.20					W	Multiply with number of the interfaces
	16b, 155 MHz						0.16					W	
	8b, 200 MHz						0.11					W	
	8b, 155 MHz						0.08					W	
QE UCC	MII/RMII								0.01			W	Multiply with number of the interfaces If UCC is programmed for other protocols, scale Ethernet power dissipation to the number of signals and the clock rate
	GMII/TBI								0.07			W	
	RGMII/RTBI									0.04		W	

Note: This is the power for each individual interface. The power must be calculated for each interface being utilized.

4 Input Clocks

4.1 System Clock Timing

Table 7 provides the system clock (SYSCLK) AC timing specifications for the MPC8568E.

Table 7. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	—	—	166	MHz	1
SYSCLK cycle time	t_{SYSCLK}	6.0	—	—	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3

Table 7. SYSCLK AC Timing Specifications (continued)

At recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK jitter	—	—	—	+/– 150	ps	4, 5

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 core frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 23.2, "CCB/SYSCLK PLL Ratio and Section 23.3, "e500 Core PLL Ratio," for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

4.2 PCI Clock Timing

Table 8 provides the PCI clock (PCI_CLK) AC timing specifications for the MPC8568E.

Table 8. PCI_CLK AC Timing Specifications

At recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
PCI_CLK frequency	f_{PCI_CLK}	—	—	66.7	MHz	—
PCI_CLK cycle time	t_{PCI_CLK}	15	—	—	ns	—
PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	1
PCI_CLK duty cycle	t_{KHK}/t_{PCI_CLK}	40	—	60	%	2
PCI_CLK jitter	—	—	—	+/– 150	ps	3,4

Notes:
1. Rise and fall times for PCI_CLK are measured at 0.4 V and 2.7 V.
2. Timing is guaranteed by design and characterization.
3. This represents the total input jitter—short term and long term—and is guaranteed by design.
4. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

4.3 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the Time Base unit of the e500. There is no need for jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency. RTC may be grounded if not needed.

4.4 eTSEC Gigabit Reference Clock Timing

Table 9 provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the MPC8568E.

Table 9. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time L/TVDD = 2.5 V L/TVDD = 3.3 V	t_{G125R}, t_{G125F}	 — —	 — —	 0.75 1.0	ns	—
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	1, 2

Notes:
1. Timing is guaranteed by design and characterization.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.
3. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for L/TVDD = 2.5 V, and from 0.6 and 2.7 V for L/TVDD = 3.3 V.

4.5 FIFO Clock Speed Restrictions

Note the following FIFO maximum speed restrictions based on the platform speed.

For FIFO GMII mode:

FIFO TX/RX clock frequency <= platform clock frequency / 4.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no higher than 127 MHz.

For FIFO encoded mode:

FIFO TX/RX clock frequency <= platform clock frequency / 3.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no higher than 167 MHz

4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8568E. Table 10 provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 10. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	µs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	µs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Notes:
1. SYSCLK is the primary clock input for the MPC8568E.

Table 11 provides the PLL lock times.

Table 11. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
Platform PLL lock times	—	100	µs	—
QE PLL lock times	—	100	µs	—
CPU PLL lock times	—	100	µs	—
PCI PLL lock times	—	100	µs	—
Local bus PLL	—	100	µs	—

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8568E. Note that DDR SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8568E when GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF}+ 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	—
Output leakage current	I_{OZ}	–10	10	µA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 13 provides the DDR capacitance when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5 V.

Table 14. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.3	2.7	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.15	GV_{DD} + 0.3	V	—

Table 14. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input low voltage	V_{IL}	–0.3	MV_{REF}– 0.15	V	—
Output leakage current	I_{OZ}	–10	10	μA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 15 provides the DDR capacitance when GV_{DD} (typ)=2.5 V.

Table 15. DDR SDRAM Capacitance for GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 16 provides the current draw characteristics for MV_{REF}.

Table 16. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM when $GV_{DD}(typ)$=1.8 V.

Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V	—

Table 18 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ)$=2.5 V.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V	—

Table 19 provides the input AC timing specifications for the DDR SDRAM interface.

Table 19. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM	t_{CISKEW}			ps	1, 2
533 MHz		–300	300		3
400 MHz		–365	365		—
333 MHz		–390	390		—

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: t_{DISKEW} =+/-(T/4 – abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.
3. Maximum DDR1 frequency is 400 MHz.

Figure 3 provides the input timing diagram for the DDR SDRAM interface. t_{DISKEW} can be calculated from t_{CISKEW}. See Table 19 footnote 2.

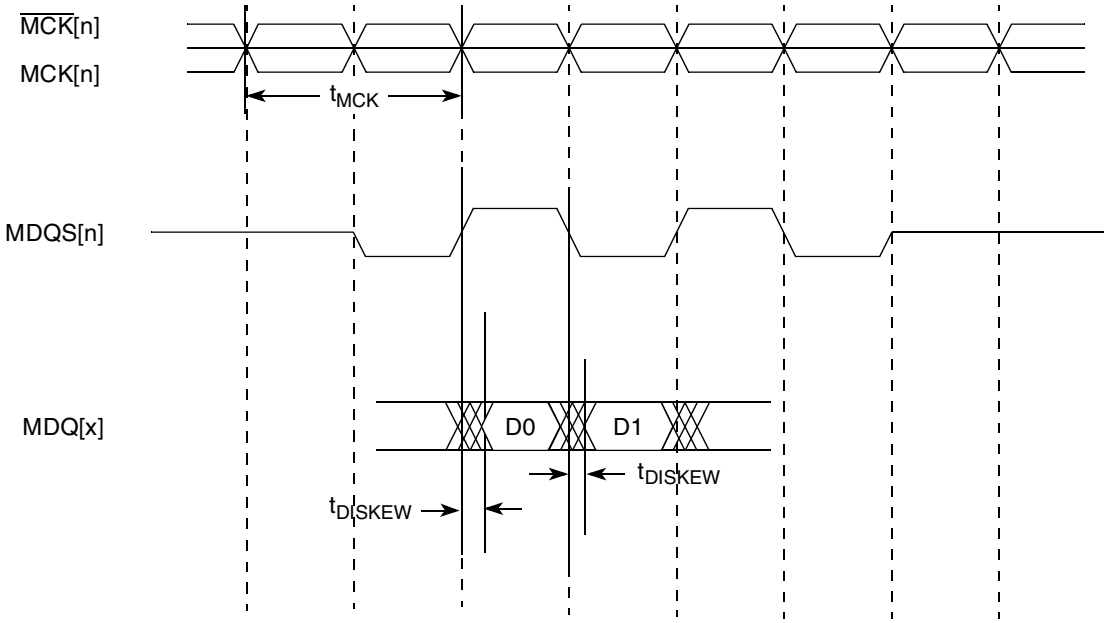


Figure 3. DDR SDRAM Input Timing Diagram

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 20. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	3.75	10	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		

Table 20. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
533 MHz		538	—		7
400 MHz		700	—		
333 MHz		900	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
533 MHz		538	—		7
400 MHz		700	—		
333 MHz		900	—		
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8568E Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. Maximum DDR1 frequency is 400 MHz

NOTE

For the ADDR/CMD setup and hold specifications in Table 20, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 4 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (tDDKHMH).

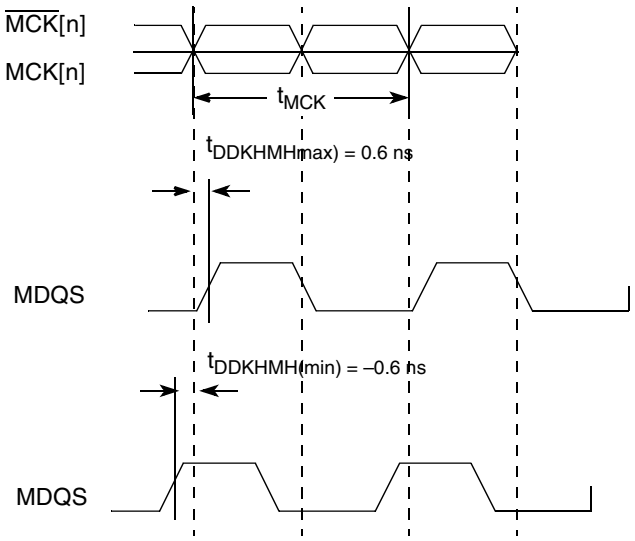


Figure 4. Timing Diagram for tDDKHMH

Figure 5 shows the DDR SDRAM output timing diagram.

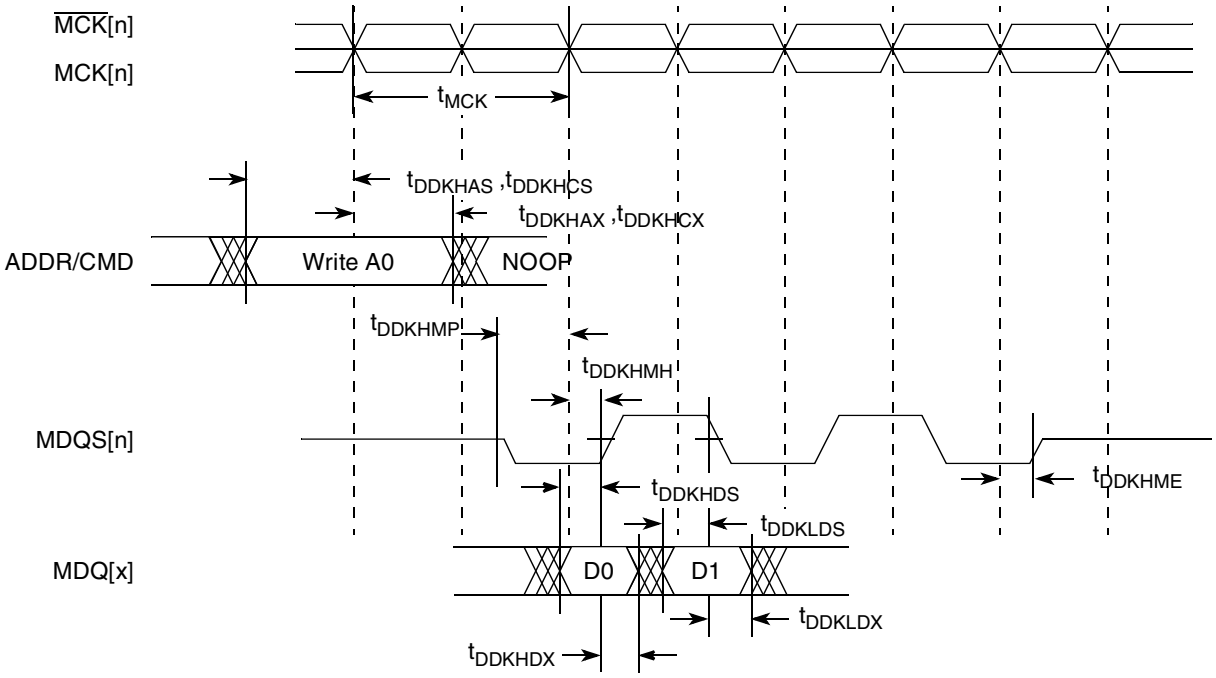


Figure 5. DDR SDRAM Output Timing Diagram

Figure 6 provides the AC test load for the DDR bus.

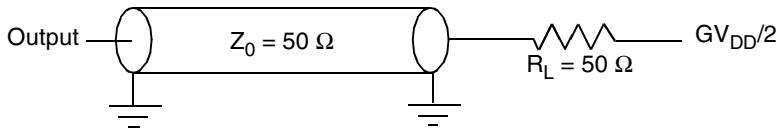


Figure 6. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8568E.

7.1 DUART DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the DUART interface.

Table 21. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V