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PRMD12

50 V, 100 mA NPN/PNP Resistor-Equipped double Transistors (RET)

11 July 2017

Product data sheet

1. General description

NPN/PNP Resistor-Equipped double Transistors (RET) in an ultra small DFN1412-6 (SOT1268) leadless Surface-Mounted Device (SMD) plastic package.

NPN/PNP complement: PRMH12.

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Low package height of 0.5 mm
- AEC-Q101 qualified

3. Applications

- Digital applications
- Cost-savings alternative to BC847/BC857 series digital applications
- Control of IC inputs
- Switching loads

4. Quick reference data

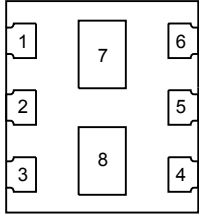
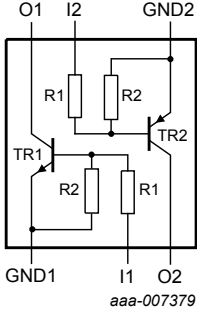
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Per transistor, for the PNP transistor with negative polarity							
V_{CEO}	collector-emitter voltage	open base	-	-	50	V	
I_O	output current		-	-	100	mA	
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 5\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$	80	-	-		
R1	bias resistor 1	$T_{amb} = 25\text{ }^\circ\text{C}$	[1]	33	47	61	k Ω
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	

[1] See section "Test information" for resistor calculation and test conditions.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 <p>Transparent top view DFN1412-6 (SOT1268)</p>	 <p>GND1 I2 GND2 O1 I1 O2 TR1 TR2 R1 R2 aaa-007379</p>
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		
7	O1	output (collector) TR1		
8	O2	output (collector) TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PRMD12	DFN1412-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body: 1.4 mm x 1.2 mm x 0.47 mm	SOT1268

7. Marking

Table 4. Marking codes

Type number	Marking code
PRMD12	B2

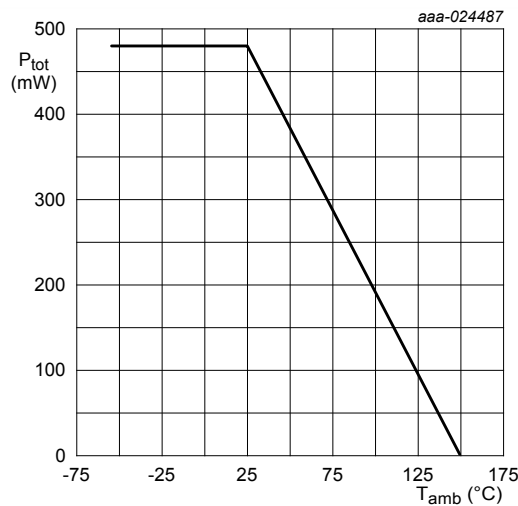
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor, for the PNP transistor with negative polarity						
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V_{EBO}	emitter-base voltage	open collector		-	10	V
V_I	input voltage	positive		-	40	V
		negative		-	-10	V
I_O	output current			-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1]	-	325	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1]	-	480	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



FR4 PCB, standard footprint

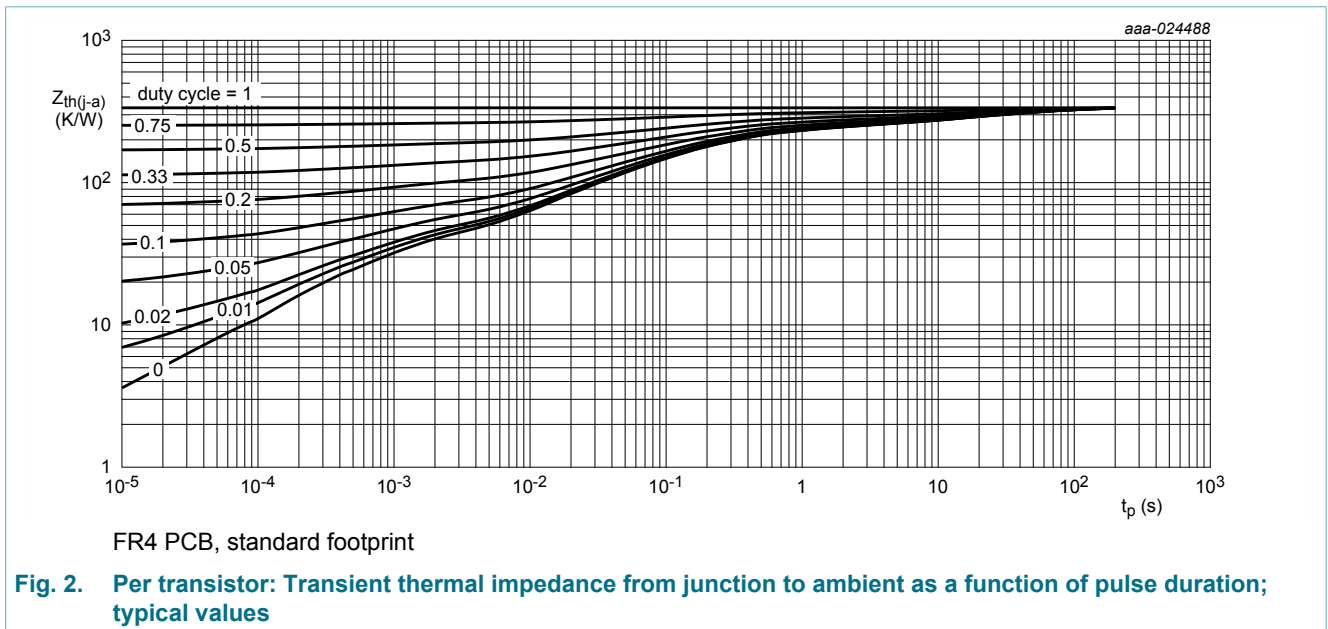
Fig. 1. Per device: Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	385	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	261	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Per transistor, for the PNP transistor with negative polarity							
I_{CBO}	collector-base cut-off current (emitter open)	$V_{CB} = 50\text{ V}; I_E = 0\text{ A}; T_{amb} = 25\text{ °C}$	-	-	100	nA	
I_{CEO}	collector-emitter cut-off current (base open)	$V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_{amb} = 25\text{ °C}$	-	-	1	μA	
		$V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_j = 150\text{ °C}$	-	-	5	μA	
I_{EBO}	emitter-base cut-off current (collector open)	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}; T_{amb} = 25\text{ °C}$	-	-	90	μA	
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 5\text{ mA}; T_{amb} = 25\text{ °C}$	80	-	-		
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 0.5\text{ mA}; T_{amb} = 25\text{ °C}$	-	-	150	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}; I_C = 100\text{ }\mu\text{A}; T_{amb} = 25\text{ °C}$	-	1.2	0.8	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}; I_C = 2\text{ mA}; T_{amb} = 25\text{ °C}$	3	1.6	-	V	
R1	bias resistor 1	$T_{amb} = 25\text{ °C}$	[1]	33	47	61	k Ω
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	
C_C	collector capacitance	$V_{CB} = 10\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A};$ $f = 1\text{ MHz}; T_{amb} = 25\text{ °C}$	-	-	2.5	pF	
		$V_{CB} = -10\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A};$ $f = 1\text{ MHz}; T_{amb} = 25\text{ °C}$	-	-	3	pF	
f_T	transition frequency	$V_{CE} = 5\text{ V}; I_C = 10\text{ mA}; f = 100\text{ MHz};$ $T_{amb} = 25\text{ °C}$	[2]	-	230	-	MHz
		$V_{CE} = -5\text{ V}; I_C = -10\text{ mA}; f = 100\text{ MHz};$ $T_{amb} = 25\text{ °C}$	[2]	-	180	-	MHz

[1] See section "Test information" for resistor calculation and test conditions.

[2] Characteristics of built-in transistor.

50 V, 100 mA NPN/PNP Resistor-Equipped double Transistors (RET)

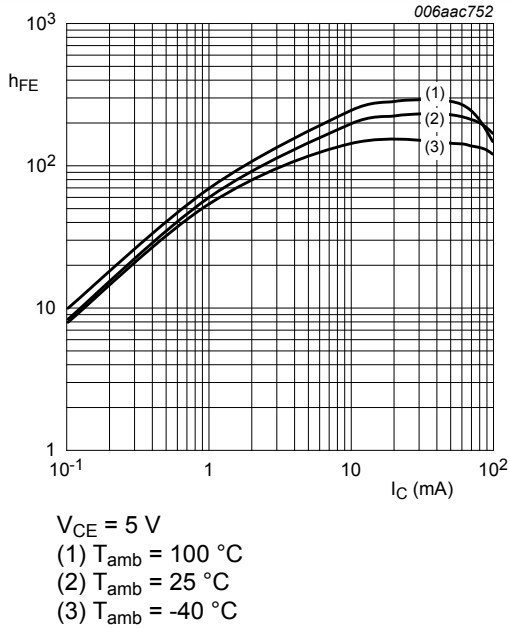


Fig. 3. NPN transistor: DC current gain as a function of collector current; typical values

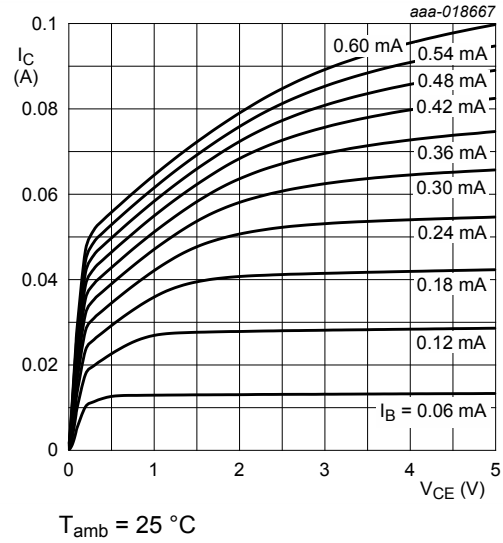


Fig. 4. NPN Transistor: Collector current as a function of collector-emitter voltage; typical values

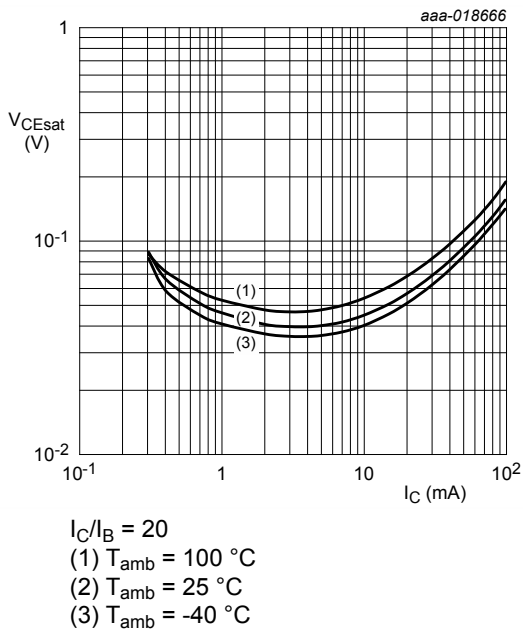


Fig. 5. NPN Transistor: Collector-emitter saturation voltage as a function of collector current; typical values

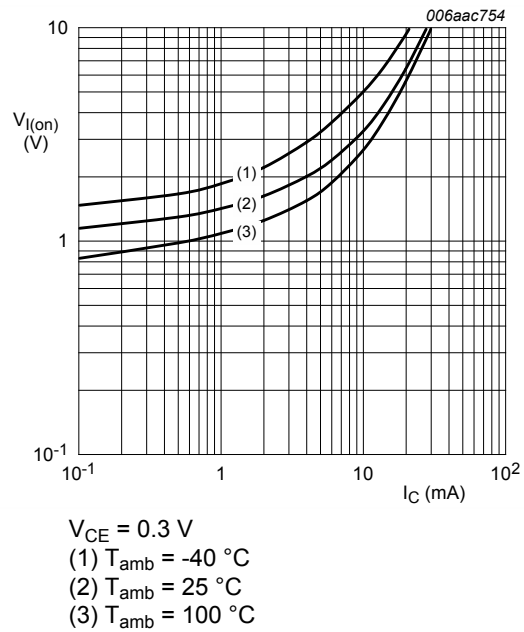
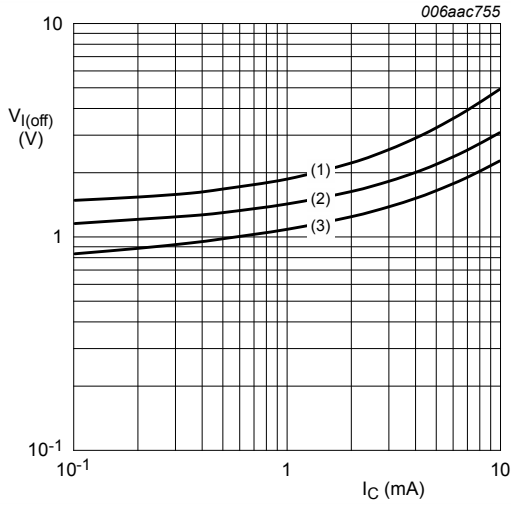


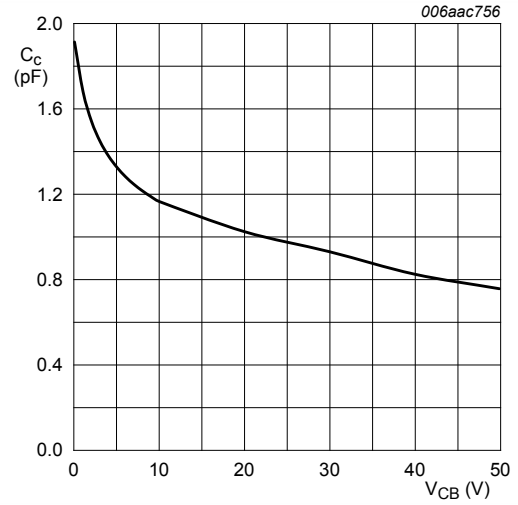
Fig. 6. NPN transistor: On-state input voltage as a function of collector current; typical values

50 V, 100 mA NPN/PNP Resistor-Equipped double Transistors (RET)



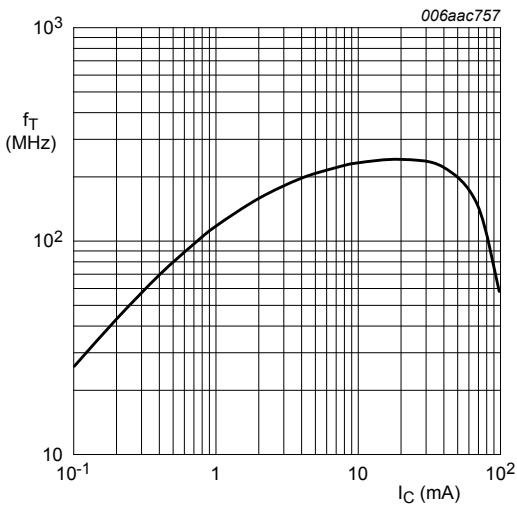
$V_{CE} = 5\text{ V}$
 (1) $T_{amb} = -40\text{ }^\circ\text{C}$
 (2) $T_{amb} = 25\text{ }^\circ\text{C}$
 (3) $T_{amb} = 100\text{ }^\circ\text{C}$

Fig. 7. NPN transistor: Off-state input voltage as a function of collector current; typical values



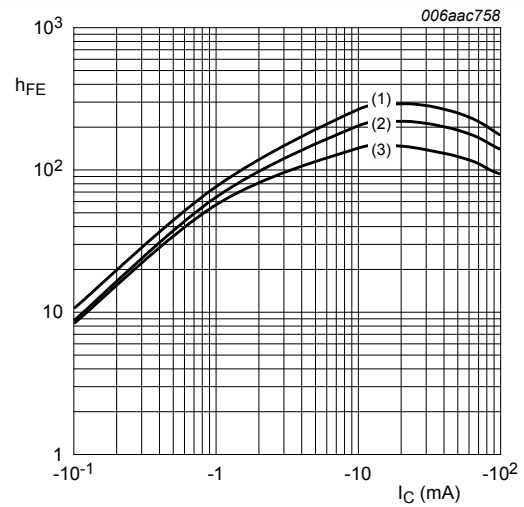
$f = 1\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$

Fig. 8. NPN transistor: Collector capacitance as a function of collector-base voltage; typical values



$V_{CE} = 5\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}$

Fig. 9. NPN transistor: Transition frequency as a function of collector current; typical values of built-in transistor



$V_{CE} = -5\text{ V}$
 (1) $T_{amb} = 100\text{ }^\circ\text{C}$
 (2) $T_{amb} = 25\text{ }^\circ\text{C}$
 (3) $T_{amb} = -40\text{ }^\circ\text{C}$

Fig. 10. PNP transistor: DC current gain as a function of collector current; typical values

50 V, 100 mA NPN/PNP Resistor-Equipped double Transistors (RET)

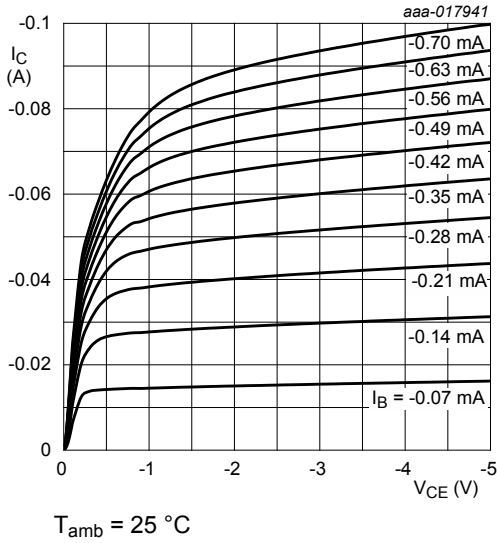


Fig. 11. PNP transistor: Collector current as a function of collector-emitter voltage; typical values

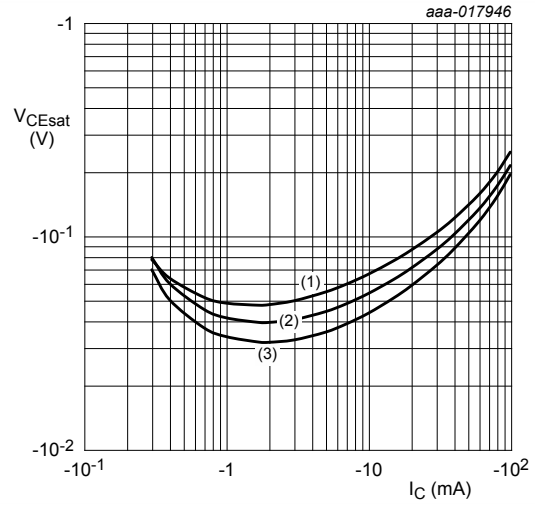


Fig. 12. PNP transistor: Collector-emitter saturation voltage as a function of collector current; typical values

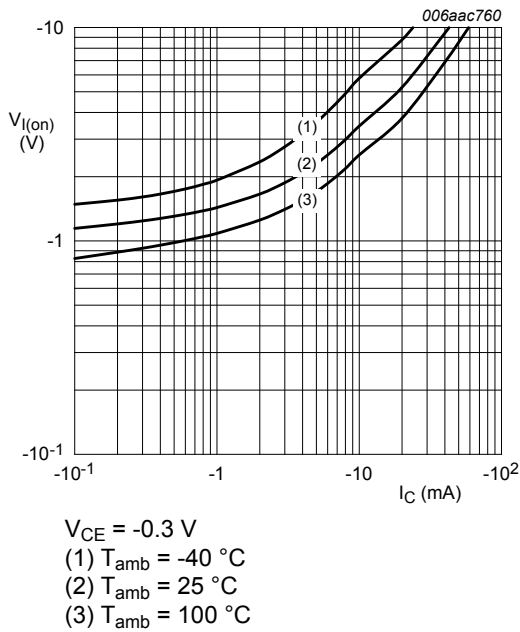


Fig. 13. PNP transistor: On-state input voltage as a function of collector current; typical values

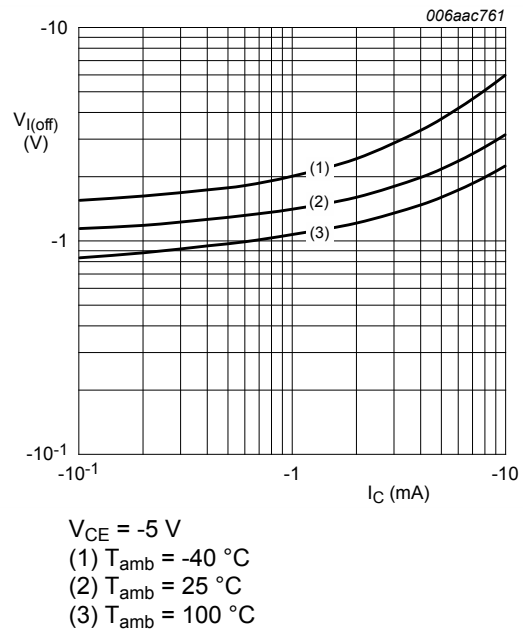
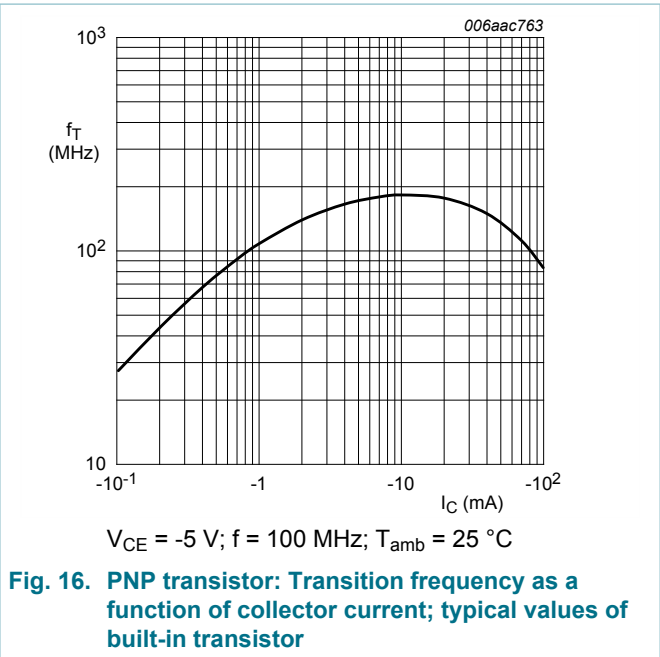
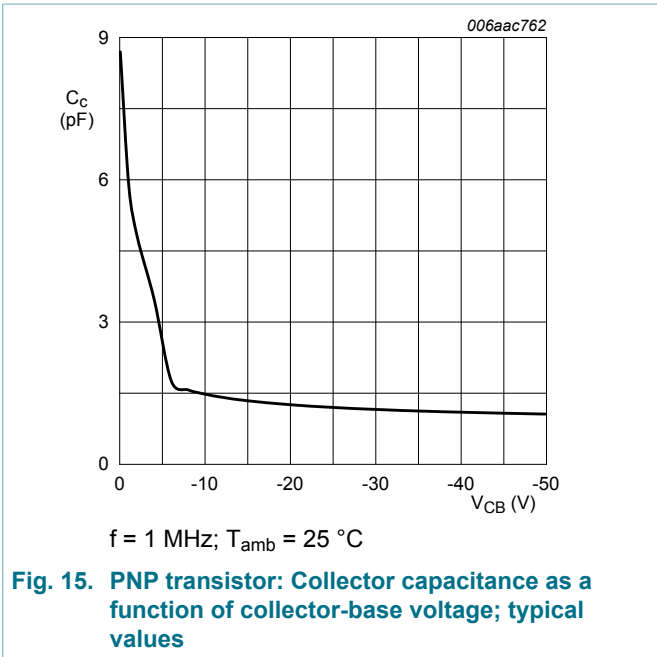


Fig. 14. PNP transistor: Off-state input voltage as a function of collector current; typical values

50 V, 100 mA NPN/PNP Resistor-Equipped double Transistors (RET)



11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

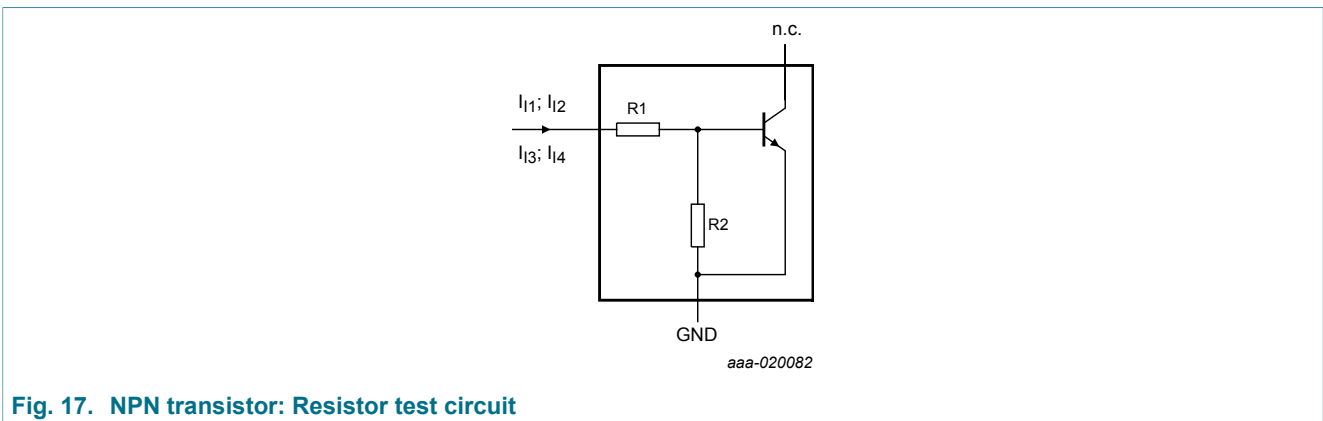
Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R1 = \frac{V(I12) - V(I11)}{I12 - I11}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I14) - V(I13)}{R1 \cdot (I14 - I13)} - 1$$



50 V, 100 mA NPN/PNP Resistor-Equipped double Transistors (RET)

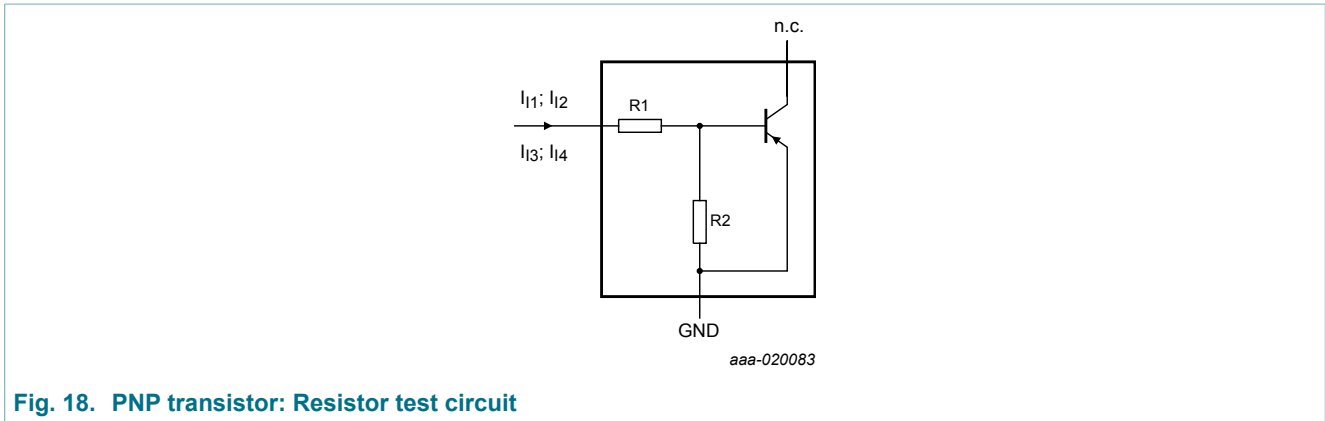


Fig. 18. PNP transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

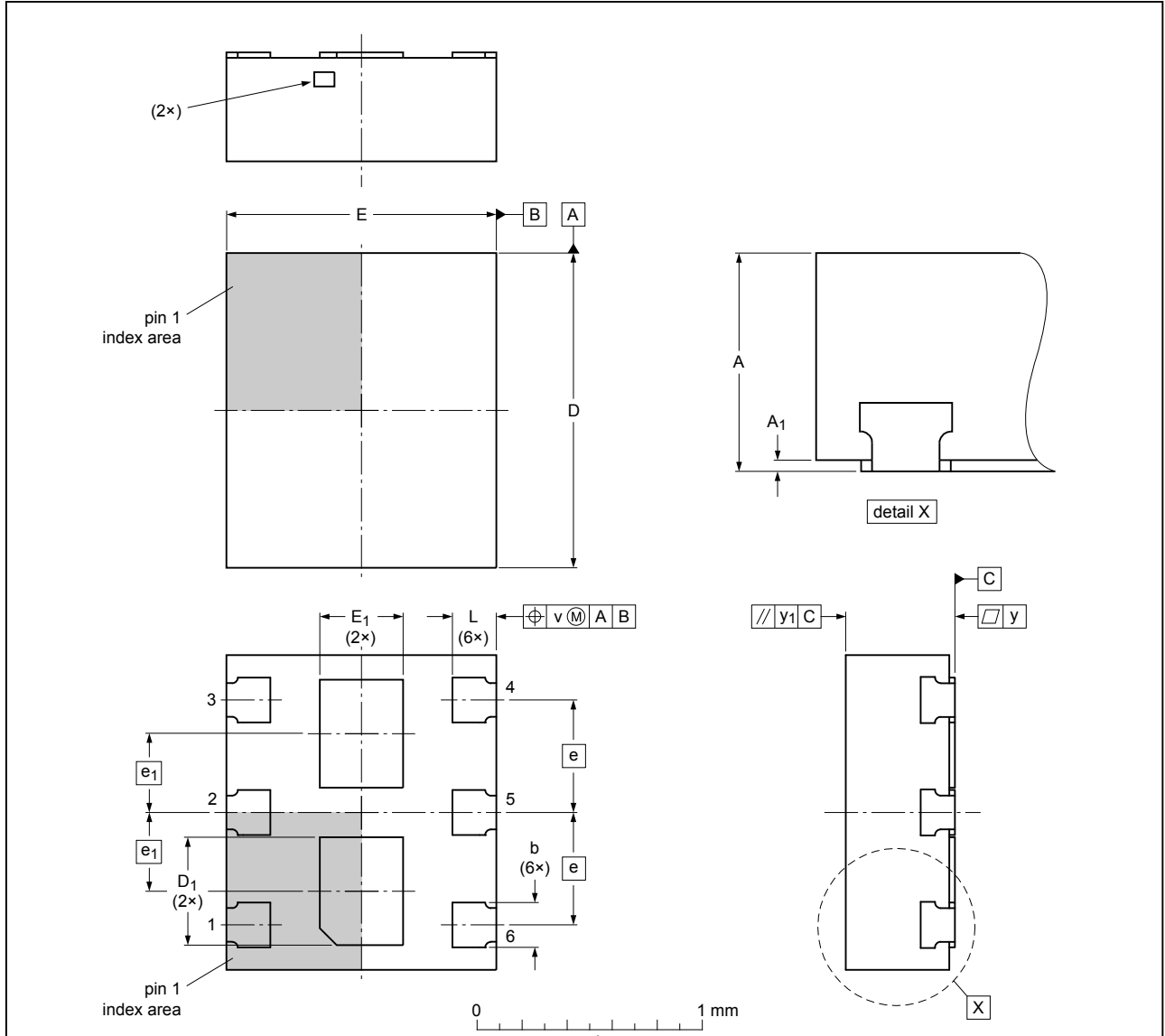
Per transistor; for the PNP transistor with negative polarity

R1 (kΩ)	R2 (kΩ)	Test conditions			
		I ₁	I ₂	I ₃	I ₄
47	47	55 μA	105 μA	-55 μA	-150 μA

12. Package outline

DFN1412-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body: 1.4 x 1.2 x 0.47 mm

SOT1268



Dimensions (mm are the original dimensions)

Unit ⁽¹⁾	A	A ₁	b	D	D ₁	E	E ₁	e	e ₁	L	V	Y	Y ₁
min	0.44	0.00	0.15	1.35	0.43	1.15	0.32			0.145			
mm nom	0.47		0.20	1.40	0.48	1.20	0.37	0.5	0.35	0.195	0.1	0.05	0.05
max	0.50	0.04	0.25	1.45	0.53	1.25	0.42			0.245			

Note

1. Dimension A is including plating thickness.

sot1268_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1268	---	---	---		-16-02-25- 16-09-02

Fig. 19. Package outline DFN1412-6 (SOT1268)

13. Soldering

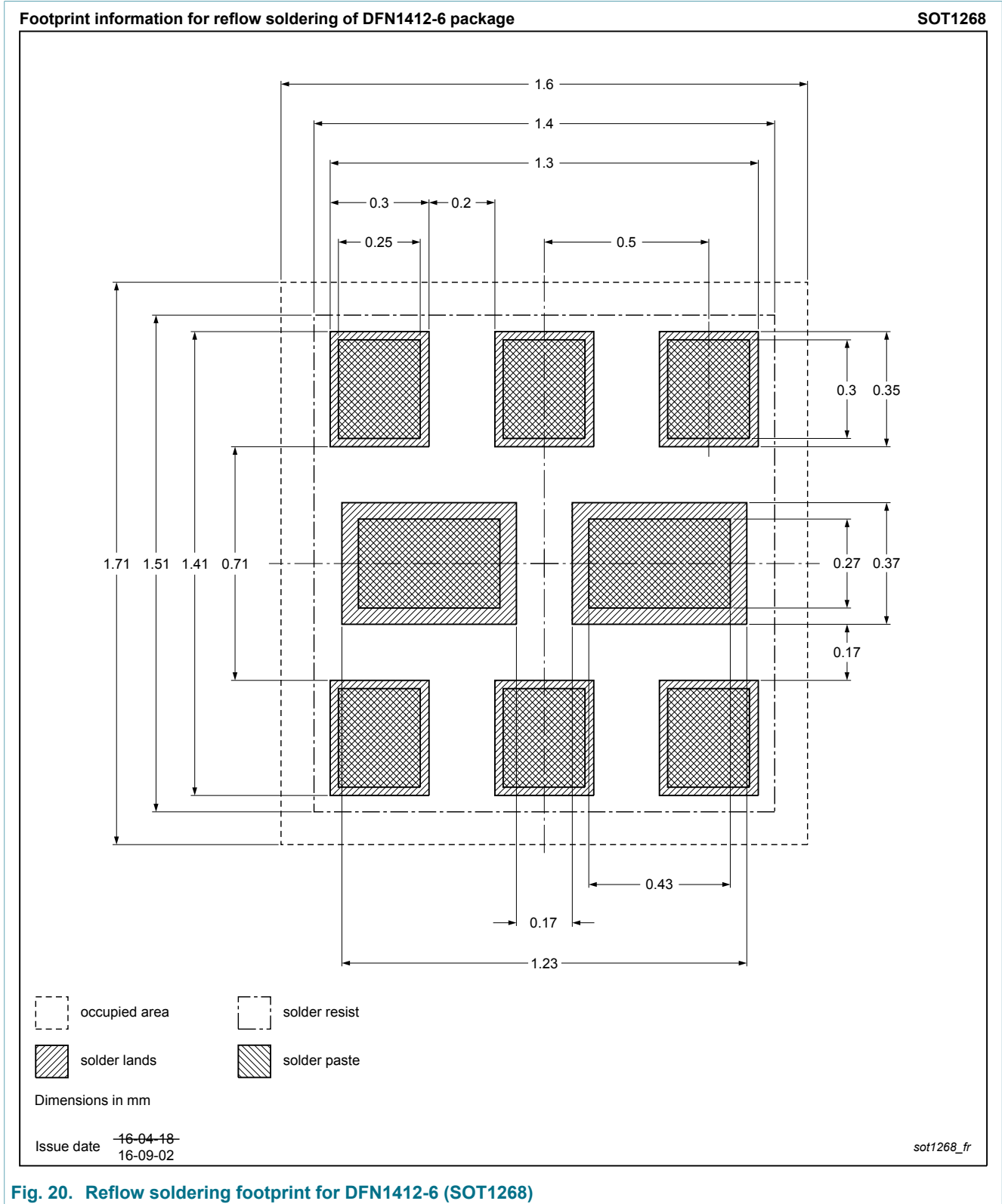


Fig. 20. Reflow soldering footprint for DFN1412-6 (SOT1268)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PRMD12 v.1	20170711	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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