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PICOSTRAIN

Digital Amplifier for Strain Gages

PS021

Datasheet

02ND JUNE 2006

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Precision Time Interval Measurement

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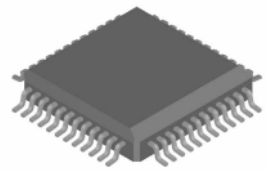
1. Introduction

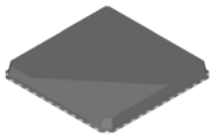
1.1 System Overview

PSØ21 is the newest front-end device out of the PICOSTRAIN® product family. PICOSTRAIN stands for a new digital concept to measure metal strain gages (SG). It is based on TDC technology (Time-to-Digital Converter). The digital measurement principle allows a high degree of flexibility. The current consumption of the total system, including the sensor, can be reduced down to less than 100 µA. The precision to be achieved is comparable to high-end 24-Bit A/D-converters and even surpasses them at high measurement rates. It has a serial interface, SPI® compatible, to communicate with a microcontroller or DSP.

The PSØ21 is downwardly compatible to the PSØ2. Hard-and software for PSØ2 can also be used with PSØ21.



TQFP 48
PSØ21



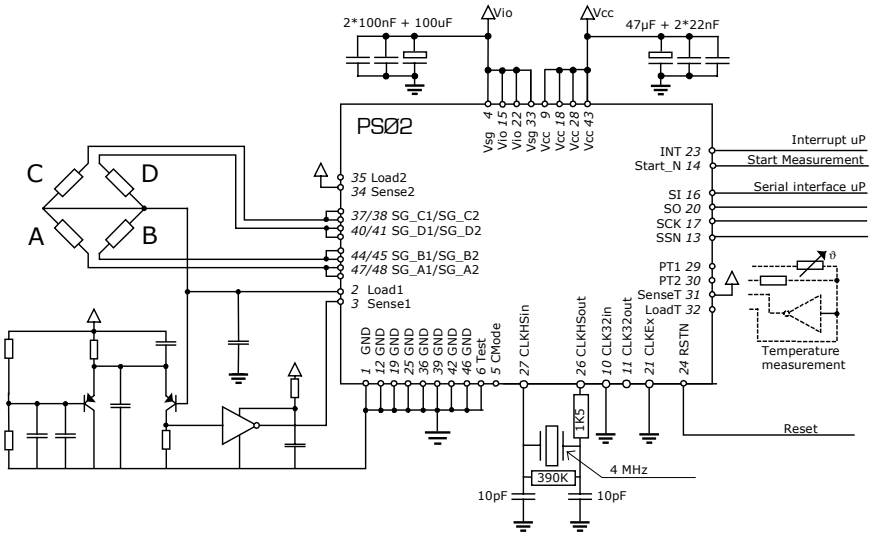
QFN7-48
PSØ21FN

Features

- Digital measuring principle in CMOS technology
- Up to 2 full- or 4 halfbridges
- Optional mode for Wheatstone bridges
- Compensated or non-compensated bridges
- Adaptation of compensation resistor's Tk by software
- Offset and span compensation internally separated (mathematically), therefore no need to trim the bridge offset
- Capable of driving only a halfbridge without any loss in precision
- Resistance strain gauge: 350 Ohm – 10 kOhm
- Programmable resolution:
  Up to 19 Bit (20nV rms or 500,000 scale div)
  @ 2 mV/V strain and 5 Hz update rate
- High Measurement rate:
  Up to 50 kHz with high resolution
  (12.4 ENOB @ 4 kHz and 2 mV/V max. strain)
- Extremely low current consumption possible: Down to 15 µA (incl. SG) at 1 Hz and 10 ENOB with 1 kOhm SG and 1000 µ strain
- High stability with temperature, low gain error (< 1 ppm/K)
- No need for a pre-amplifier
- No separate supply of SG
- No separate reference voltage
- Optional Single-conversion mode
- Separate temperature measurement
- Optional capacitor measurement
- Serial interface (SPI compatible)
- Supply voltage I/O and SG: 1.8 ... 5.5 V
- Separate Supply for interface I/Os
- Supply voltage PSØ21: 1.8 ... 3.6 V
- Op. temperature range –40°C ... +120°C
- QFN48 / QFP48 package (body size 7 x 7 mm²)

Applications

- Scales and load cells
- Force sensors
- Pressure sensors (also 4 – 20 mA)
- SG-amplifiers in general
- Solar cell driven devices
- Battery driven devices
- Wireless applications



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1.3 Structure of the datasheet

This functional description is made of several main sections for easy implementation of the PSØ21.

These main sections are:

2. Technical Characteristics

This main section is for reference with all the important technical data in a brief. Pinning, operating conditions and timings are shown. Several tables give an overview about the read and write register as well as a short description of the different bits. This section provides technical reference for the engineer actually working on the design-in of this product.

3. General Introduction

This main section is a general introduction into the field of measuring strain gauges. Some fundamental terms are introduced, which will be used frequently in this manual. We mainly explain the basics of the **PICO**STRAIN measuring principle and it's specialties.

4. Description of Basic Functions

Here the user finds everything to successfully start a first application with PSØ21. This section is important for anyone working with PSØ21 for the first time.

5. Details and Special Functions

In this section special functions and control bits are discussed. It provides information for those who want to optimize the maximum performance of the PSØ21. Things like temperature measurement and the calculation of the current consumption can be found here.

6. Special Modes

This section treats mainly measurement range 1 and capacity measurement.

7. How to get the best performance

This section gives hints what to do to get get the highest possible performance out of the PSØ21.

8. Applications

This section shows some typical application examples with schematics and configuration.

9. Background

This section gives some general background information about TDCs, strain gage measurement...

2 Characteristics and Specifications

2.1 Absolute Maximum Ratings

Supply voltage

Vcc vs. GND	-0.3 to 4	V
Vio, Vsg vs. GND	-0.3 to 7	V
Current into Output-Pin (Iout)	±30	mA
Storage temperature (Tstg)	-65 to 150	°C
Junction temperature (Tj) max.	125	°C

2.2 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{cc}	Core supply voltage	$V_{io} > V_{cc}$	1.8		3.6	V
V_{io}	I/O supply voltage		1.8		5.5	V
V_{sg}	Strain gage supply voltage		1.8		5.5	V
t_{ri}	Normal Input Rising Time				50	ns
t_{fa}	Normal Input Falling Time				50	ns
t_{ri}	Schmitt Trigger Rising Time				5	ms
t_{fa}	Schmitt Trigger Falling Time				5	ms
T_a	Ambient Temperature		-40		120	°C

2.3 Electrical Characteristics

At Vcc=3.3 V ± 0.3 V, Ambient temperature –40 °C ... +85 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_q	Quiescent current 32 kHz	I_{cc} + I_{io}, only 32kHz oscillator running, V_{cc}=V_{io}=3V		5		µA
I_q	Quiescent current 4 Mhz	I_{cc} + I_{io}, only ClkHS running at 4MHz, V_{cc}=V_{io}=3V		150		µA
I_l	Input Leakage Current		-1		+1	µA
V_{oh}	High Level Output Voltage	I_{oh}= tbd mA V_{io}=Min.	Vio-0.4			V
V_{ol}	Low Level Output Voltage	I_{ol} = tbd mA, V_{io}=Min			0.4	V
V_{ih}	High Level Input Voltage	LVTTL Level, V_{io} = Max.	2.0			V
V_{il}	Low Level Input Voltage	LVTTL Level, V_{io} = Min.			0.8	V
V_{th}	High Level Schmitt Trigger Voltage		1.1		2.4	V
V_{tl}	Low Level Schmitt Trigger Voltage		0.6		1.8	V
V_h	Schmitt Trigger Hysteresis		0.1			V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{pu}	Pull Up Resistor	V_i=0V	20		200	kΩ
R_{pd}	Pull Down Resistor	V_i=Vcc	20		200	kΩ
C_i	Input Terminal Capacitance	f=1MHz, V_{cc}=0V			10	pF
C_o	Output Terminal Capacitance	f=1MHz, V_{cc}=0V			10	pF
C_{io}	Input/Output Terminal Cap.	f=1MHz, V_{cc}=0V			10	pF
t(POR)	Time delay Power-on Reset	From rising edge of WRN			360	ns

2.4 System Performance

At Vcc=3.3 V ± 0.3 V, Ambient temperature –40 °C ... +85 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INL	Integral Non-linearity strain			t.b.d.		% of FS
	Offset	Initial, uncalibrated		± 50		µV
	Offset drift	total system, 1kOhm DMS, 5V				
		Fullbridge		5		nV/K
		Halfbridge		80		nV/K
	Gain drift over -40°C ... 120°C	total system, 1kOhm DMS, 5V		1		ppm /K
PSRR1[1]	Power Supply Rejection Ratio Vio	Halfbridge[2] Vio 3 V or 5 V ±10%		120		dB
PSRR2[1]	Power Supply Rejection Ratio Vio	Fullbridge[2] Vio 3 V or 5 V ±10%		>140		dB
CMRR	Common Mode Rejection Ratio Vcc	Cannot be defined for PICOSTRAIN measuring principle		120		dB

[1] PSRR= -20*log(dVdd/dVout)

[2] Variation Vsg from 3 V to 5 V, Vcc from 2.5 V to 3.3 V

2.4.1 Measurement Capability

The following tables show the measurement capabilities for different supply voltages for the strain gage and the PSØ21 core.
All data shown include a SINC3 filter. For getting the data with fast-settle mode multiply the noise values by 1.73 or reduce the #LSB values by 0.8 Bit.
The data refer to the comparator circuit shown in Figure 21.

All measurements are done with a 1 kΩ fullbridge modified for **PICO**STRAIN.

Table 1: Measurement range 2, Vsg = 5.0 V, Vcc = 3.3 V

Measuring Rate in Hz	ENOB			No. of LSB's	Noise	
	SG Ratio	2 mV/V FS	3,3 mV/V FS	@ 2 mV/V	µV	ppm
*50.000	18,3	9,3	10,0	625	16.000	3,200
*35.000	18,4	9,4	10,1	695	14,400	2,880
*20.000	19,4	10,4	11,1	1.333	7,500	1,500
10.000	20,8	11,8	12,5	3.400	2.900	0,580
4.000	22,2	13,2	13,9	9.500	1,050	0,210
2.000	22,9	13,9	14,6	15.100	0,660	0,132
1.000	23,5	14,5	15,2	22700	0,440	0,088
500	24,0	15,0	15,7	32.700	0,305	0,061
250	24,5	15,5	16,2	47.600	0,210	0,042
100	25,3	16,3	17.0	83.000	0,120	0,024
50	25,8	16,8	17,5	117.000	0,085	0,017
20	26,5	17,5	18,2	192.000	0,055	0,010
10	27,1	18,1	18,8	277.000	0,036	0,007
5	27,5	18,5	19.2	384.000	0,028	0,005
2	28.1	19.1	19,8	555.000	0,018	0,004

SG Ratio: Resolution referred to resistance ratio of the SG
2mV/V: Resolution referred to 2mV/V maximum output (Full Scale)
3.3 mV/V: Resolution referred to 3.3mV/V maximum output (Full Scale)
***measured in measuring range 1**

Table 2: Measurement range 2, Vsg = 3.0 V, Vcc = 3.0 V

Measuring Rate in Hz	ENOB			No. of LSB's	Noise	
	SG Ratio	2 mV/V FS	3,3 mV/V FS	@ 2 mV/V	µV	ppm
*50.000						
*35.000						
*20.000						
10.000	20,5	11,5	12,2	2850	2,100	0,700
4.000	22.0	13.0	13.7	8.000	0,750	0,250
2.000	22.5	13.5	14.2	11.700	0,510	0,170
1.000	22.9	13.9	14.6	15.700	0,380	0,126
500	23.5	14.5	15,2	23.000	0,260	0,086
250	24,0	15,0	15.7	34.200	0,175	0,058
100	24.8	15.8	16.5	57.000	0,105	0,035
50	25.3	16.3	17.0	80.000	0,075	0,025
20	26.0	17.0	17.1	136.000	0,044	0,015
10	26.4	17.4	18.1	176.000	0,034	0,011
5	27.0	18.0	18.7	250.000	0,024	0,008
2	27.3	18.3	19.0	333.000	0,018	0,006

* measured in measuring range 1

Table 3: Measurement range 2, Vsg = 2.0 V, Vcc = 2.0 V

Measuring Rate in Hz	Eff. Bits			No. of LSB's	Noise	
	SG Ratio	2 mV/V FS	3,3 mV/V FS	@ 2 mV/V	µV	ppm
10.000	19,5	10,5	11,2	1.430	2,800	1,400
4.000	21,3	12,3	13,0	5.100	0,780	0,390
2.000	21.7	12.7	13.4	7.000	0,570	0,285
1.000	22.0	13.0	13.7	8.000	0,500	0,250
500	22,6	13,6	14.3	12.500	0,320	0,160
250	23.3	14.3	15.0	20.000	0,200	0,100
100	24.0	15.0	15.7	32.000	0,125	0,062
50	24.5	15.5	16.2	48.000	0,082	0,041
20	25.2	16.2	16,9	77.000	0,052	0,026
10	25.8	16.8	17.5	114.000	0,035	0,017
5	26.3	17.3	18.0	166.000	0,024	0,012
2	26.7	17.7	18.4	210.000	0,019	0,009

2.4.2 Offset and Gain Error

Figure 1: Offset drift of the complete electronics[1] in temperature range –20°C to 90°C
Vsg = Vcc = 3V, 1kOhm SG with 0 mV/V strain
Offset drift halfbridges: 55 nV/K; Offset drift fullbridge: < 2 nV/K

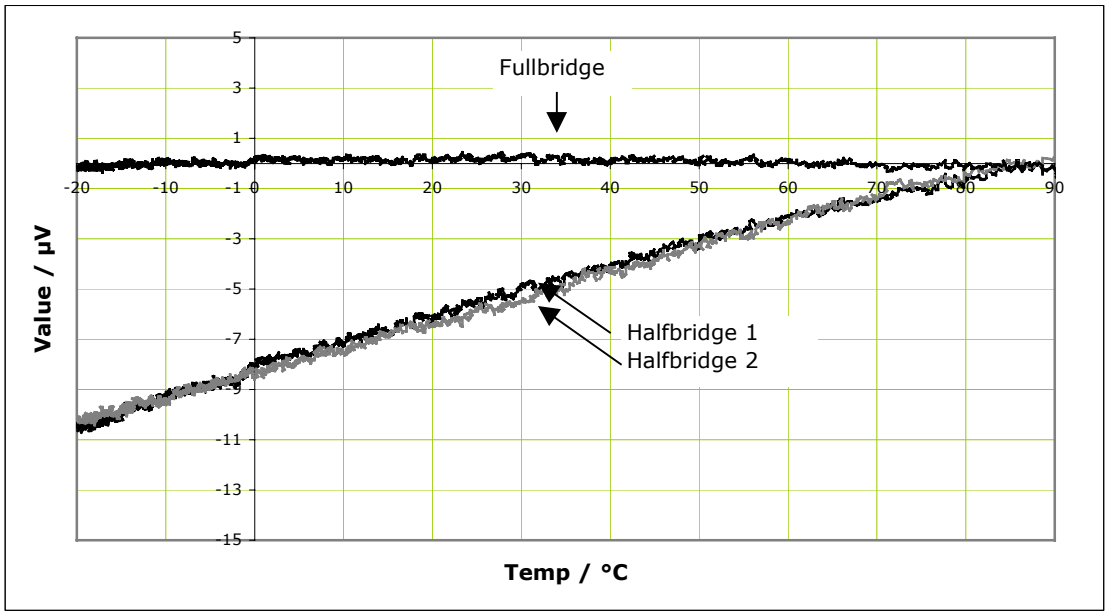
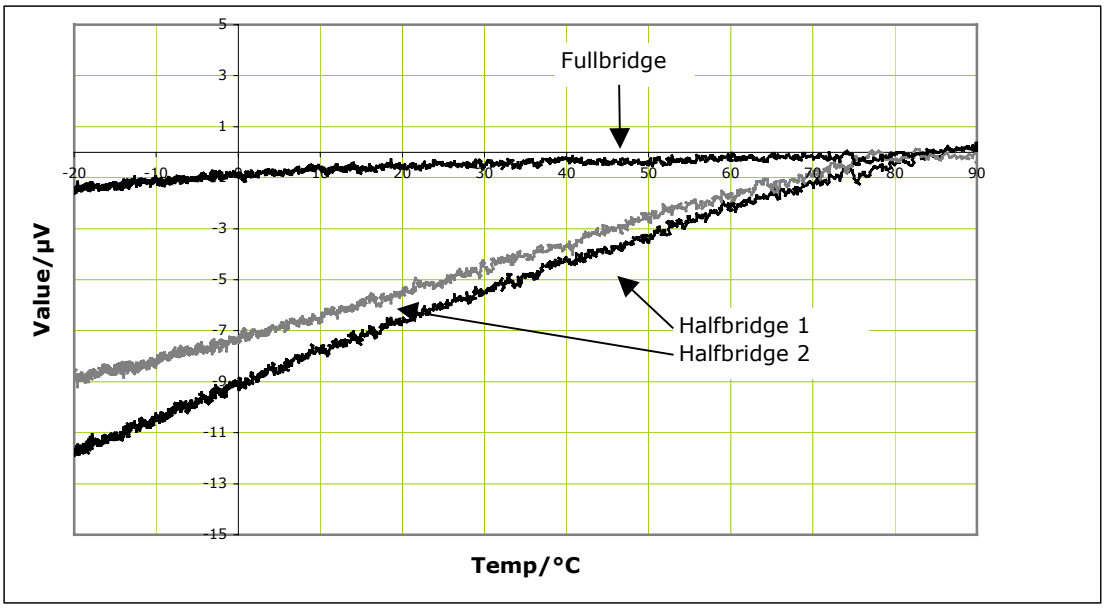


Figure 2: Gain+Offset drift complete electronics[1] in ppm of max. strain in temperature range –20°C to 90°C
Vsg = Vcc = 3V, 1kOhm SG with 2,5mV/V strain
Gain+Offset drift HB1: 1,02 ppm/K; HB2: 1,16 ppm/K; Fullbridge: < 2 nV/K



[1] measured with PSA2 evaluation board, SG temperature constant

2.4.3 Current consumption

The following graphs refer to the **total** current, which is the current into the strain gage and into PSØ21 incl. the comparator.

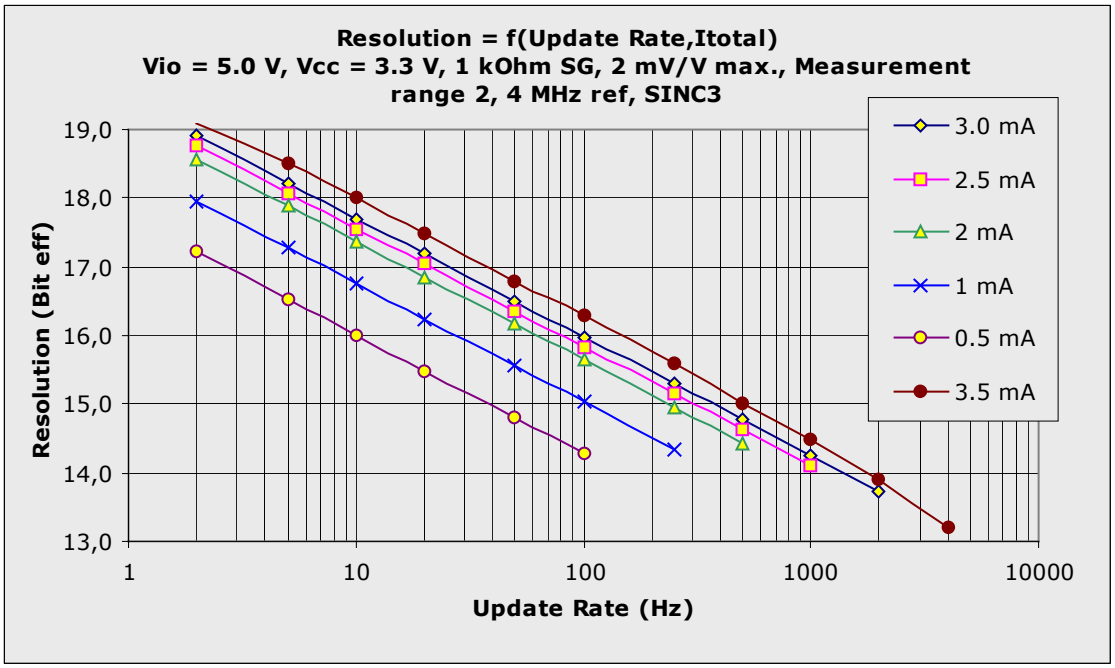


Figure 3: Vsg = 5 V (Strain gage), Vcc = 3.3V (PSØ21)

2.5 Timings

At Vcc=3.3V ± 0.3V, ambient temperature -40°C ... +85°C unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units
	Oscillator				
Clk32	32 kHz reference oscillator		32,768		kHz
t_{oszst}	Oscillator start-up time with ceramic resonator		150		µs
t_{oszst}	Oscillator start-up time with crystal oszillator		700		
ClkHS	High-speed reference oscillator	2	4	5	MHz
ClkEx	External high-speed reference clock input	2	4	5	MHz
	Serial interface	Max @ V_{io} =			
		1.8V	3.3V	5V Vio	
f_{clk}	Serial clock frequency	-	10	20	MHz
		Min @ V_{io} =[1]			
		1.8V	2.2V	3.0V	4.5V[2]
t_{pwh}	Serial clock, pulse width high	80	50	30	25	ns
t_{pwl}	Serial clock, pulse width low	80	50	30	25	ns
t_{sussn}	SSN enable to valid latch clock	20	10	8	7	ns
t_{pwssn}	SSN pulse width between write cycles	100	50	30	25	ns
t_{sud}	Data set-up time prior to SCLK falling	15	7	6	5	ns
t_{hd}	Data hold time before SCLK falling	10	5	4	3	ns
		Max @ V_{io} =			
		1.8V	2.5V	3.3V	5V	
t_{vd}	Data valid after SCLK rising	tbd.	40	26	18	ns

[1] Worst case at supply voltages 2.5V, 3.3V and 5V

[2] Core-Voltage Vcc=3.3V

Serial Interface (SPI compatible, Clock Phase Bit =1, Clock Polarity Bit =0)**:**

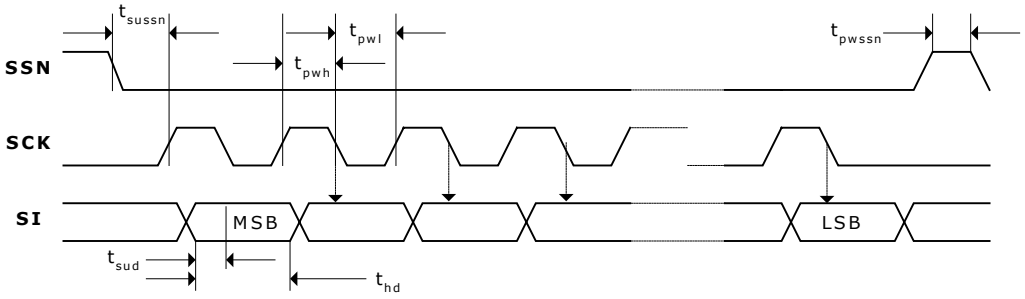


Figure 4: Write

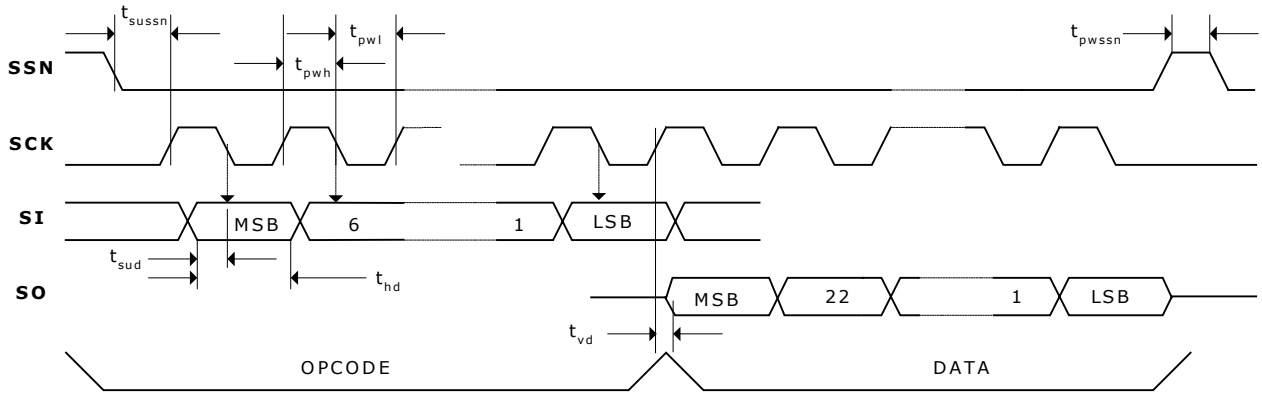


Figure 5: Read

Table 4: OP-Codes

8 Bit OP Code								
MSB							LSB	Description
1	0	0	0	ADR3	ADR2	ADR1	ADR0	Write into 24 Bit register at address
1	0	1	1	0	ADR2	ADR1	ADR0	Read 24 Bit register from address
1	0	1	1	1	ADR2	ADR1	ADR0	Read 24 Bit register from address, autoincrement address
1	1	0	0	0	0	0	0	Init
0	1	0	1	0	0	0	0	Power On Reset
0	0	0	0	0	0	0	1	Start measurement
0	0	0	0	1	0	0	0	Select Double Bridge 1
0	0	0	0	1	0	0	1	Select Double Bridge 2
0	1	1	ADR4	ADR2	ADR3	ADR1	ADR0	Write {Reg4, Reg5} to RAM address

2.6 Pin Configuration

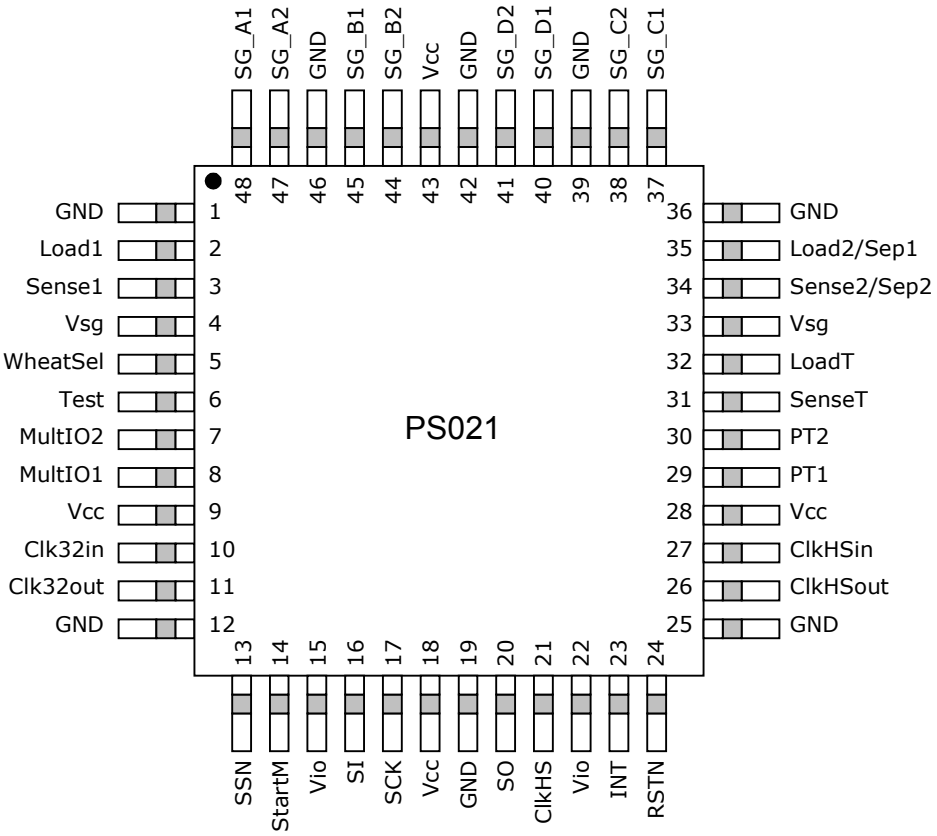


Figure 6: Pinning TQFP48 / QFN7-48

Table 5: Pin Descriptions

No.	Name	Description	Value	If not used
1	GND	Ground		
2	Load1	Load output 1		Pins 44, 48,47,48
3	Sense1	Sense input 1		GND
4	Vsg	Strain gage supply voltage		
5	WheatSel	Select for Wheatstone Mux in the comparator		n.c.
6	TestIn	Test-Pin, connect to GND		GND
7	MultIO2	Multifunctional IO		n.c.
8	MultIO1	Multi-funcional IO		n.c.
9	Vcc	Core supply voltage		
10	CLK32in	Input 32kHz clock generator		GND
11	CLK32out	Output 32kHz clock generator		n.c.
12	GND			
13	SSN	Slave Select	Low active	GND
14	StartM	Start new measurement	High active	GND
15	Vio	I/O supply voltage		
16	SI	Input serial interface		

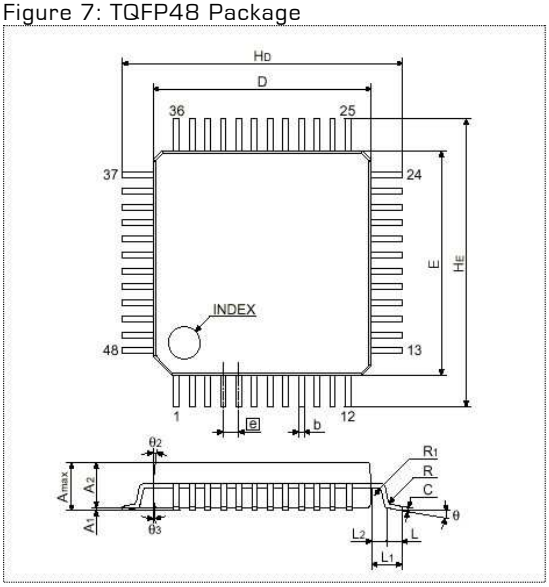
17	SCK	Clock serial interface		
18	Vcc	Core supply voltage		
19	GND			
20	SO	Output serial interface		
21	ClkEx	Input external high-speed reference clock		GND
22	Vio	I/O supply voltage		
23	INTN	Interrupt Flag	LOW active	n.c.
24	RSTN	Reset input	LOW active	Vio
25	GND			
26	ClkHSout	Output high-speed clock generator		n.c.
27	ClkHSin	Input high-speed clock generator		GND
28	Vcc	Core supply voltage		
29	PT1	Port 1 temperature measurement		Pin 32
30	PT2	Port 2 temperature measurement		Pin 32
31	SenseT	Sense input temperature measurement		GND
32	LoadT	Load output temperature measurement		Pins 29, 30
33	Vsg	Strain gage supply voltage		
34	Sense2 Sep1	Sense input 2 Separate compensation		Vsg
35	Load2 Sep2	Load output 2 Separate compensation	one-sense mode: halfbridge:	n.c. Pins 37, 38,40,41
36	GND			
37	SG_C1	Port 1 halfbridge C		Pin 35
38	SG_C2	Port 2 halfbridge C		Pin 35
39	GND			
40	SG_D1	Port 1 halfbridge D		Pin 35
41	SG_D2	Port 2 halfbridge D		Pin 35
42	GND			
43	Vcc	Core supply voltage		
44	SG_B2	Port 2 halfbridge B		Pin 2
45	SG_B1	Port 1 halfbridge B		Pin 2
46	GND			
47	SG_A2	Port 2 halfbridge A		Pin 2
48	SG_A1	Port 1 halfbridge A		Pin 2

2.7 Package Drawings

Table 6: Dimensions TQFP48 package

Symbol	Dimension in Millimeters			Dimension in Inches (*)		
	Min.	Nom.		Max.	Min.	Nom.
E	6,9	7		7,1	(0,272)	(0,276)
D	6,9	7		7,1	(0,272)	(0,276)
A				1,7		
A1		0,1				(0,004)
A2	1,3	1,4		1,5	(0,052)	(0,055)
e		0,5				(0,020)
b	0,13	0,18		0,28	(0,006)	(0,007)
C	0,1	0,125		0,175	(0,004)	(0,005)
θ	0°			10°	(0°)	
L	0,3	0,5		0,7	(0,012)	(0,020)
L1		1				(0,039)
L2		0,5				(0,020)
HE	8,6	9		9,4	(0,339)	(0,354)
HD	8,6	9		9,4	(0,339)	(0,354)
θ2		7°				(7°)
θ3		4°				(4°)
R		0,2				(0,008)
R1		0,2				(0,008)

Figure 7: TQFP48 Package

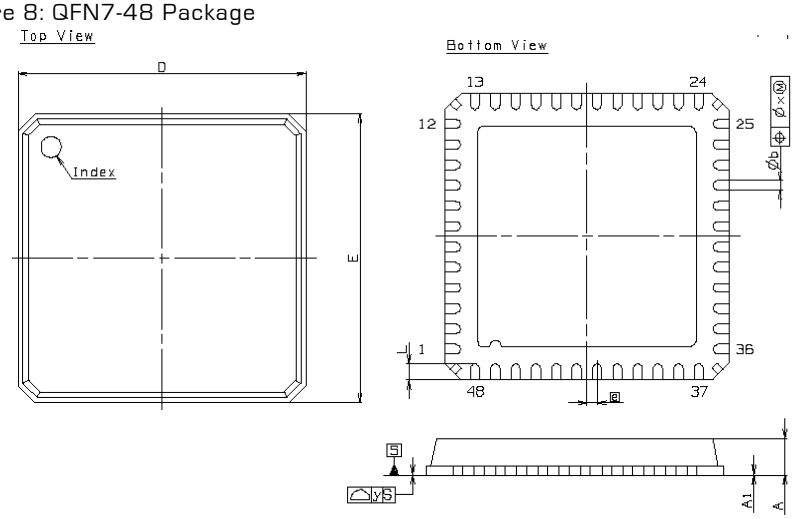


* for reference

Table 7: Dimensions QFN7-48 package

Symbol	Dimension in Millimeters		
	Min.	Nom.	
E		7	
D		7	
A			1.00
A1			0.05
e		0,5	
b	0.18		0.30
L	0.30		0.50
x			0.10
y			0.08

Figure 8: QFN7-48 Package

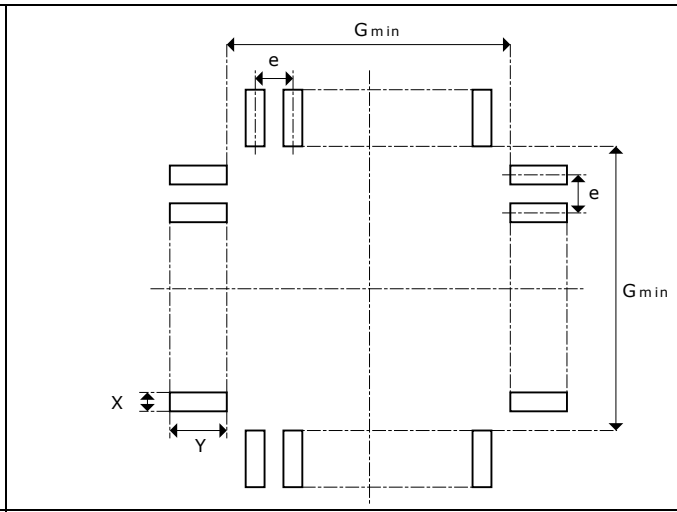


Recommended Foot Pattern

TQFP48

e = 0,5 mm
G_{min} = 7,4 mm
0,2 mm < X < 0,25 mm
Y ≥ 1 mm (2 mm recommended)

Recommended sockets for testing:
Yamaichi IC51-0484-806
Seiko IC51-806.KS11882



QFN7-48

e = 0,5 mm
G_{min} = 5,93 mm
Zmax = 7,31 mm
D2' < 5,63 mm
CPL = mm
CII = mm
Amax = 5,78 mm
X = 0,28 mm
Y = 0,69 mm

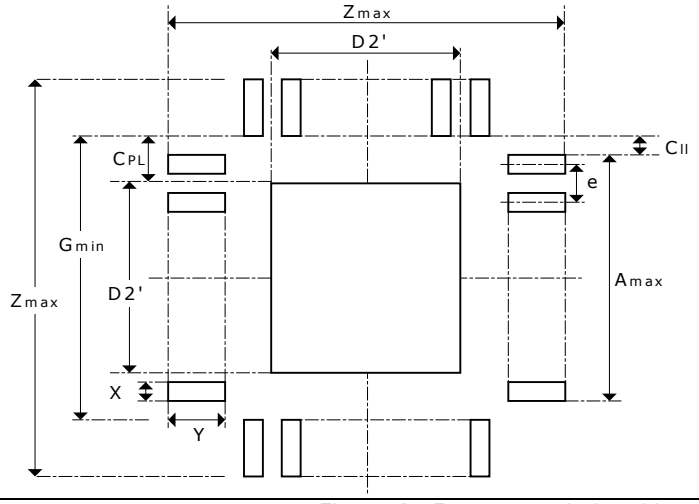


Figure 9: Recommended pad layout

2.8 Registers

2.8.1 Write Registers

Table 8 Write registers (Default values in second row)

Bit	Reg 0		Reg 1		Reg 2		Reg 3		Reg 4		Reg 5		Reg 6		Reg 7	
23	CalAvRate	1	CycleTime	0	RdsonModify	0	Mult1	x	RD1	1	RD2	1	s.c.	0	RunCont	0
22		0		0		1		x		0		0	s.c.	1	Rdson Filter	0
21	RdsonSimple	0		0		0		x		0		0	s.c.	0	s.c.	0
20	ClkHSDiv	0		0		0		x		0		0	s.c.	1	ClkHSring	0
19		0		0	RdsonAvRate	1		x		0		0	s.c.	0	ClkHSon	0
18	Cmeasure	0		0		0		x		0		0	s.c.	0		1
17	MultEN	0		0		0		x		0		0	s.c.	0	s.c.	0
16	SelClk32	1		0		0		x		0		0	Noise1	0	s.c.	0
15	SubFB	0		0	GainAvRate	0		x		0		0	CalDel	0	n.c.	
14	SumFB	0		0		1		x		0		0		1	s.c.	0
13	NegSense2	0		0		0		x		0		0		0	s.c.	0
12	NegSense1	0		1		0		x		0		0		0	s.c.	0
11	NegSenseT	1	AvRate	0	GainCorRate	0		x		0		0	s.c.	0	s.c.	0
10	TempRate	0		0		0		x		0		0	s.c.	1	s.c.	0
9		0		0		0		x		0		0	s.c.	0	s.c.	0
8	DoubleBr	0		0		1		x		0		0	s.c.	1	s.c.	0
7	SubOffset	0		0	PortFilter	0		x		0		0	n.c.		s.c.	0
6	Sinc3	0		0	OffsetAvRate	0		x		0		0	s.c.	0	s.c.	0
5	SingleCon	0		1		1		x		0		0	s.c.	0	s.c.	1
4	HighRes	1		0		0		x		0		0	WarmUp	1	s.c.	1
3	Mrange2	1		0	CalCycle	0		x		0		0		0	s.c.	0
2	HighSpeed	0		0		0		x		0		0		0	s.c.	1
1	Bridge	0		0		1		x		0		0	MFake	0	s.c.	0
0		0		0		0		x		0		0		0	s.c.	1

s.c. = Special acam configuration bits, n.c. = not in use

Bit	Reg 8		Reg 9		Reg 10		Reg 11		Reg 12		Reg 13		Reg 14		Reg 15	
23	SignTG2	0	s.c.	0	SignMult2	0		x		x		x		x		x
22	SignTG1	0	s.c.	0	SignMult1	0		x		x		x		x		x
21	CompSleep	0	s.c.	0	PSØ21_Adj1	0		x		x		x		x		x
20	CompConOn	0	s.c.	0	PSØ21_Adj1	1		x		x		x		x		x
19	CompCon	0	s.c.	0	PSØ21_Adj1	0		x		x		x		x		x
18		0	s.c.	1	PSØ21_Adj1	0		x		x		x		x		x
17		0	s.c.	1	PSØ21_Adj1	0		x		x		x		x		x
16		0	s.c.	0	PSØ21_Adj1	1		x		x		x		x		x
15	PortSw4	1	n.c.	0	Quarterbridge	0		x		x		x		x		x
14		1	n.c.	0	Cal_Adjust	0		x		x		x		x		x
13	PortSw3	1	Cmeas2	0	Cal_Adjust	0		x		x		x		x		x
12		0		0	Cal_Adjust	0	Mult2	x	TKOffs1	x	TKOffs2	x	TKGain1	x	TKGain2	x
11	PortSw2	0	AvRate2	0	Cal_Adjust	0		x		x		x		x		x
10		1		0	Cal_Adjust	0		x		x		x		x		x
9	PortSw1	0		0	Cal_Adjust	0		x		x		x		x		x
8		0		0	Cal_Adjust	0		x		x		x		x		x
7	SpreadRng	0		0	ModSpanByT	0		x		x		x		x		x
6		0		0	ModRSpan	0		x		x		x		x		x
5	SpreadSrc	0		0	LoadStartDel	0		x		x		x		x		x
4		0		0	LoadStart	0		x		x		x		x		x
3	SpreadEN	0		0	PSØ21_Adj2	0		x		x		x		x		x
2	WheatEN	0		0	PSØ21_Adj2	0		x		x		x		x		x
1	SepGain	0		0	PSØ21_Adj2	0		x		x		x		x		x
0	Mult2En	0		0	PSØ21_Adj2	0		x		x		x		x		x

Note:
Registers Mult1, Mult2, TKOffs1, TKOffs2, TKGain1 and TKGain2 are not initialized when a INIT or Power-on reset is done. It is mandatory to write the correct values into these registers before switching on multiplication.

Table 9: Short description of the Bits:

Name	Description	Values
Reg 0		
Bridge <1,0>:	Select bridge mode: One-sense or Alternating mode Halfbridge or fullbridge	[0,0] = Fullbridge, One-sense mode [1,1] = Fullbridge, alt. mode [0,1] = Bridge0 (Ports A, B) [1,0] = Bridge1 (Ports C, D)
HighSpeed:	Select frequency mode in measurement range 1	0 = 32 kHz Clock 1 = ClkHS
Mrange2	Switch PSØ21 to measurement range 2	0 = measurement range 1 1 = measurement range 2
HighRes	Select High-Resolution mode of the TDC time measuring unit	0 = without HighRes 1 = with HighRes
SingleCon	Single-conversion mode	1 = Single-conversion on

Sinc3	Switch-on SINC3 filter	0 = Fast settle 1 = SINC3-Filter on
SubOffset	Select Auto-offset calculation	1 = with Auto-offset
DoubleBr	Switch to doublebridge mode	
TempRate	Controls temperature measurement	0 = off 1 = each AVRate 2 = each 6th AVRate 3 = each 9th AVRate
NegSenseT	Negation SenseT input	0 = falling edge
NegSense1	Negation Sense1 input	0 = falling edge
NegSense2	Negation Sense2 input	0 = falling edge
SumFB	Select summation in fullbridge mode	HB1 + HB2
SubFB	Select difference in fullbridge mode	HB2 – HB1
SelClk32	Use 32 kHz clock as cycle clock	1 = on, MRange 1 only
MultEN	Switch-on multiplication	1 = on
Cmeasure	Switch-on capacity measurement	1 = on
ClkHSDiv	Sets predivider for CLKHS Mrange2: TDC range = max. discharge time = $Tref * 2^{ClkHSDiv} * 2^{8}$ ClkHSDiv = 1 is recommended	0 = divided by 1 1 = divided by 2 2 = divided by 4 3 = divided by 8
RdsonSimple	Enable simplified Rdson correction	1 =on
CalAvRate	Sets the averaging rate of the calibration value in measurement range 2	0 = 1 1 = 8 2 = 32 3 = 64

Reg 1		
AVRate	Averaging rate for a single measurement	1 ... 4095
CycleTime	Cycle time in multiples of the reference clock for the cycle time	1 ... 4095

Reg 2		
CalCycle	Sets the number of cycles before the TDC does a calibration measurement	1 = each cycle 2 = each 2nd ... 15 = each 15th
OffsetAVRate	Averaging rate of Auto-offset measurements	1 = 1 2 = 2 3 = 4 ... 7 = 128
PortFilter	Additional Filter	1 = on (is recommended)
GainCorRate	Sets the repetition rate of gain compensation measurements in multiples of AVRate	0 = off (no gain compensation) 1 = each AVRate 2 = each 2nd ... 15 = each 15th
GainAVRate	Averaging rate of gain compensation	1 = 1 2 = 2 3 = 4 ... 15 = 16284

RdsonAVRate	Averaging rate Rdson compensation	1=1 2=2 3=4 ... 15=16284
RdsonModify	Modification of Rdson calculation after an INIT	Use default value

Reg 3		
Mult1	Multiplication factor, fixed-point number with 8 integer and 16 fractional digits	Mult1 = Register3/2^{16} = 0 ... 255.9999

Reg 4		
RD1	Write-back register Rdson halfbridge1	Use default value 0x800000

Reg 5		
RD2	Write-back register Rdson halfbridge2	Use default value 0x800000

Reg 6		
Mfake	Number of dummy cycles at the beginning of an AVRate measurement	0 = 0 1 = 1 2 = 2 3 = 4
WarmUp	Number of dummy cycles after an INIT	0 = off 1 = 16 2 = 32 3 = 64 ... 7 = 1024
CalDel	Controls point in time of calibration in multiples of the ClkHS/ClkEx period after start of capacitor discharge	CalDel: 0, 1, 2, ..., 15 # of periods: don't use, 4, 5, ..., 18
Noise1	Modifies the internal noise generator	0 = on

Reg 7		
ClkHSon	Switch-on high-speed oscillator	0 = Oscillator off 1 = Oscillator on 2 = settling time = 640 µs 3 = settling time = 1280 µs
ClkHSring	Switch-on internal ring-oscillator	1 = ring oscillator on
RdsonFilter	Switch-on spike filter for Rdson compensation	1 = Filter on
RunCont	Runtime of internal ring-oscillator	0 = if required 1 = continuously

Reg 8		
Mult2EN	Enable 2nd multiplication factor for 2nd halfbridge or 2nd fullbridge	1 = on

SepGain	Switch to separate gain compensation resistors	1 = on, mandatory in Wheatstone mode
WheatEN	Switch to Wheatstone mode	1 = on
SpreadEN	Enable adding noise to the cycle time	1 = on
SpreadSrc	Select source of noise generator	0 = each cycle 1 = each 8th cycle 2 = each interrupt 2 = interrupt
SpreadRng	Sets the range of the cycle time noise	0 = 0 cycle 1 = add noise to 4 cycles 2 = add noise to 8 cycles 3 = add noise to 16 cycles
PortSw1	Free assignment ports to pins 48,47	00 = SG_A1,SG_A2 01 = SG_B1,SG_B2 10 = SG_C1,SG_C2 11 = SG_D1,SG_D2
PortSw2	Free assignment ports to pins 45,44	
PortSw3	Free assignment ports to pins 41,40	
PortSw4	Free assignment ports to pins 37,38	
CompCon	Comparator control bits	
CompConOn	Selects 'switched Comparator'	1 = on
CompSleep	Sets external comparator to sleep mode	1 = on
SignTG1, SignTG2	Sign of correction for span compensation resistors	

Reg 9		
AvRate2	Averaging rate for the 2nd bridge in doublebridge mode	0 = off, 2nd bridge uses AvRate
Cmeas2	Switch for capacity measurement with external multiplexer	0 = off 1 = on without compensation 2 = on with compensation, analog Mux with enable 3 = on with compensation, 2 single analog switches

Reg 10		
LoadStart	Start measurement through load pin (not the port pins)	1 = on (recommended)
LoadStartDel	Sets delay with LoadStart	0 = about 25 ns typ. 1 = about 140ns Typ.
ModRSpan	Software adaptation of the bridges Span resistor Rspan	1 = on, recommended for bridges with Rspan
ModSpanByT	Replace Rspan with temperature measurement value	1 = on
SignMult2, SignMult1	Signs for the multiplication factors	0 = positive 1 = negative

Reg 11		
Mult2	Multiplication factor, fixed-point number with 8 integer and 16 fractional digits	Mult1 = Register3/2^{16} = 0 ... 255.9999

Reg 12		
TkOffs1	Offset factor for 1st fullbridge in ppm	16 Bit integer, 8 Bit fractional

Reg 13		
TkOffs2	Offset factor for 2nd fullbridge in ppm	16 Bit integer, 8 Bit fractional

Reg 14		
TkGain1	Multiplication factor Rspan 1st fullbridge	8 Bit integer, 16 Bit fractional

Reg 15		
TkGain2	Multiplication factor Rspan 2nd fullbridge	8 Bit integer, 16 Bit fractional

2.8.2 Read Registers / Ouput Data Formats

Table 10: Read Registers

ADR	Symbol	Bits	Description								
0	HB1	24	Result halfbridge 1, fixed-point no. with 16 integer digits, 8 fractional digits								
1	HB2	24	Result halfbridge 2, fixed-point no. with 16 integer digits, 8 fractional digits								
2	STAT/ TMP	24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Bit 15...0
			Double Bridge	TMP	Error PLL1	Error PLL2	Error DSP	Timeout TMP	Timeout HB2	Timeout HB1	Temperature result
3	REG 0	24	Content of write register 0, to be used for testing the communication								
4	TDC1	24	TDC result								
5	TDC2	24	TDC CAL value in measuring range 2								
6	RD1	24	Rdson configuration value to be written into register 4								
7	RD2	24	Rdson configuration value to be written into register 5								

- **Result registers HB1 and HB2**
  The contents of registers HB1 and HB2 depend on the operating mode:

a. Without Doublebridge

Table 11:

Bridge[1:0]	SumFB	SubFB	Content HB1	Content HB2
0 or 3	0	0	HB1	HB2
1	0	0	HB1	-----
2	0	0	-----	HB2
0 or 3	1	0	-----	HB1 + HB2
0 or 3	0	1	-----	HB2 – HB1

b. With Doublebridge

Table 12:

Bridge[1:0]	SumFB	SubFB	DBStat	Content HB1	Content 2
0 or 3	0	0	0	HB1 of FB1	HB2 of FB1
1	0	0	X	HB1 of FB1	HB2 of FB1
2	0	0	X	HB1 of FB2	HB2 of FB2
0 or 3	1	0	0	-----	(HB1 + HB2) of FB1
0 or 3	0	1	0	-----	(HB2 - HB1) of FB1
0 or 3	0	0	1	-----	HB2 of FB2
0 or 3	1	0	1	-----	(HB1 + HB2) of FB2
0 or 3	0	1	1	-----	(HB2 - HB1) of FB2