Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# Quad Power Sequencing Controller

## Features

- Sequencing of four supplies, ICs, or subsystems
- Independently programmable delays between open drain PWRGD flags (5.0 to 200ms)
- ±10 to ±90V operation
- Tracking in combination with Schottky diodes
- Input supervisors including:
  - UV/OV lock out/enable
  - Power-on-Reset (POR)
- Low power consumption, 0.4mA supply current
- Available in a space saving 14-Lead SOIC package

## Applications

- Power supply sequencing
- -48V telecom and networking distributed systems
- -24V cellular and fixed wireless systems
- -24V PBX systems
- +48V storage systems
- FPGA, microprocessor tracking
- Industrial/embedded system timing/sequencing
- High voltage MEMs driver's supply sequencing
- High voltage display driver's supply sequencing

## General Description

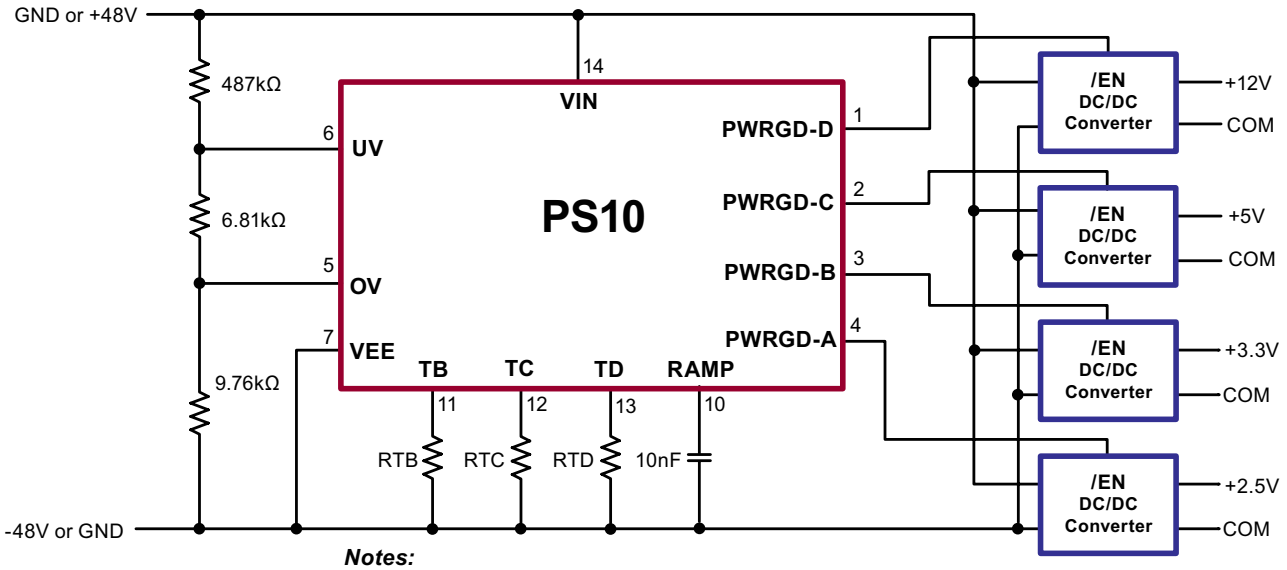
Many of today's high performance FPGA's, microprocessors, DSP and industrial/embedded subsystems require sequencing of the input power. Historically this has been accomplished by: i) discretely using comparators, references & RC circuits; ii) using expensive programmable controllers; or iii) with low voltage sequencers requiring resistor drop downs and several high voltage optocoupler or level shift components.

The PS10 saves board space, improves accuracy, eliminates optocouplers or level shifts and reduces overall component count by combining four timers, programmable input UV/OV supervisors, a programmable POR, and four 90V open drain outputs. A high reliability, high voltage, junction isolated process allows the PS10 to be connected directly across the high voltage input rails.

The power-on-reset interval (POR) may be programmed by a capacitor on $C_{RAMP}$. To sequence additional systems, multiple PS10s may be daisy-chained together. If at any time the input supply falls outside the UV/OV detector range, the PWRGD outputs will immediately become IN-ACTIVE.

The PS10 is available in a space saving 14-Lead SOIC package.

## Typical Application Circuit




***Notes:***

*1. Under Voltage Shutdown (UV) set to 37V.*

*2. Over Voltage Shutdown (OV) to 57.8V.*

## Ordering Information

| Part Number | Package Option | Packing |
|---|---|---|
| PS10NG-G | 14-Lead SOIC | 53/Tube |
| PS10NG-G-G M905 | 14-Lead SOIC | 2500/Reel |

*-G indicates package is RoHS compliant ('Green')*

## Absolute Maximum Ratings

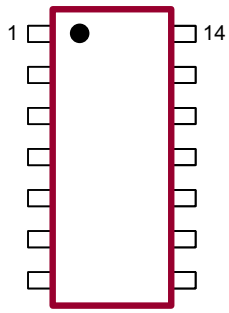
| Parameter | Value |
|---|---|
| $V_{EE}$ referenced to VIN pin | +0.3V to -100V |
| $V_{PWRGD}$ referenced to $V_{EE}$ voltage | -0.3V to +100V |
| $V_{UV}$ and $V_{OV}$ referenced to $V_{EE}$ voltage | -0.3V to 12V |
| Operating ambient temperature | -40°C to +85°C |
| Operating junction temperature | -40°C to +125°C |
| Storage temperature range | -65° to +150°C |
| Power dissipation @ 25°C | 750mW |

*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.*

## PWRGD Logic

| Condition | PWRGD-A/B/C/D | |
|---|---|---|
| Inactive (not ready) | 0 | $V_{EE}$ |
| Active (ready) | 1 | Hi Z |

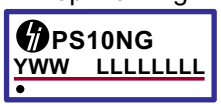
## Pin Configuration



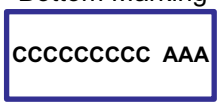

**14-Lead SOIC**
***(top view)***

## Product Marking

Top Marking




Bottom Marking




Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin
A = Assembler ID*
____ = "Green" Packaging

**May be part of top marking*

*Package may or may not include the following marks: Si or*

**14-Lead SOIC**

## Typical Thermal Resistance

| Package | $\theta_{ja}$ |
|---|---|
| 14-Lead SOIC | 75°C/W* |

## Electrical Characteristics *(-10V ≤ $V_{IN}$ ≤ -90V, $T_A$ = 25°C unless otherwise specified)*

| Sym | Parameter | | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| **Supply** *(Referenced to VIN pin)* | | | | | | | |
| $V_{EE}$ | Supply voltage | - | -90 | - | -10 | V | --- |
| $I_{EE}$ | Supply current | - | - | 400 | 450 | µA | $V_{EE}$ = -48V |
| **OV and UV Control** *(Referenced to VEE pin)* | | | | | | | |
| $V_{UVH}$ | UV high threshold | # | 1.16 | 1.22 | 1.28 | V | Low to high transition |
| $V_{UVL}$ | UV low threshold | # | 1.06 | 1.12 | 1.18 | V | High to low transition |
| $V_{UVHY}$ | UV hysteresis | # | - | 100 | - | mV | --- |
| $I_{UV}$ | UV input current | - | - | - | 1.0 | nA | $V_{UV}$ = $V_{EE}$ + 1.9V |
| $V_{OVH}$ | OV high threshold | # | 1.16 | 1.22 | 1.28 | V | Low to high transition |
| $V_{OVL}$ | OV low threshold | # | 1.06 | 1.12 | 1.18 | V | High to low transition |
| $V_{OVHY}$ | OV hysteresis | # | - | 100 | - | mV | --- |
| $I_{OV}$ | OV input current | - | - | - | 1.0 | nA | $V_{UV}$ = $V_{EE}$ + 1.9V |

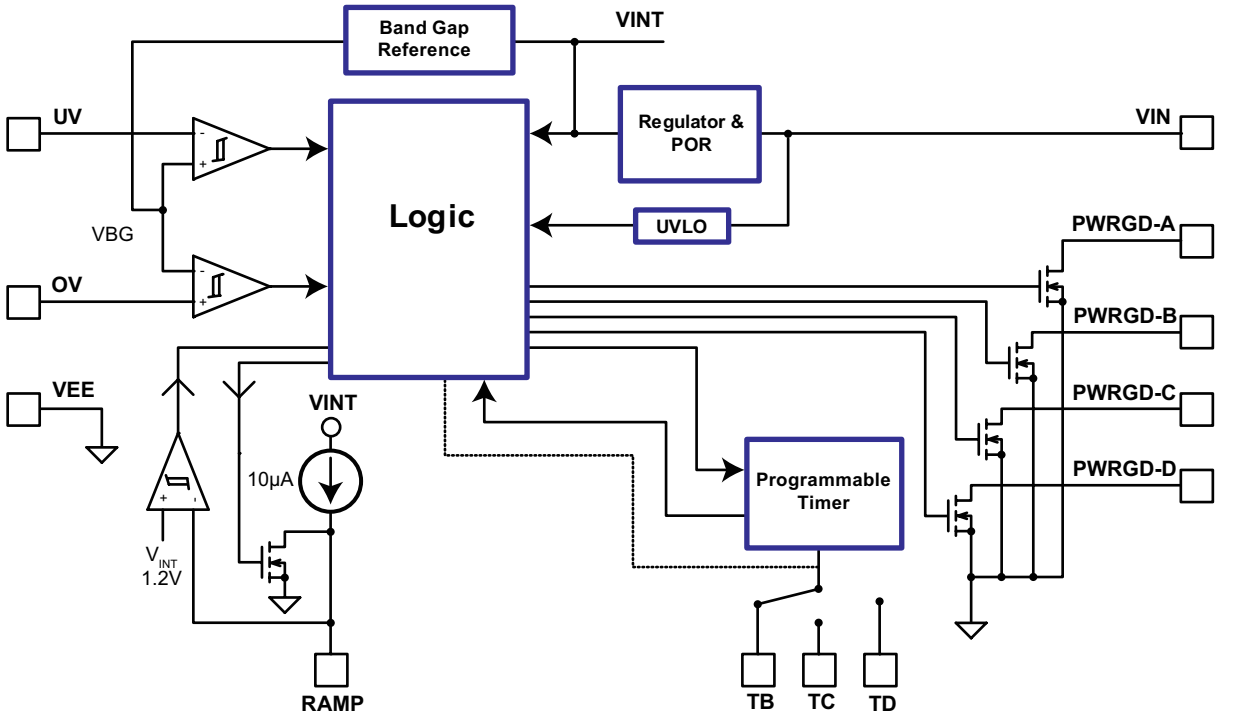
# *Specifications apply over 0°C ≤ $T_A$ ≤ 70°C*

## Electrical Characteristics *(cont.)* *(-10V ≤ $V_{IN}$ ≤ -90V, $T_A$ = 25°C unless otherwise specified)*

| Sym | Parameter | | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| **Power Good Timing** *(Test Conditions: $C_{RAMP}$ = 10nF, $V_{UV}$ = $V_{EE}$ + 1.9V, $V_{OV}$ = $V_{EE}$ + 0.5V)* | | | | | | | |
| $I_{RAMP}$ | Ramp pin output current | - | - | 10 | - | µA | --- |
| $t_{PWRGD-A}$ | Time from UV high to PWRGD-A | - | - | 8.8 | - | ms | $V_{EE}$ = -48V, $C_{RAMP}$ = 10nF, see typical application circuit |
| $t_{PWRGD-B}$ | Maximum time from PWRGD-A to PWRGD-B | - | 150 | 200* | 250 | ms | RTB = 120kΩ |
| $t_{PWRGD-B}$ | Minimum time from PWRGD-A to PWRGD-B | - | 3.0 | 5.0* | 8.0 | ms | RTD = 3.0kΩ |
| $t_{PWRGD-C}$ | Maximum time from PWRGD-B to PWRGD-C | - | 150 | 200* | 250 | ms | RTB = 120kΩ |
| $t_{PWRGD-C}$ | Minimum time from PWRGD-B to PWRGD-C | - | 3.0 | 5.0* | 8.0 | ms | RTD = 3.0kΩ |
| $t_{PWRGD-D}$ | Maximum time from PWRGD-C to PWRGD-D | - | 150 | 200* | 250 | ms | RTB = 120kΩ |
| $t_{PWRGD-D}$ | Minimum time from PWRGD-C to PWRGD-D | - | 3.0 | 5.0* | 8.0 | ms | RTD = 3.0kΩ |
| **Power Good Outputs** *(Test Conditions: $V_{UV}$ = $V_{EE}$ + 1.9V, $V_{OV}$ = $V_{EE}$ + 0.5V)* | | | | | | | |
| $V_{PWRGD-X(hi)}$ | Power good pin breakdown voltage | - | 90 | - | - | V | PWRGD-X = HI Z |
| $V_{PWRGD-X(lo)}$ | Power good pin output low voltage | - | - | 0.4 | 0.5 | V | $I_{PWRGD}$ = 1.0mA, PWRGD-X = LOW |
| $I_{PWRGD-X(lk)}$ | Maximum leakage current | - | - | <1.0 | 10 | µA | $V_{PWRGD}$ = 90V, PWRGD-X = HI Z |

* *Variations will track. For example if $t_{PWRGD-A}$ is 250ms, then so will be $t_{PWRGD-B/C/D}$. Contact factory for tighter tolerance version.*

## Functional Block Diagram



## Functional Description

The PS10 is designed to sequence up to 4 power supply modules, ICs or subsystems when the backplane voltage is within the programmed under voltage and over voltage limits. The power good open drain outputs are sequentially enabled starting from PWRGD-A to PWRGD-D. The time delay between power goods is programmable up to 200ms simply by changing the value(s) of RTB, RTC, and RTD. The initial time between satisfaction of the UV/OV supervisors & PWRGD-A can be programmed with $C_{RAMP}$.

### Description of Operation

During the initial power application, the Power Good pins are held low (rising with $V_{IN}$). Once the internal under voltage lock out has been satisfied, the circuit checks the input supply under voltage (UV) and over voltage (OV) sense circuits to ensure that the input voltage is within programmed limits. These limits are determined by the selected values for R1, R2, and R3, which form a voltage divider.

At the same time, a 10µA current source is enabled, charging the external capacitor connected to the ramp pin. The rise time of the RAMP pin is determined by the value of the capacitor ($10\mu A/C_{RAMP}$). When the ramp voltage reaches 8.8V, the PWRGD-A pin will change into an active state. PWRGD-B will change into an active state after a programmed time delay from PWRGD-A inactive to active transition. PWRGD-C will change into an active state after a programmed time delay from PWRGD-B inactive to active transition. PWRGD-D will change into an active state after a programmed time delay from PWRGD-C inactive to active transition.

The controller continuously monitors the UV and OV pins as long as the internal UVLO and POR circuits are satis-fied. At any time during the start up cycle or thereafter, crossing the UV low and OV high limits will cause an im-mediate discharge on Cramp and reset on the power good pins. When the input voltage returns to a value within the programmed UV and OV limits, a new start up sequence will initiate immediately.

### Programming the Under and Over Voltage Limits

The UV and OV pins are connected to comparators with nominal 1.17V thresholds and 100mV of hysteresis (1.17V ±50mV). They are used to detect under voltage and over voltage conditions at the input to the circuit. Whenever the OV pin rises above its high threshold (1.22V) or the UV pin falls below its low threshold (1.12V), the PWRGD outputs immediately deactivate.

Calculations can be based on either the desired input voltage operating limits or the input voltage shutdown limits. In the following equations the shutdown limits are assumed.

The undervoltage and overvoltage shut down thresholds can be programmed by means of the three resistor divider formed by R1, R2 and R3. Since the input currents on the UV and OV pins are negligible the resistor values may be calculated as follows:

$$UV_{OFF} = V_{UVL} = 1.12 = (V_{EEUV(off)}) \times (R2+R3)/(R1+R2+R3)$$

$$OV_{OFF} = V_{OVL} = 1.22 = (V_{EEOV(off)}) \times R3/(R1+R2+R3)$$

Where ($V_{EEUV(off)}$) and ($V_{EEOV(off)}$) relative to $V_{EE}$ are under and over voltage shut down threshold points.

If we select a divider current of 100µA at a nominal operating input voltage of 50V, then:

$$R1+R2+R3 = 50V/100\mu A = 500k\Omega$$

From the second equation, for an OV shut down threshold of 65V, the value of R3 may be calculated.

$$OV_{OFF} = 1.22 = (65xR3)/500k\Omega$$

$$R3 = (1.22x\ 500k\Omega)/65 = 9.38k\Omega$$

The closest 1% value is 9.31kΩ.

From the first equation, for a UV shut down threshold of 35V, the value of R2 can be calculated.

$$UV_{OFF} = 1.12 = 35 \times (R2+R3)/\ 500k\Omega$$

$$R2 = ((1.12 \times 500k\Omega)/35) - 9.76k\Omega = 6.69k\Omega$$

6.65kΩ is a standard 1% value

Then:

$$R1 = 500k\Omega - R2 - R3 = 484.04k\Omega.$$

487kΩ, is a standard 1% value.

From the calculated resistor values the OV and UV start up threshold voltages can be calculated as follows:

$$UV_{ON} = V_{UVH} = 1.22 = (V_{EEUV(on)}) \times (R2+R3)/(R1+R2+R3)$$

$$OV_{ON} = V_{OVL} = 1.12 = (V_{EEOV(on)}) \times R3/(R1+R2+R3)$$

Where ($V_{EEUV(on)}$) and ($V_{EEOV(on)}$) are under and over voltage start up threshold points relative to $V_{EE}$.

Then:

$(V_{EEUV(on)}) = 1.22 \times (R1+R2+R3)/(R2+R3)$

$(V_{EEUV(on)}) = 1.22 \times (487k+6.65k+9.31k)/(6.65k+9.31k)$

$= 38.45V$

And:

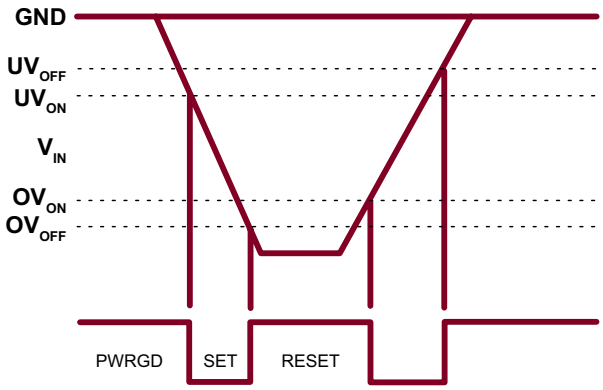
$(V_{EEOV(on)}) = 1.12 \times (R1+R2+R3)/R3$

$(V_{EEOV(on)}) = 1.12 \times (487k\Omega +6.65k\Omega +9.31k\Omega)/9.31k\Omega$

$= 60.51V$

Therefore, the circuit will start when the input supply voltage is in the range of 38.45V to 60.51V.

## Undervoltage/Overvoltage Protection




$t_{PWRGD-A}$ is the time delay from $V_{EEUV(on)}$ to PWRGD-A going active. It can be approximated by:

$t_{PWRGD-A} = C_{RAMP} \times (V_{INT}-1.17)/I_{RAMP}$

where:

$C_{RAMP}$ = capacitor connected from RAMP pin to VEE pin
$V_{INT}$ = internal regulated power supply voltage (10V typ.)
$I_{RAMP}$ = 10µA charge current

## PWRGD Flags Delay Programming

When the ramp voltage hits $V_{INT}$ - 1.17V, PWRGD-A becomes active indicating that the input supply voltage is within the programmed limits. PWRGD-B goes active after a programmed time delay after PWRGD-A went active. PWRGD-C goes active after a programmed time delay after PWRGD-B went active. PWRGD-D goes active after a programmed time delay after PWRGD-C went active.

The resistors connected from TB, TC, and TD to VEE pin determines the delay times between the PWRGD flags.

The value of the resistors determines the capacitor charging and discharging current of a triangular wave oscillator. The oscillator output is fed into an 8-bit counter to generate the desired time delay.

The respective time delay is defined by the following equation:

$t_{TX} = (255 \times 2 \times C_{OSC} \times V_{PP})/I_{CD}$

and

$I_{CD} = V_{BG} / (4 \times R_{TX})$

Where:

$t_{TX}$ = Time delay between respective PWRGD flags
$C_{OSC}$ = 120pF (internal oscillator capacitor)
$V_{PP}$ = 8.2V (peak-to-peak voltage swing of oscillator)
$I_{CD}$ = Charge and discharge current of oscillator
$V_{BG}$ = 1.17V (internal band gap reference)
$R_{TX}$ = Programming resistor at TB, TC, or TD

Combining the two equations and solving for $R_{TX}$ yields:

$R_{TX} = (V_{BG} \times t_{TX}) / (2040 \times C_{OSC} \times V_{PP})$

$= 0.585 \times 106 \times t_{TX}$

For a time delay of 200ms

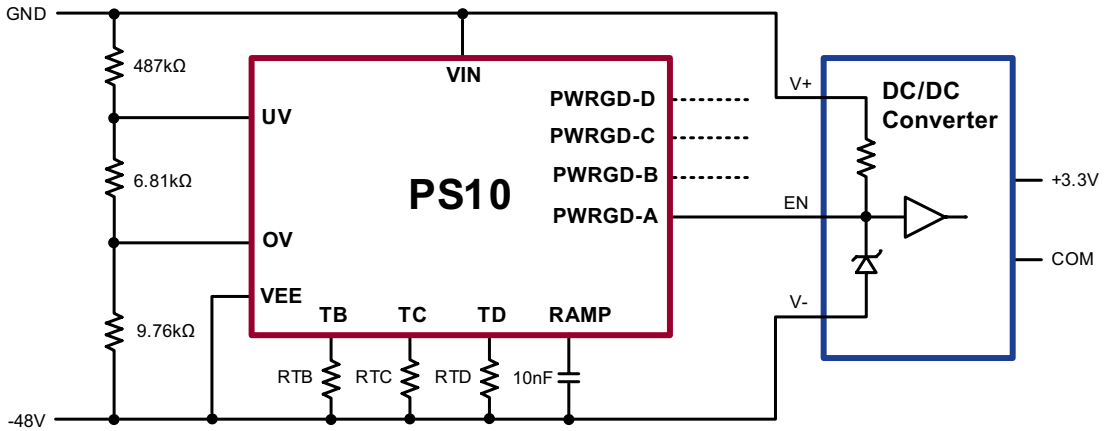
$R_{TX} = 0.585 \times 106 \times 0.2 = 117k\Omega$

For a time delay of 5ms

$R_{TX} = 0.585 \times 106 \times 0.005 = 2.925k\Omega$

## PWRGD Output Configuration

The PS10 open drain power good outputs can be connected directly to the Enable pins of the DC/DC converter. The internal pull-up and clamp of the DC/DC converter sets the logic High Enable/Disable voltage.

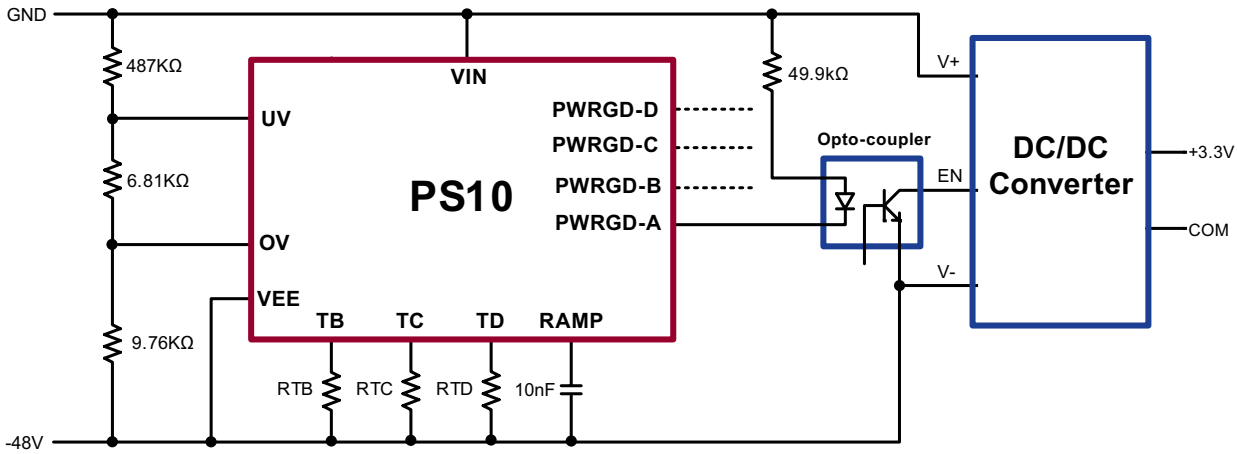



***Notes:***

1. *Under Voltage Shutdown (UV) set to 37V.*
2. *Over Voltage Shutdown (OV) to 57.8V.*
3. *Other power good outputs will have the same configuration as PWGRGD-A for Active High Enabled Converters.*

## Opto-isolated Enable

Some applications require opto-isolator interface to the Enable pin of the DC/DC converter.

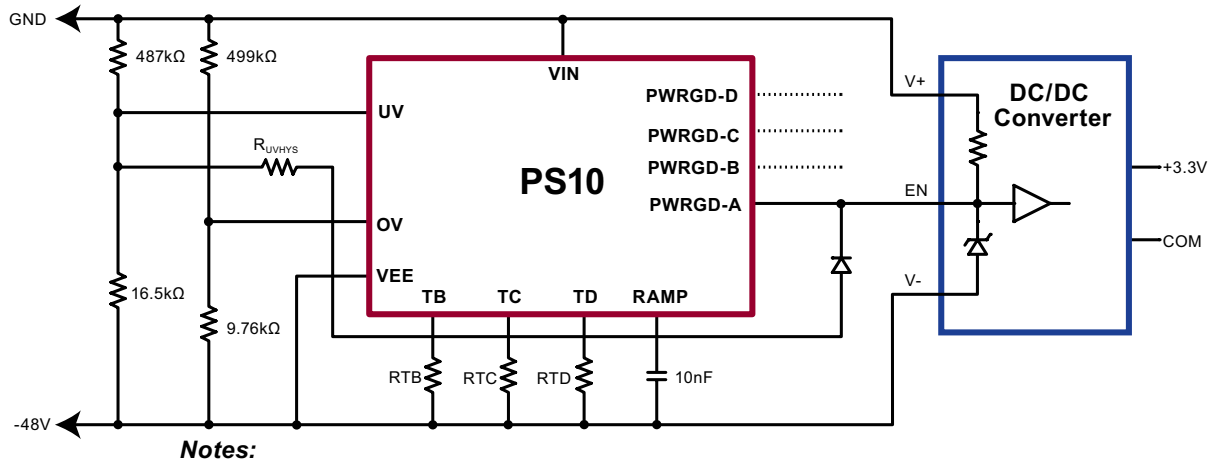



***Notes:***

1. *Under Voltage Shutdown (UV) set to 37V.*
2. *Over Voltage Shutdown (OV) to 57.8V.*
3. *Other power good outputs will have the same configuration as PWGRGD-A for Active High Enabled Converters.*

## Increasing the Under and Over Voltage Hysteresis

If the internal UV hysteresis is insufficient for a particular system application, then it may be increased by using separate resis-tor dividers for UV and OV and providing a resistor feedback from UV pin to the PWRGD pin.




***Notes:***

1. *Other power good outputs will have the same configuration as: PWGRGD-A for Active High Enabled Converters.*
2. *Over voltage shut down set to 63.6V*

$R_{UVHYS}$ *can be calculated based on higher UV On voltage (say 42V):*

$R_{UVHYS} = (V_{UVON} - V_{DIODE} - V_{PWRGDLOW})/((V_{IN} - V_{UVON})/487k\Omega - V_{UVON}/16.5k\Omega)$

$= (1.22\text{-}0.65\text{-}0.4)/((42\text{-}1.22)/487k\Omega - 1.22/16.5k\Omega)$

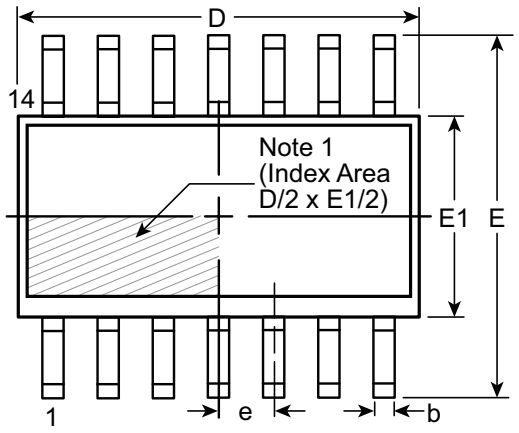
$= 17.35k\Omega$

## Pin Description

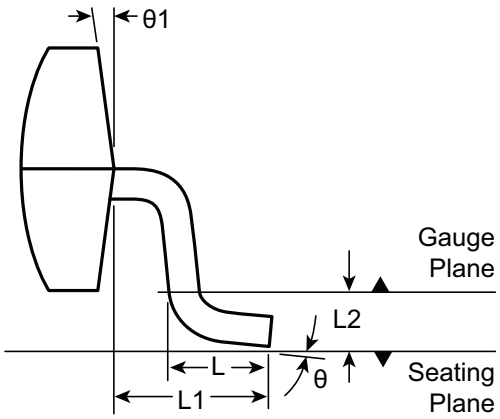
| Pin | Function | Description | |
|---|---|---|---|
| 1 | PWRGD-D | This open drain Power Good Output Pin is held inactive on initial power application and goes active a programmed time delay after PWRGD-C goes active. | To function as an indicator, a pullup resistor must be connected from this pin to a voltage rail no more than 90V from VEE. |
| 2 | PWRGD-C | This open drain Power Good Output Pin is held inactive on initial power application and goes active a programmed time delay after PWRGD-B goes active. | |
| 3 | PWRGD-B | This open drain Power Good Output Pin is held inactive on initial power application and goes active a programmed time delay after PWRGD-A goes active. | |
| 4 | PWRGD-A | This open drain Power Good Output Pin is held inactive on initial power application and goes active one POR delay after the UV pin goes above its High threshold (provided VIN stays within the UV/OV window during this period). | |
| 5 | OV | This Over Voltage (OV) sense pin, when raised above its high threshold will immediately cause the Power Good Outputs to be pulled low. These outputs will remain low until the voltage on this pin falls below the low threshold limit, initiating a new start-up cycle. | |
| 6 | UV | This Under Voltage (UV) sense pin, when lowered below its low threshold will immediately cause the Power Good Outputs to be pulled low. These outputs will remain low until the voltage on this pin rises above the low threshold limit, initiating a new start-up cycle. | |
| 7 | VEE | This pin is the negative terminal of the power supply input to the circuit. | |
| 8 | NC | No Connect. This pin can be grounded or left floating. | |
| 9 | NC | | |
| 10 | RAMP | This pin provides a current output so that a timing ramp is generated when a capacitor is connected. This timing Ramp is used to program POR and the time from satisfaction of the UV/OV supervisors to PWRGD-A. | |
| 11 | TB | The resistor connected from this pin to VEE pin sets the time delay from PWRGD-A going active to PWRGD-B going active. | |
| 12 | TC | The resistor connected from this pin to VEE pin sets the time delay from PWRGD-B going active to PWRGD-C going active. | |
| 13 | TD | The resistor connected from this pin to VEE pin sets the time delay from PWRGD-C going active to PWRGD-D going active. | |
| 14 | VIN | This pin is the positive terminal of the power supply input to the circuit and can withstand 90V with respect to VEE. | |

# 14-Lead SOIC (Narrow Body) Package Outline (NG)

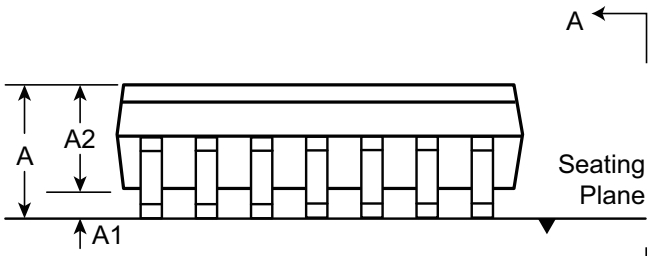
***8.65x3.90mm body, 1.75mm height (max), 1.27mm pitch***



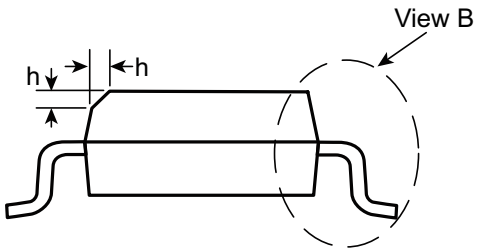

**Top View**




**View B**




**Side View**




**View A-A**

***Note:***

1. *This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

| Symbol | | A | A1 | A2 | b | D | E | E1 | e | h | L | L1 | L2 | θ | θ1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (mm) | MIN | 1.35* | 0.10 | 1.25 | 0.31 | 8.55* | 5.80* | 3.80* | 1.27 BSC | 0.25 | 0.40 | 1.04 REF | 0.25 BSC | 0° | 5° |
| | NOM | - | - | - | - | 8.65 | 6.00 | 3.90 | | - | - | | | - | - |
| | MAX | 1.75 | 0.25 | 1.65* | 0.51 | 8.75* | 6.20* | 4.00* | | 0.50 | 1.27 | | | 8° | 15° |

*JEDEC Registration MS-012, Variation AB, Issue E, Sept. 2005.*
** This dimension is not specified in the JEDEC drawing.*
***Drawings are not to scale.***
***Supertex Doc. #:** DSPD-14SOICNG, Version F041309.*

*(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)*



**Supertex inc.**
1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
***www.supertex.com***