Chipsmall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

<Dual-In-Line Package Intelligent Power Module>

Super mini DIPIPM Ver.5 Series APPLICATION NOTE
PS219Bx -S/-ST/-AS/-AST/-CS/CST

Table of contents

CHAPTER 1 INTRODUCTION

1.1 Features of Super mini DIPIPM Ver.5

Super Mini DIPIPM Ver.5 (hereinafter called DIP Ver.5) is an ultra-small compact intelligent power module with transfer mold package favorable for larger mass production. Power chips, drive and protection circuits are integrated in the module, which make it easy for AC100-240V class low power motor inverter control. Current Super mini DIPIPM Ver.4 series are most suitable for inverterized white goods because of our unique high efficiency power chips CSTBT, insulated sheet structure with very low thermal resistance and ultra small package. While the DIP Ver.5 keeps these features of Ver.4, it makes further progress. Main features of DIP Ver.5 are as below.

- *Newly developed 6th generation CSTBT are integrated for improving efficiency.*
- *Incorporating bootstrap diode with current limiting resistor for P-side gate driving supply*
- *Selectable new function for outputting package(control IC) temperature by analog signal*
- *Easy to replace from current Ver.4 due to high pin compatibility*

About detailed differences, please refer Section 1.5. Fig.1-1-1 and Fig.1-1-2 show the outline and internal cross-section structure respectively.
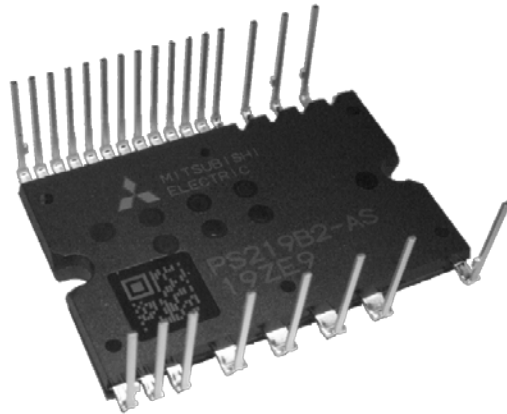
Fig.1-1-1 Package photograph
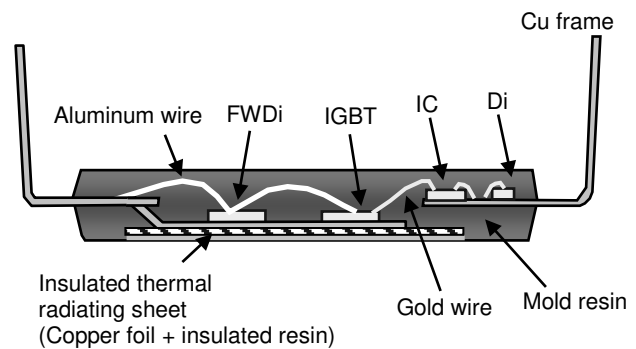
Fig.1-1-2 Internal cross-section structure

1.2 Functions

DIP Ver.5 has following functions and inner block diagram is described in Fig.1-2-1.

- For P-side IGBTs:
    - Drive circuit;
    - High voltage level shift circuit;
    - Control supply under voltage (UV) lockout circuit (without fault signal output).
    - Built-in bootstrap diode (BSD) with current limiting resistor
- For N-side IGBTs:
    - Drive circuit;
    - Short circuit (SC) protection circuit (by inserting external shunt resistor into main current path)
    - Control supply under voltage (UV) lockout circuit (with fault signal output)
    - Over temperature (OT) protection by monitoring LVIC temperature.（-T series only）
    - Outputting LVIC temperature by analog signal (Need to select from this function or OT)
- Fault Signal Output
    - Corresponding to N-side IGBT SC, N-side UV and OT protection.
- IGBT Drive Supply
    - Single DC15V power supply (in the case of using bootstrap method)
- Control Input Interface
    - Schmitt-triggered 3V,5V input compatible, high active logic.
- UL recognized : UL1557　File E323585

Fig.1-2-1 Inner block diagram

1.3 Target Applications

Motor drives for household electric appliances, such as air conditioners, washing machines, refrigerators
Low power industrial motor drive except automotive applications

1.4 Product Line-up

Table 1-4-1 DIP Ver.5 Line-up *with temperature output function*

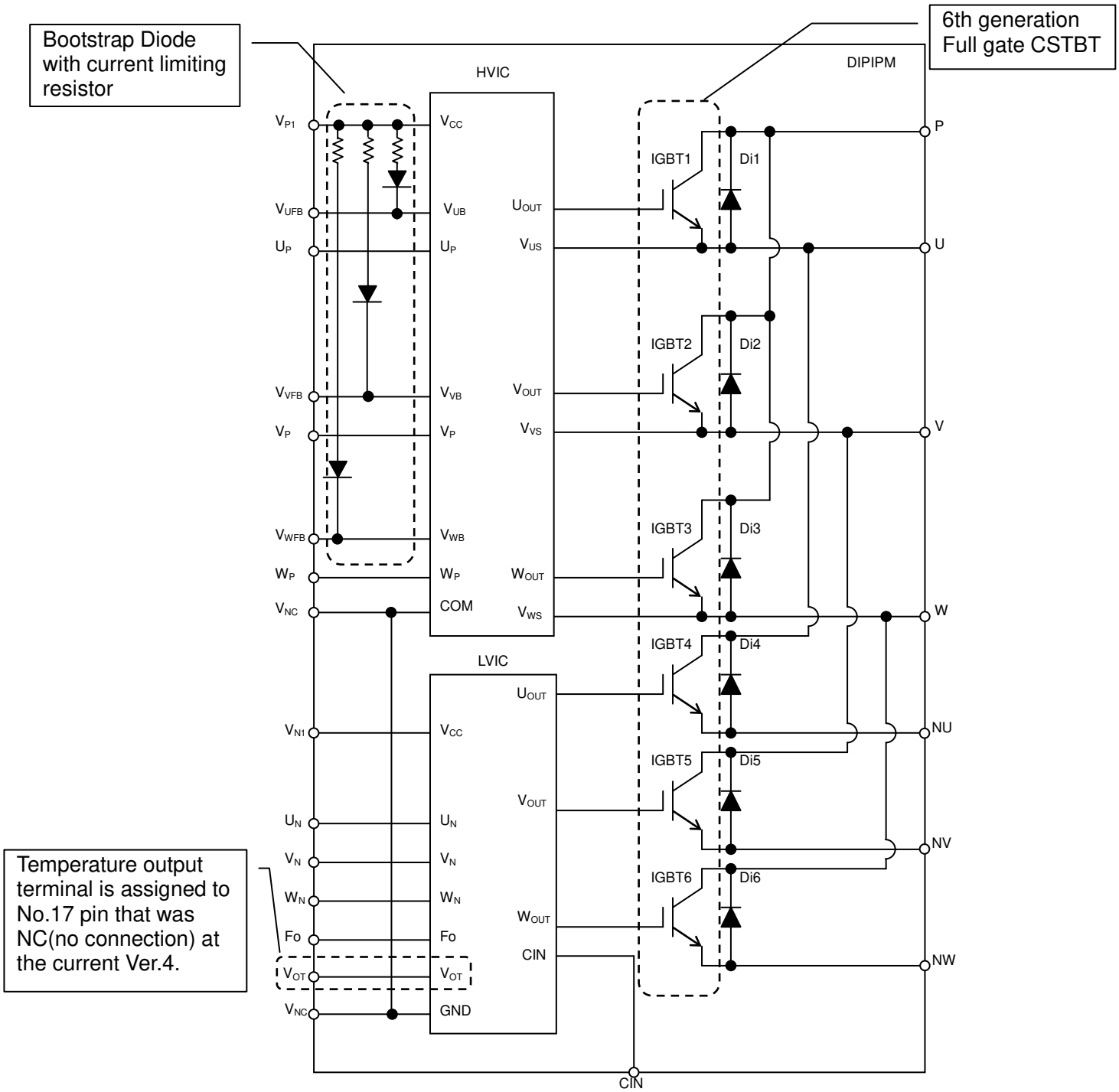| Type Name [(Note 1)]	IGBT Rating	Motor Rating [(Note 2)]	Isolation Voltage
PS219B2-S/-AS/-CS	5A/600V	0.4kW/220V$_{AC}$	V_{iso} = 1500Vrms (Sine 60Hz, 1min All shorted pins-heat sink)
PS219B3-S/-AS/-CS	10A/600V	0.75kW/220V$_{AC}$	
PS219B4-S/-AS/-CS	15A/600V	0.75kW/220V$_{AC}$	

Table 1-4-2 DIP Ver.5 Line-up *with over temperature protection function*

Type Name [(Note 1)]	IGBT Rating	Motor Rating [(Note 2)]	Isolation Voltage
PS219B2-ST/-AST/-CST	5A/600V	0.4kW/220V$_{AC}$	V_{iso} = 1500Vrms (Sine 60Hz, 1min All shorted pins-heat sink)
PS219B3-ST/-AST/-CST	10A/600V	0.75kW/220V$_{AC}$	
PS219B4-ST/-AST/-CST	15A/600V	0.75kW/220V$_{AC}$	

Note 1: Suffix 'A' indicates long pin type, 'C' indicates zigzag pin type, 'S' indicates N-side open emitter type and
'T' indicates built-in over temperature protect function type. Please refer to chapter 2 for details.
When selecting terminal shape for Super Mini DIPIPM series, please contact Mitsubishi Electric Corporation or authorized Mitsubishi Semiconductor product distributors.

Note 2: The motor ratings are simulation results under following conditions: V_{AC}=220V, V_D=V_{DB}=15V, Tc=100°C, Tj=125°C, f_{PWM}=5kHz, P.F=0.8, motor efficiency=0.75, current ripple ratio=1.05, motor over load 150% 1min.

1.5 The Differences between Previous Series and This Series (PS219B*)

DIP Ver.5 has some differences against current DIP Ver.4 (PS2196* and PS219A*)
Main differences are described in Table 1-5-1 and Table 1-5-2.

Table 1-5-1 Differences of functions and outlines

Items	PS2196* Ver.4	PS219A* Ver.4 with BSD	PS219B* Ver.5	Ref.
Built-in bootstrap diodes	-	Built-in [1]	Built-in [1] with current limiting resistor	Section 4.2
Temperature protection	OT (-T)	OT (-T)	OT (-T) or Temperature output [2]	Section 2.2.4
Dummy terminal (Compare with PS2196*)[3]	-	Add one terminal (No. 1-B pin)	Add one terminal (No. 1-B pin)	Section 2.3
N-side IGBT emitter terminal	Common / Open	Common / Open	Open [4]	
Terminal shapes [4]	**Total 5 types** short, long, one side zigzag, both sides zigzag, short with 3 shunts	**Total 5 types** 5 types of PS2196* and long or one side zigzag with 3shunts	**Total 3 types** All types are 3 shunts short, long, one side zigzag	Section 2.3

(1) Built-in bootstrap diode (BSD) of DIP Ver.5 PS219B* incorporates current limiting resistor (typ. 100Ω). So there isn't any limitation about bootstrap capacitance like current PS219A* has (22μF or less in the case of one long pulse initial charging).

(2) Temperature protection function of DIP Ver.5 is selectable from two functions. (They have different model numbers as above.) One is conventional over temperature protection (OT), and the other is LVIC temperature output function (V_{OT}). OT function shutdowns all N-side IGBTs automatically when LVIC temperature exceeds specified value (typ.120 °C). But V_{OT} function cannot shutdown by itself in that case. So it is necessary for system controller to monitor this V_{OT} output and shutdown when the temperature reaches the protection level.

(3) Because of incorporating bootstrap diodes, a part of package was changed. (Just one dummy terminal was added) But its package size, pin assignment and pin number weren't changed, so the same PCB can be used with small modification when replacing from current Super min DIP Ver.4. (External bootstrap diodes and current limit resistors should be removed in the case of replacing from PS2196*. And also if N-side common emitter type was used in former PCB, it is necessary to change wiring from common emitter to open emitter wiring because of DIP Ver.5 has open emitter type only.)

(4) N-side IGBT emitter terminal of DIP Ver.5 is open emitter type only and terminal shapes are short (-S), long (-A) and one (control) side zigzag (-C) types.

Table 1-5-2 Differences of specifications and recommended operating conditions

Items	Symbol	PS2196* Ver.4	PS219A* Ver.4 with BSD	PS219B* Ver.5
Circuit current for P-side driving	I_{DB}	Max. 0.55mA	Max. 0.10mA	Max. 0.10mA
Trip voltage for P-side control supply under voltage protection	UV_{DBt}	Min.10.0V	Min. 7.0V	Min. 7.0V
Trip voltage for P-side control supply under voltage protection	UV_{DBr}	Min.10.5V	Min. 7.0V	Min. 7.0V
Bootstrap Di forward voltage	V_F	-	Typ. 2.8V @100mA	Typ. 1.7V @10mA
Arm-shoot-through blocking time for 5~15A rating products	t_{dead}	Min. 1.5µs	Min. 1.0µs	Min. 1.0µs
Allowable minimum input pulse width	PWIN(on)	Min. 0.5µs	Min. 0.5µs	Min. 0.7µs
	PWIN(off)	Min. 0.5µs	Min. 0.5µs	Min. 0.7µs

For more detail and the other characteristics, please refer the datasheet or application note for each product.

CHAPTER 2 SPECIFICATIONS AND CHARACTERISTICS

2.1 Super Mini DIPIPM Ver.5 Specifications

DIP Ver.5 specifications are described below by using PS219B4 (15A/600V) as an example. Please refer to respective datasheet for the detailed description of other types.

2.1.1 Maximum Ratings
The maximum ratings of PS219B4 are shown in Table 2-1-1.

Table 2-1-1 Maximum Ratings

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit	
V_{CC}	Supply voltage	Applied between P-NU,NV,NW	450	V	(1)
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-NU,NV,NW	500	V	(2)
V_{CES}	Collector-emitter voltage		600	V	(3)
$\pm I_C$	Each IGBT collector current	T_C= 25°C	15	A	(4)
$\pm I_{CP}$	Each IGBT collector current (peak)	T_C= 25°C, less than 1ms	30	A	
P_C	Collector dissipation	T_C= 25°C, per 1 chip	33.3	W	
T_j	Junction temperature	(Note)	-20~+150	°C	(5)

Note: The maximum junction temperature rating of built-in power chips is 150°C(@Tc≤100°C).However, to ensure safe operation of DIPIPM, the average junction temperature should be limited to Tj(Ave)≤125°C (@Tc≤100°C).

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	20	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-U, V_{VFB}-V, V_{WFB}-W	20	V
V_{IN}	Input voltage	Applied between U_P, V_P, W_P-V_{PC}, U_N, V_N, W_N-V_{NC}	-0.5~V_D+0.5	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	-0.5~V_D+0.5	V
I_{FO}	Fault output current	Sink current at F_O terminal	1	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	-0.5~V_D+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit	
$V_{CC(PROT)}$	Self protection supply voltage limit (Short circuit protection capability)	V_D = 13.5~16.5V, Inverter Part T_j = 125°C, non-repetitive, less than 2µs	400	V	(6)
T_C	Module case operation temperature	Measurement point of Tc is provided in Fig.1	-20~+100	°C	
T_{stg}	Storage temperature		-40~+125	°C	
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	1500	V_{rms}	(7)

Tc measurement position

Control terminals

DIPIPM

11.6mm

3mm

IGBT chip position

FWD chip position

Power terminals

Tc point

Heat sink side

(8)
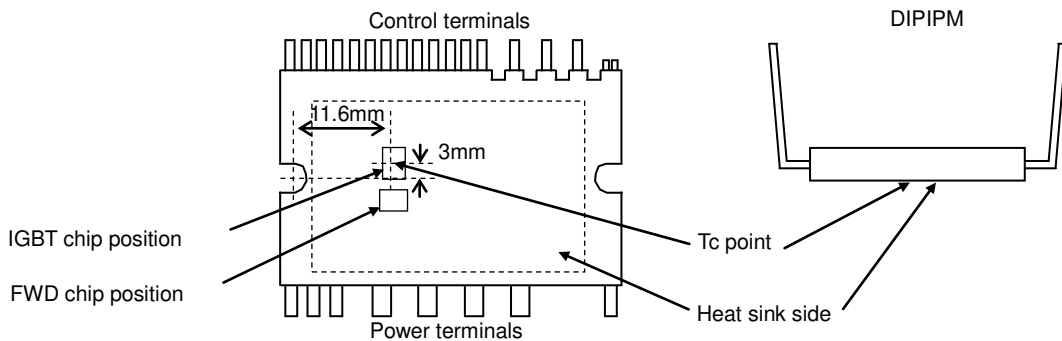
(1) Vcc   The maximum voltage can be biased between P-N. A voltage suppressing circuit such as a brake circuit is necessary if P-N voltage exceeds this value.

(2) Vcc(surge)   The maximum P-N surge voltage in switching state. If P-N voltage exceeds this voltage, a snubber circuit is necessary to absorb the surge under this voltage.

(3) V_{CES} The maximum sustained collector-emitter voltage of built-in IGBT and FWDi.

(4) +/-I_C The allowable current flowing into collect electrode (@Tc=25°C).Pulse width and period are limited due to junction temperature Tj.

(5) Tj   The maximum junction temperature rating is 150°C. But for safe operation, it is recommended to limit the average junction temperature up to 125°C. Repetitive temperature variation ΔTj affects the life time of power cycle, so refer life time curves for safety design.

(6) Vcc(prot)   The maximum supply voltage for turning off IGBT safely in the case of an SC or OC fault. The power chip might be damaged if supply voltage exceeds this specification.

(7) Isolation voltage   Isolation voltage of Super mini DIPIPM is the voltage between all shorted pins and copper surface of DIPIPM. The maximum rating of isolation voltage of Super mini DIPIPM is 1500Vrms. But if such as convex shape heat radiation fin will be used for enlarging clearance between outer terminals and heat radiation fin (2.5mm or more is recommended), it is able to correspond isolation voltage 2500Vrms. Super mini DIPIPM is recognized by UL at the condition 2500Vrms with convex shape heat radiation fin
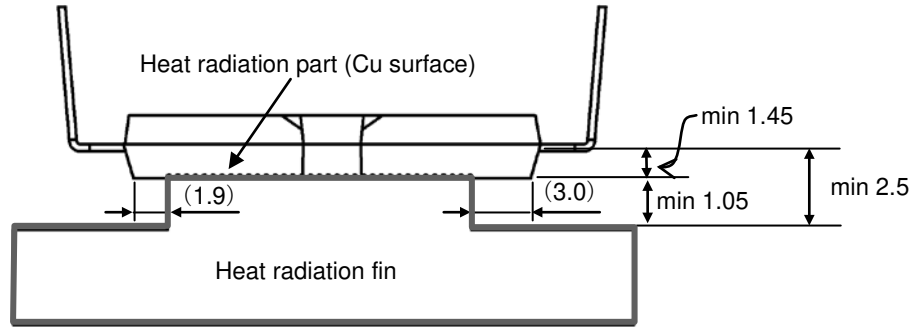

Fig.2-1-1 In the case of using convex heat sink (unit: mm)

(8) Tc position   Tc (case temperature) is defined to be the temperature just beneath the specified power chip. Please mount a thermocouple on the heat sink surface at the defined position to get accurate temperature information. Due to the control schemes such different control between P and N-side, there is the possibility that highest Tc point is different from above point. In such cases, it is necessary to change the measuring point to that under the highest power chip.

[Power chip position]
Fig.2-1-2 indicates the position of the each power chips. (This figure is the view from laser marked side.)
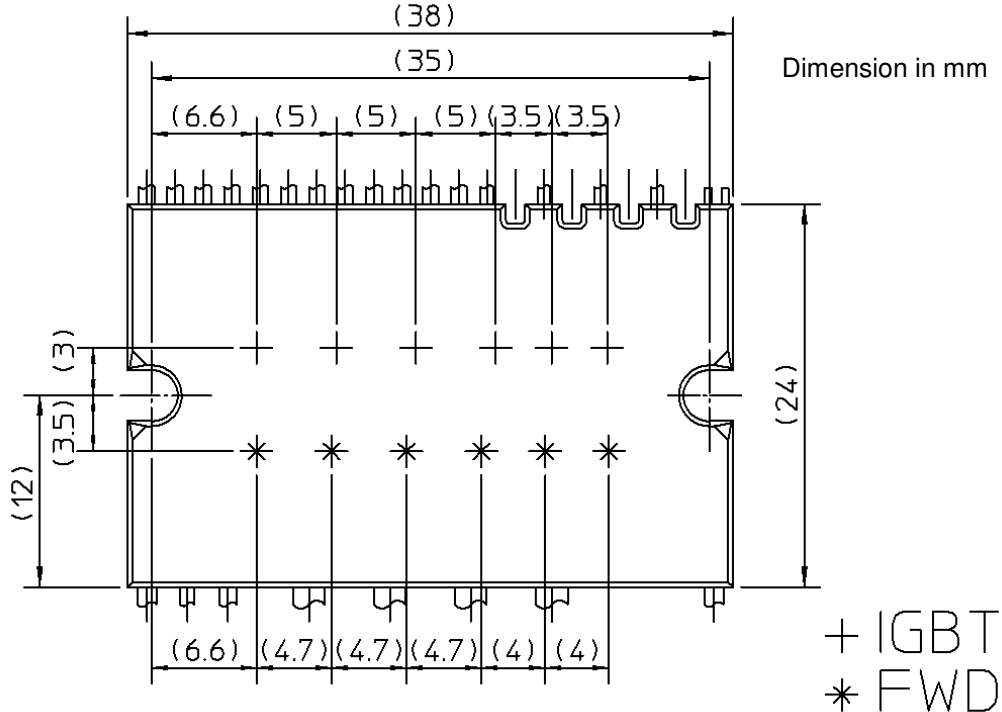

Fig.2-1-2 Power chip position

2.1.2 Thermal Resistance
Table 2-1-2 shows the thermal resistance of PS219B4.

Table 2-1-2 Thermal resistance of PS219B4

THERMAL RESISTANCE

| Symbol | Parameter | Condition | Limits | | | Unit |
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal	Inverter IGBT part (per 1/6 module)	-	-	3.0	K/W
$R_{th(j-c)F}$	resistance (Note)	Inverter FWDi part (per 1/6 module)	-	-	3.9	K/W

Note : Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100μm~+200μm on the contacting surface of DIPIPM and heat sink. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.3K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m•k).

The above data shows the thermal resistance between chip junction and case at steady state. The thermal resistance goes into saturation in about 10 seconds. The unsaturated thermal resistance is called as transient thermal impedance which is shown in Fig.2-1-3. Zth(j-c)* is the normalized value of the transient thermal impedance. (Zth(j-c)*= Zth(j-c) / Rth(j-c)max)
For example, the IGBT transient thermal impedance of PS219B4 in 0.3s is 3.0×0.8=2.4K/W.
The transient thermal impedance isn't used for constantly current, but for short period current (ms order).
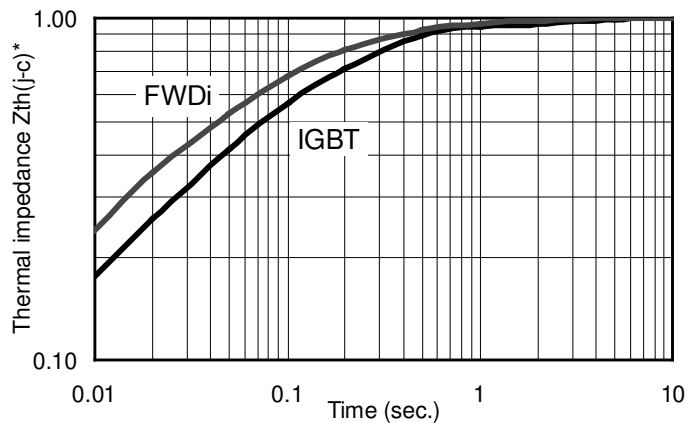(E.g. In the cases at motor starting, at motor lock···)

Fig.2-1-3 Typical transient thermal impedance

2.1.3 Electric Characteristics and Recommended Conditions

Table 2-1-3 shows the typical static characteristics and switching characteristics of PS219B4.

Table 2-1-3 Static characteristics and switching characteristics of PS219B4

INVERTER PART (T_j = 25°C, unless otherwise noted)

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D=V_{DB}$ = 15V, V_{IN}= 5V, I_C= 15A	T_j= 25°C	-	1.50	2.00	V
			T_j= 125°C	-	1.60	2.10	
V_{EC}	FWDi forward voltage	V_{IN}= 0V, $-I_C$= 15A		-	1.70	2.20	V
t_{on}	Switching times	V_{CC}= 300V, V_D= V_{DB}= 15V I_C= 15A, T_j= 125°C, V_{IN}= 0↔5V Inductive Load (upper-lower arm)		0.85	1.45	2.05	µs
$t_{C(on)}$				-	0.45	0.70	µs
t_{off}				-	1.50	2.10	µs
$t_{C(off)}$				-	0.35	0.60	µs
t_{rr}				-	0.30	-	µs
I_{CES}	Collector-emitter cut-off current	$V_{CE}=V_{CES}$	T_j= 25°C	-	-	1	mA
			T_j= 125°C	-	-	10	

Switching time definition and performance test method are shown in Fig.2-1-4 and 2-1-5.
Switching characteristics are measured by half bridge circuit with inductance load.
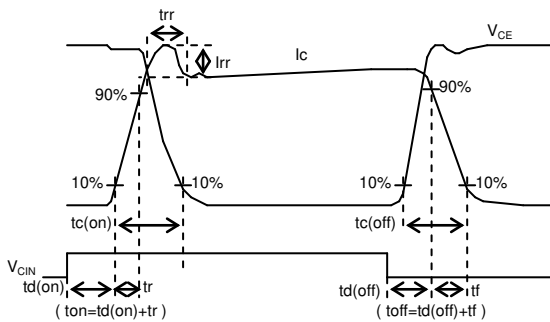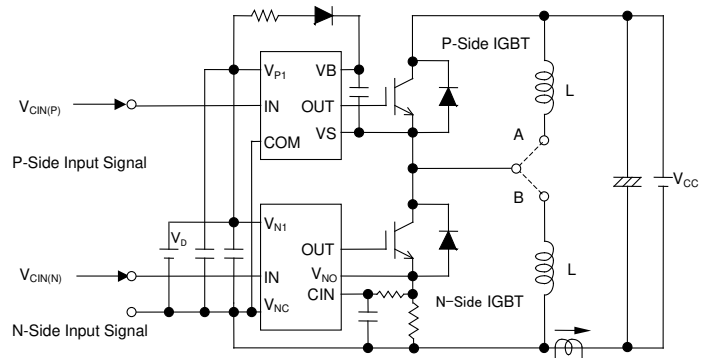

Fig.2-1-4 Switching time definition

Fig.2-1-5 Evaluation circuit (inductive load)
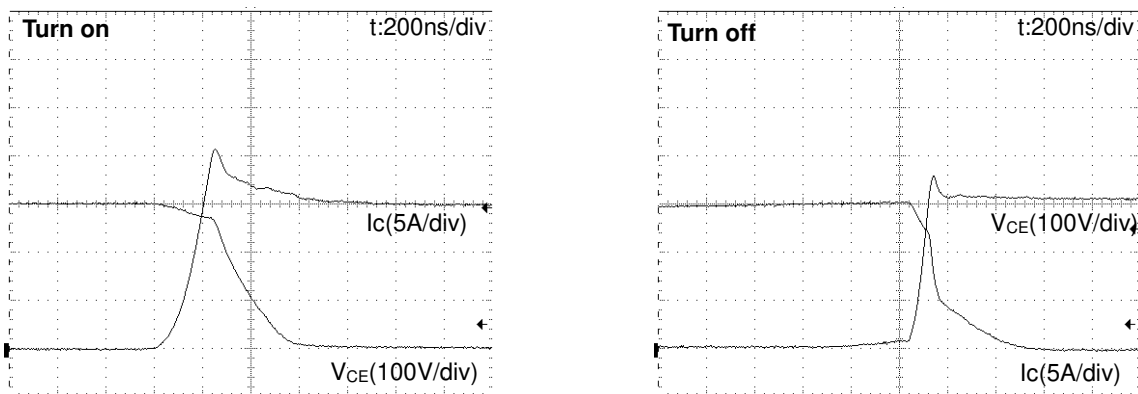Short A for N-side IGBT, and short B for P-side IGBT evaluation

Fig.2-1-6 Typical switching waveform (PS219B4)
Conditions: V_{CC}=300V, V_D=V_{DB}=15V, Tj=125°C, Ic=15A, Inductive load half-bridge circuit

Table 2-1-4 shows the typical control part characteristics of PS219B4.

Table 2-1-4 Control (Protection) characteristics of PS219B4

CONTROL (PROTECTION) PART (T_j = 25°C, unless otherwise noted)

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
I_D	Circuit current	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	V_D=15V, V_{IN}=0V	-	-	2.80	mA
			V_D=15V, V_{IN}=5V	-	-	2.80	
I_{DB}		Each part of V_{UFB}-U, V_{VFB}-V, V_{WFB}-W	V_D=V_{DB}=15V, V_{IN}=0V	-	-	0.10	
			V_D=V_{DB}=15V, V_{IN}=5V	-	-	0.10	
$V_{SC(ref)}$	Short circuit trip level	V_D = 15V (Note 1)		0.43	0.48	0.53	V
UV_{DBt}	P-side Control supply under-voltage protection(UV)	T_j ≤125°C	Trip level	7.0	10.0	12.0	V
UV_{DBr}			Reset level	7.0	10.0	12.0	V
UV_{Dt}	N-side Control supply under-voltage protection(UV)		Trip level	10.3	-	12.5	V
UV_{Dr}			Reset level	10.8	-	13.0	V
V_{OT}	Temperature output* (-S/-AS/-CS only)	Pull down R=5kΩ (Note 2)	LVIC Temperature=90°C	2.63	2.77	2.91	V
			LVIC Temperature=25°C	0.88	1.13	1.39	V
OT_t	Overt temperature protection* (OT, -ST/-AST/-CST only) (Note3)	V_D = 15V	Trip level	100	120	140	°C
OT_{rh}		Detect LVIC temperature	Hysteresis of trip-reset	-	10	-	°C
V_{FOH}	Fault output voltage	V_{SC} = 0V, F_O terminal pulled up to 5V by 10kΩ		4.9	-	-	V
V_{FOL}		V_{SC} = 1V, I_{FO} = 1mA		-	-	0.95	V
t_{FO}	Fault output pulse width	(Note 4)		20	-	-	µs
I_{IN}	Input current	V_{IN} = 5V		0.70	1.00	1.50	mA
$V_{th(on)}$	ON threshold voltage	Applied between U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}		-	2.10	2.60	V
$V_{th(off)}$	OFF threshold voltage			0.80	1.30	-	
$V_{th(hys)}$	ON/OFF threshold hysteresis voltage			0.35	0.65	-	
V_F	Bootstrap Di forward voltage	I_F=10mA including voltage drop by limiting resistor		1.1	1.7	2.3	V
R	Built-in limiting resistance	Included in bootstrap Di		80	100	120	Ω

Note 1 : SC protection works only for N-side IGBT. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.
  2 : DIPIPM don't shutdown IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIPIPM.
  3 : When the LVIC temperature exceeds OT trip temperature level(OT_t), OT protection works and Fo outputs. In that case if the heat sink dropped off or fixed loosely, don't reuse that DIPIPM. (There is a possibility that junction temperature of power chips exceeded maximum Tj(150°C).
  4 : Fault signal Fo outputs when SC, UV or OT protection works. Fo pulse width is different for each protection modes. At SC failure, Fo pulse width is a fixed width (=minimum 20µs), but at UV or OT failure, Fo outputs continuously until recovering from UV or OT state. (But minimum Fo pulse width is 20µs.)

*) It is necessary to select from temperature output function or over temperature protection about temperature protection.
Their part numbers are different. (e.g. PS219B4-S is the type with temperature output function and PS219B4-S<u>T</u> is the type with over temperature protection.)

Recommended operating conditions of PS219B4 are given in Table 2-1-5.

Although these conditions are the recommended but not the necessary ones, it is highly recommended to operate the modules within these conditions so as to ensure DIPIPM safe operation.

Table 2-1-5 Recommended operating conditions of PS219B4

RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	Applied between P-NU, NV, NW		0	300	400	V
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}		13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-U, V_{VFB}-V, V_{WFB}-W		13.0	15.0	18.5	V
ΔV_D, ΔV_{DB}	Control supply variation			-1	-	+1	V/µs
t_{dead}	Arm shoot-through blocking time	For each input signal		1.0	-	-	µs
f_{PWM}	PWM input frequency	$T_C \leq 100°C$, $T_j \leq 125°C$		-	-	20	kHz
I_O	Allowable r.m.s. current	$V_{CC} = 300V$, $V_D = 15V$, P.F = 0.8, Sinusoidal PWM $T_C \leq 100°C$, $T_j \leq 125°C$ (Note1)	f_{PWM}= 5kHz	-	-	8.0	Arms
			f_{PWM}= 15kHz	-	-	5.0	
PWIN(on)	Minimum input pulse width	(Note 2)		0.7	-	-	µs
PWIN(off)				0.7		-	
V_{NC}	V_{NC} variation	Between V_{NC}-NU, NV, NW (including surge)		-5.0	-	+5.0	V
T_j	Junction temperature			-20	-	+125	°C

Note 1: Allowable r.m.s. current depends on the actual application conditions.
    2: DIPIPM might not make response if the input signal pulse width is less than PWIN(on), PWIN(off).

<u>About Control supply variation</u>
If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet the following specifications:
$$dV/dt \leq +/-1V/µs, \quad Vripple \leq 2Vp-p$$

2.1.4 Mechanical Characteristics and Ratings

The mechanical characteristics and ratings are shown in Table 2-1-6.
Please refer to Section 2.4 for the detailed mounting instruction of DIP Ver.5.

Table 2-1-6　Mechanical characteristics and ratings of PS219B4

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw : M3 (Note 1)	Recommended 0.69N·m	0.59	0.69	0.78	N·m
Terminal pulling strength	Control terminal: Load 4.9N Power terminal: Load 9.8N	EIAJ-ED-4701	10	-	-	s
Terminal bending strength	Control terminal: Load 2.45N Power terminal: Load 4.9N 90deg. bend	EIAJ-ED-4701	2	-	-	times
Weight			-	8.5	-	g
Heat-sink flatness	(Note 2)		-50	-	100	µm

Note 1: Plain washers (ISO 7089~7094) are recommended.
Note 2: Measurement point of heat sink flatness
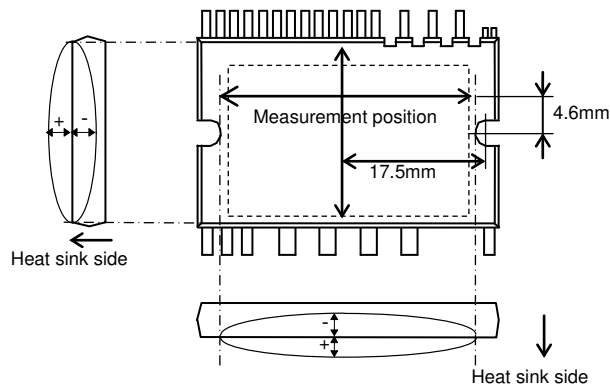
2.2 Protective Functions and Operating Sequence

DIP Ver.5 has Short circuit (SC), Under Voltage of control supply (UV), Over Temperature (OT) and temperature output (VOT) for protection function. The operating principle and sequence are described below.

2.2.1 Short Circuit Protection

1. General

DIP Ver.5 uses external shunt resistor for the current detection as shown in Fig.2-2-1. The internal protection circuit inside the IC captures the excessive large current by comparing the CIN voltage generated at the shunt resistor with the referenced SC trip voltage, and perform protection automatically. The threshold voltage trip level of the SC protection Vsc(ref) is typ. 0.48V.

In case of SC protection happens, all the gates of N-side three phase IGBTs will be interrupted together with a fault signal output. To prevent DIPIPM erroneous protection due to normal switching noise and/or recovery current, it is necessary to set an RC filter (time constant: 1.5μ ~ 2μs) to the CIN terminal input (Fig.2-2-1, 2-2-2). Also, please make the pattern wiring around the shunt resistor as short as possible.
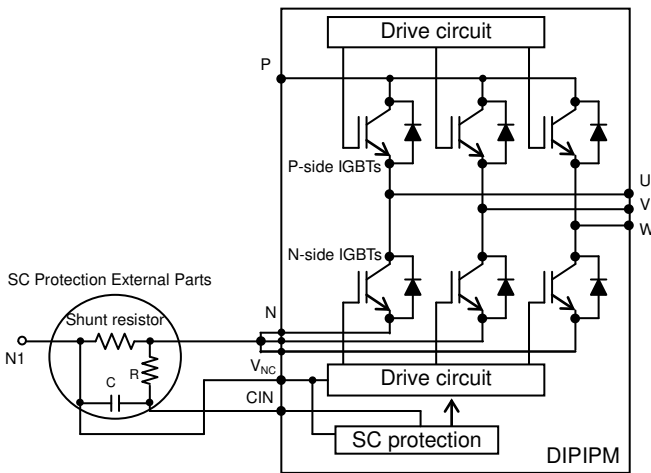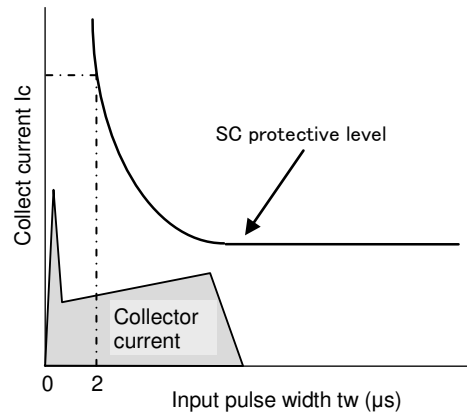

Fig.2-2-1 SC protecting circuit

Fig.2-2-2 Filter time constant setting

2. SC protection Sequence

SC protection (N-side only with the external shunt resistor and RC filter)
- a1. Normal operation: IGBT ON and carrying current.
- a2. Short circuit current detection (SC trigger).
  - (It is recommended to set RC time constant 1.5~2.0μs so that IGBT shut down within 2.0μs when SC.)
- a3. All N-side IGBTs' gate are hard interrupted.
- a4. All N-side IGBTs turn OFF.
- a5. Fo outputs for t_{Fo}=minimum 20μs.
- a6. Input = "L". IGBT OFF
- a7. Fo finishes output, but IGBTs don't turn on until inputting next ON signal (L→H).
  - (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
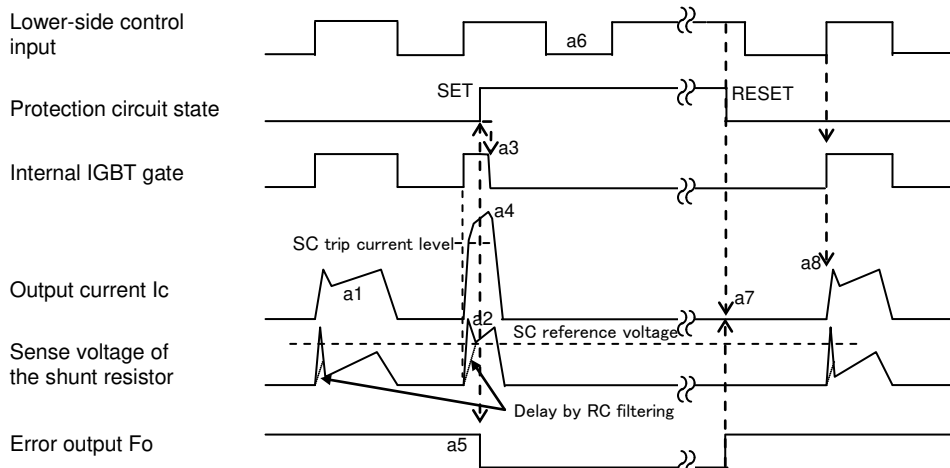- a8. Normal operation: IGBT ON and outputs current.

Fig.2-2-3 SC protection timing chart

3. Determination of Shunt Resistance

(1) Shunt resistance

The value of current sensing resistance is calculated by the following expression:
$$R_{Shunt} = V_{SC(ref)}/SC$$
where $V_{SC(ref)}$ is the referenced SC trip voltage.

The maximum SC trip level SC(max) should be set less than the IGBT minimum saturation current which is 1.7 times as large as the rated current. For example, the SC(max) of PS219B4 should be set to 15x1.7=25.5A. The parameters ($V_{SC(ref)}$, R_{Shunt}) dispersion should be considered when designing the SC trip level.

For example of PS219B4, there is +/-0.05V dispersion in the spec of $V_{SC(ref)}$ as shown in Table 2-2-1.

Table 2-2-1 Specification for $V_{SC(ref)}$ (unit: V)

Condition	Min	Typ	Max
at Tj=25°C, VD=15V	0.43	0.48	0.53

Then, the range of SC trip level can be calculated by the following expressions:
$$R_{Shunt(min)}=V_{SC(ref)\,max}/SC(max)$$
$$R_{Shunt(typ)}= R_{Shunt(min)}/0.95* \quad then \quad SC(typ) = V_{SC(ref)\,typ}/R_{Shunt(typ)}$$
$$R_{Shunt(max)}= R_{Shunt(typ)} \times 1.05* \quad then \quad SC(min)= V_{SC(ref)\,min}/R_{Shunt(max)}$$
*)This is the case that shunt resistance dispersion is within +/-5%.

So the SC trip level range is described as Table 2-2-2.

Table 2-2-2 Operative SC Range (R_{Shunt}=20.8mΩ (min), 21.9mΩ (typ), 23.0mΩ(max)

Condition	min.	typ.	Max.
at Tj=25°C	18.7A	21.9A	25.5A

(e.g. 20.8mΩ ($R_{shunt(min)}$)= 0.53V (=$V_{SC(max)}$) / 25.5A(=SC(max)))

There is the possibility that the actual SC protection level becomes less than the calculated value. This is considered due to the resonant signals caused mainly by parasitic inductance and parasitic capacity. It is recommended to make a confirmation of the resistance by prototype experiment.

(2) RC Filter Time Constant

It is necessary to set an RC filter in the SC sensing circuit in order to prevent malfunction of SC protection due to noise interference. The RC time constant is determined depending on the applying time of noise interference and the SCSOA of the DIPIPM.

When the voltage drop on the external shunt resistor exceeds the SC trip level, The time (t1) that the CIN terminal voltage rises to the referenced SC trip level can be calculated by the following expression:

$$V_{SC} = R_{shunt} \cdot I_c \cdot (1 - \varepsilon^{-\frac{t1}{\tau}})$$
$$t1 = -\tau \cdot \ln(1 - \frac{V_{SC}}{R_{shunt} \cdot I_c})$$

Vsc : the CIN terminal input voltage, Ic : the peak current, τ : the RC time constant

On the other hand, the typical time delay t2 (from Vsc voltage reaches Vsc(ref) to IGBT gate shutdown) of IC is shown in Table 2-2-3.

Table 2-2-3 Internal time delay of IC

Item	min	typ	max	Unit
IC transfer delay time	-	-	0.5	µs

Therefore, the total delay time from an SC level current happened to the IGBT gate shutdown becomes:
$$t_{TOTAL}=t1+t2$$

2.2.2 Control Supply UV Protection

The UV protection is designed to prevent unexpected operating behavior as described in Table 2-2-4.
Both P-side and N-side have UV protecting function. However, fault signal (Fo) output only corresponds to N-side UV protection. Fo output continuously during UV state.
In addition, there is a noise filter (typ. 10µs) integrated in the UV protection circuit to prevent instantaneous UV erroneous trip. Therefore, the control signals are still transferred in the initial 10µs after UV happened.

Table 2-2-4 DIPIPM operating behavior versus control supply voltage

Control supply voltage	Operating behavior
0-4.0V (P, N)	In this voltage range, built-in control IC may not work properly. Normal operating of each protection function (UV, Fo output etc.) is not also assured. Normally IGBT does not work. But external noise may cause DIPIPM malfunction (turns ON), so DC-link voltage need to start up after control supply starts-up.
4.0-UV_{Dt} (N), UV_{DBt} (P)	UV function becomes active and output Fo (N-side only). Even if control signals are applied, IGBT does not work
UV_{Dt} (N)-13.5V UV_{DBt} (P)-13.0V	IGBT can work. However, conducting loss and switching loss will increase, and result extra temperature rise at this state,.
13.5-16.5V (N) 13.0-18.5V (P)	Recommended conditions.
16.5-20.0V (N) 18.5-20.0V (P)	IGBT works. However, switching speed becomes fast and saturation current becomes large at this state, increasing SC broken risk.
20.0V- (P, N)	The control circuit will be destroyed.

Ripple Voltage Limitation of Control Supply

If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem happens, line ripple voltage should meet the following specifications:

$$dV/dt \leq +/-1V/\mu s, \ Vripple \leq 2Vp\text{-}p$$

[N-side UV Protection Sequence]
a1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but IGBT turns ON by next
    ON signal (L→H).(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
a2. Normal operation: IGBT ON and carrying current.
a3. V_D level dips to under voltage trip level. (UV_{Dt}).
a4. All N-side IGBTs turn OFF in spite of control input condition.
a5. Fo outputs for t_{Fo}=minimum 20μs, but output is extended during V_D keeps below UV_{Dr}.
a6. V_D level reaches UV_{Dr}.
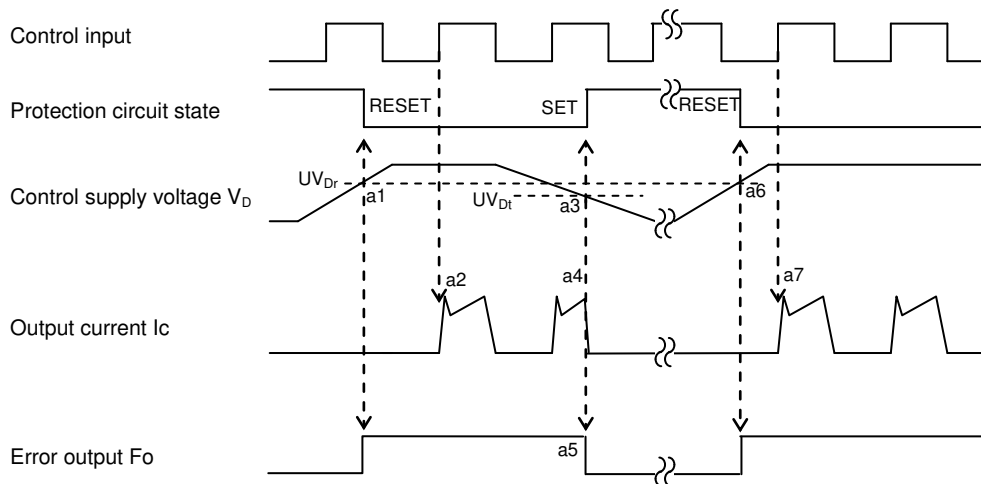a7. Normal operation: IGBT ON and outputs current.

Fig.2-2-4 Timing chart of N-side UV protection

[P-side UV Protection Sequence]
a1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr},
    IGBT turns on by next ON signal (L→H).
a2. Normal operation: IGBT ON and outputs current.
a3. V_{DB} level dips to under voltage trip level (UV_{DBt}).
a4. IGBT of the correspond phase only turns OFF in spite of control input signal level,
    but there is no F_O signal output.
a5. V_{DB} level reaches UV_{DBr}.
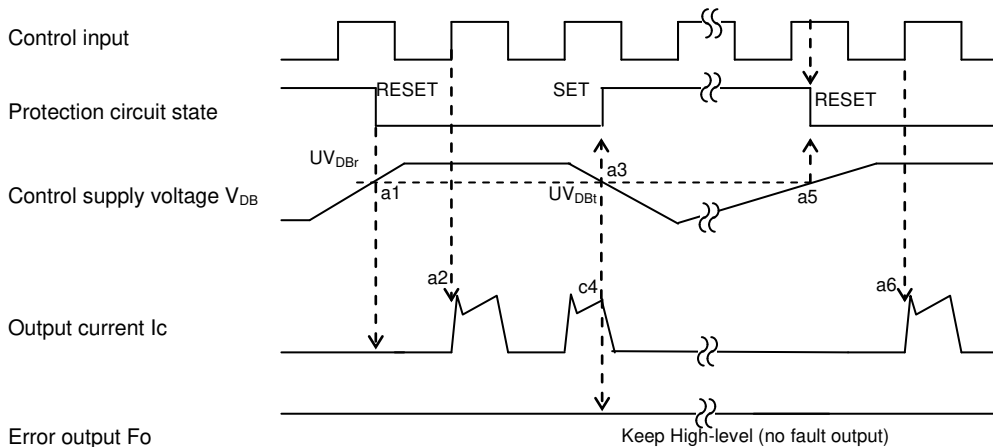a6. Normal operation: IGBT ON and outputs current.

Fig.2-2-5 Timing Chart of P-side UV protection

2.2.3 OT Protection (PS219B*-ST/AST/CST only)

PS219B*-T series have OT (over temperature) protection function by monitoring LVIC temperature rise.
While LVIC temperature exceeds and keeps over OT trip temperature, error signal Fo outputs and all N-side IGBTs are shut down without reference to input signal. (P-side IGBTs are not shut down)
The specification of OT trip temperature and its sequence are described in Table 2-2-5 and Fig.2-2-6.

Table 2-2-5 OT trip temperature specification

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Over temperature protection	OT_t	V_D=15V, At temperature of LVIC	Trip level	100	120	140	°C
	OT_{rh}		Trip/reset hysteresis	-	10	-	

[OT Protection Sequence]
a1. Normal operation: IGBT ON and outputs current.
a2. LVIC temperature exceeds over temperature trip level(OT_t).
a3. All N-side IGBTs turn OFF in spite of control input condition.
a4. Fo outputs for t_{Fo}=minimum 20μs, but output is extended during LVIC temperature keeps over OT_t.
a5. LVIC temperature drops to over temperature reset level.
a6. Normal operation: IGBT turns on by next ON signal (L→H).
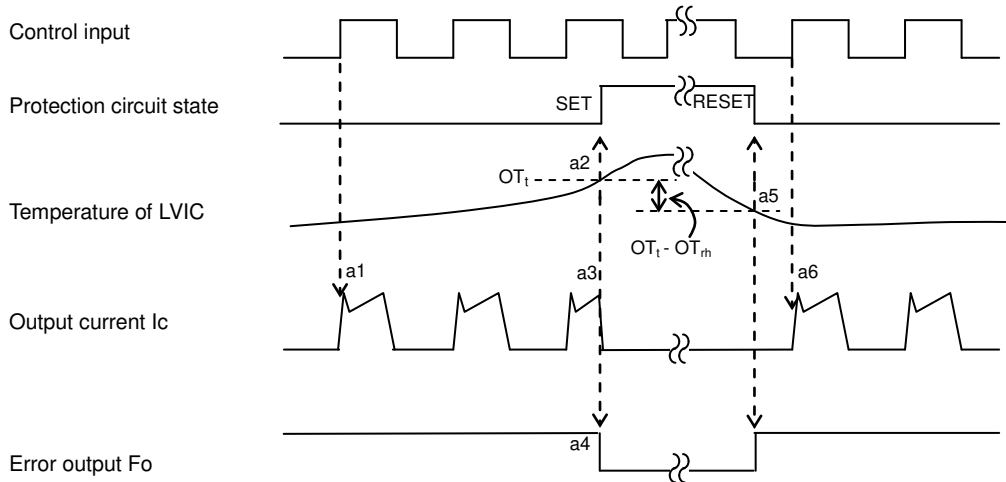 (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
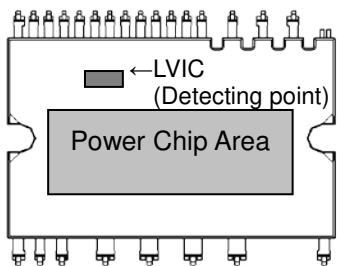
Fig.2-2-6 Timing Chart of OT protection
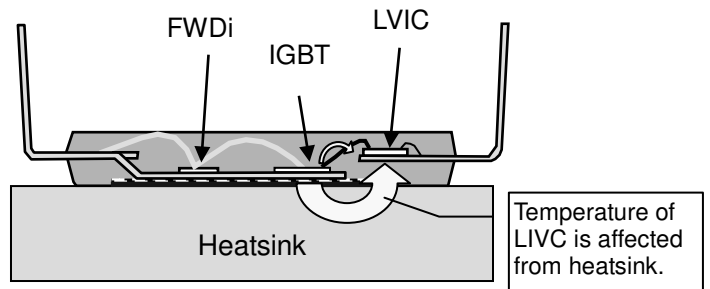
Fig.2-2-7 Temperature detecting point

Fig.2-2-8 Thermal conducting from power chips

Precaution about this OT protection function
(1)This OT protection will not work effectively in the case of rapid temperature rise like motor lock or over current. (This protection monitors LVIC temperature, so it cannot respond to rapid temperature rise of power chips.)

(2)If the cooling system is abnormal state (e.g. heat sink comes off, fixed loosely, or cooling fun stops) when OT protection works, can't reuse the DIPIPM. (Because the junction temperature of power chips will exceeded the maximum rating of Tj(150°C).)

2.2.4 Temperature output function V_{OT} (PS219B*-S/AS/CS only)

(1) Usage of this function

This function measures the temperature of control LVIC by built in temperature sensor on LVIC.
The heat generated at IGBT and FWDi transfers to LVIC through molding resin of package and outer heat sink. So LVIC temperature cannot respond to rapid temperature rise of those power chips effectively. (e.g. motor lock, short circuit) It is recommended to use this function for protecting from slow excessive temperature rise by such cooling system down and continuance of overload operation. (Replacement from the thermistor which was mounted on outer heat sink currently)

[Note]
In this function, DIPIPM cannot shutdown IGBT and output fault signal by itself when temperature rises excessively. When temperature exceeds the defined protection level, controller (MCU) should stop the DIPIPM.

(2) V_{OT} characteristics

V_{OT} output circuit, which is described in Fig.2-2-9, is the output of OP amplifier circuit. The current capability of V_{OT} output is described as Table 2-2-6. The characteristics of V_{OT} output vs. LVIC temperature is linear characteristics described in Fig.2-2-13. There are some cautions for using this function as below.

Table 2-2-6 Output capability
(Tc=-20°C ~100°C)

	min.
Source	1.7mA
Sink	0.1mA

Source: Current flow from V_{OT} to outside.
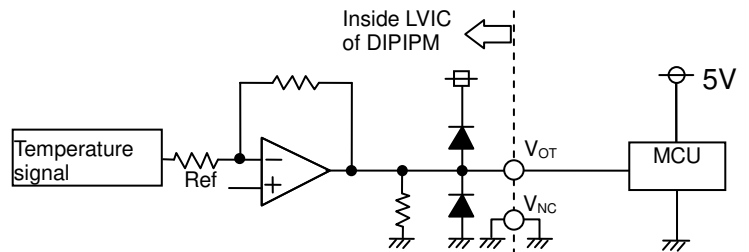Sink : Current flow from outside to V_{OT}.

Fig.2-2-9 V_{OT} output circuit

- In the case of detecting lower temperature than room temperature

It is recommended to insert 5kΩ(5.1kΩ is recommended.) pull down resistor for getting linear output characteristics at lower temperature than room temperature. When the pull down resistor is inserted between V_{OT} and V_{NC}(control GND), the extra current calculated by V_{OT} output voltage / pull down resistance flows as LVIC circuit current continuously. In the case of only using V_{OT} for detecting higher temperature than room temperature, it isn't necessary to insert the pull down resistor.
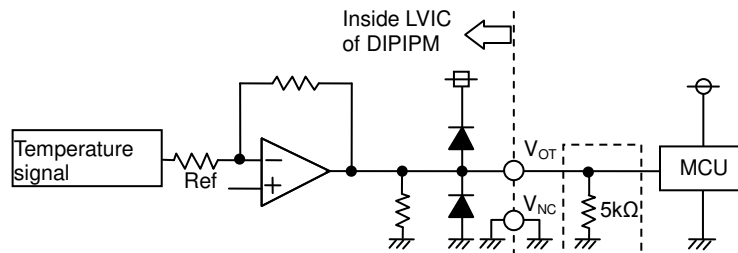

Fig.2-2-10 V_{OT} output circuit in the case of detecting low temperature

- In the case of using with low voltage controller(MCU)

In the case of using V_{OT} with low voltage controller (e.g. 3.3V MCU), V_{OT} output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and this output for preventing over voltage.
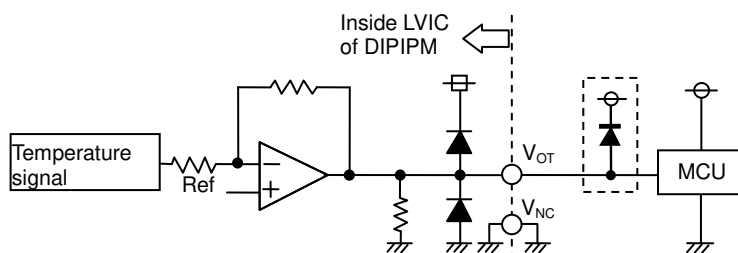

Fig.2-2-11 V_{OT} output circuit in the case of using with low voltage controller

- In the case that the protection level exceeds control supply of the controller

    In the case of using low voltage controller like 3.3V MCU, if it is necessary to set the trip V_{OT} level to control supply voltage (e.g. 3.3V) or more, there is the method of dividing the V_{OT} output by resistance voltage divider circuit and then inputting to A/D converter on MCU (Fig.2-2-12). In that case, sum of the resistances of divider circuit should be 5kΩ. About the necessity of clamp diode, we consider that the divided output will not exceed the supply voltage of controller generally, so it will be unnecessary to insert the clump diode. But it should be judged by the divided output level finally.
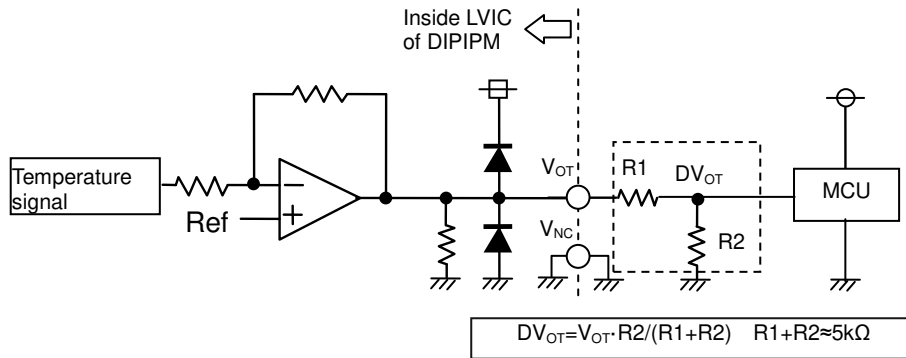

$$DV_{OT}=V_{OT}\cdot R2/(R1+R2) \quad R1+R2\approx5k\Omega$$

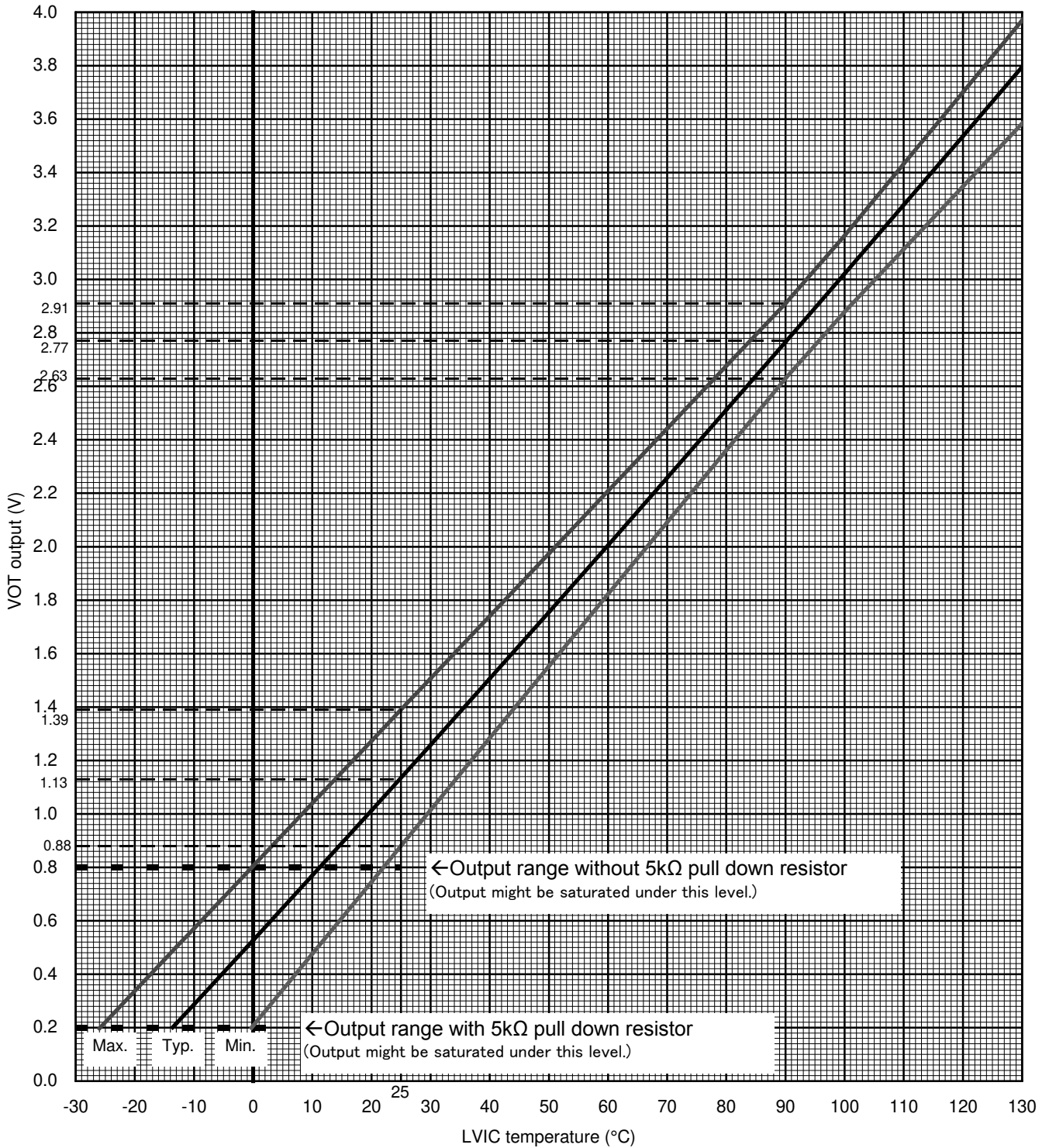Fig.2-2-12 V_{OT} output circuit in the case with high protection level

Fig.2-2-13 V_{OT} output vs. LVIC temperature

As mentioned above, the heat of power chips transfers to LVIC through the heat sink and package, so the relationship between LVIC temperature: Tic(=V_{OT} output), case temperature: Tc(under the chip defined on datasheet), and junction temperature: Tj depends on the system cooling condition, heat sink, control strategy, etc. For example, , their relationship example in the case of using the heat sink (Table 2-2-7) is described in Fig.2-2-14. This relationship may be different due to the cooling conditions. So when setting the threshold temperature for protection, it is necessary to get the relationship between them on your real system. And when setting threshold temperature Tic, it is important to consider the protection temperature assures Tc≤100°C and Tj ≤150°C.

Table 2-2-7 Outer heat sink

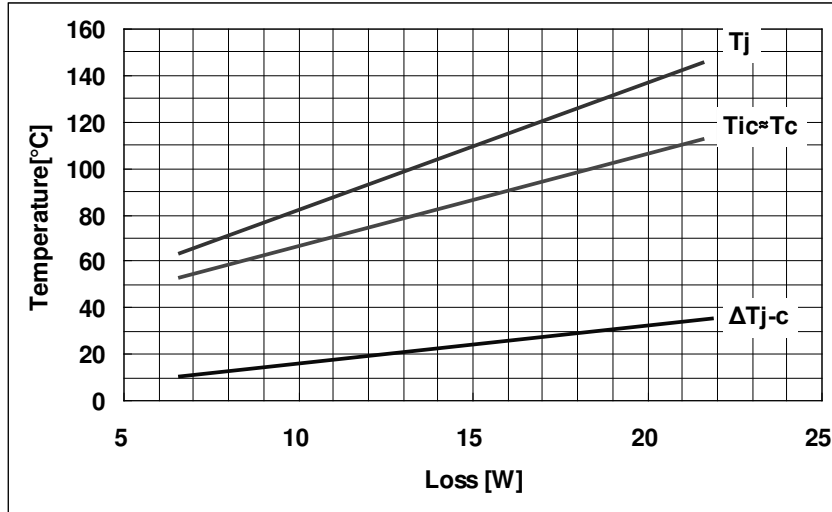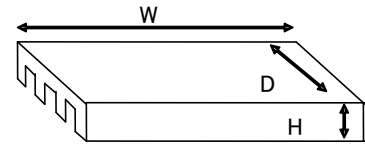| Heat sink size (W x D x H)	Thermal resistance Rth(f-a)
100 x 88 x 40 mm	2.20K/W

Fig.2-2-14 Example of relationship of Tj, Tc, Tic
（One IGBT chip turns on. DC current Ta=25°C, In this example, Tic and Tc are almost same temperature.）

Procedure about setting the protection level by using Fig.2-2-15 is described as below.

Table 2-2-8 Procedure for setting protection level

	Procedure	Setting value example
1)	Set the protection Tj temperature	Set Tj to 120°C as protection level.
2)	Get LVIC temperature Tic that matches to above Tj of the protection level from the relationship of Tj-Tic in Fig.2-2-15.	Tic=93°C (@Tj=120°C)
3)	Get V_{OT} value from the VOT output characteristics in Fig.2-2-16 and the Tic value which was obtained at phase 2) .	V_{OT}=2.84V (@Tic=93°C) is decided as the protection level.

As above procedure, the setting value for V_{OT} output is decided to 2.84V. But V_{OT} output has some data spread, so it is important to confirm whether the protection temperature fluctuation of Tj and Tc due to the data spread of V_{OT} output is Tj≤150°C and Tc≤100°C. Procedure about the confirmation of temperature fluctuation is described in Table 2-2-9.

Table 2-2-9 Procedure for confirmation of temperature fluctuation

	Procedure	Confirmation example
4)	Confirm the region of Tic fluctuation at above V_{OT} from Fig.2-2-16.	Tic=87°C~98.5°C (@V_{OT}=2.84V)
5)	Confirm the region of Tj and Tc fluctuation at above region of Tic from Fig.2-2-15.	Tj=113°C~126°C (≤150°C No problem) Tc=87°C~98.5°C (≤100°C No problem) In this example, Tic and Tc are almost same temperature, so Tc fluctuation is also same that of Tic
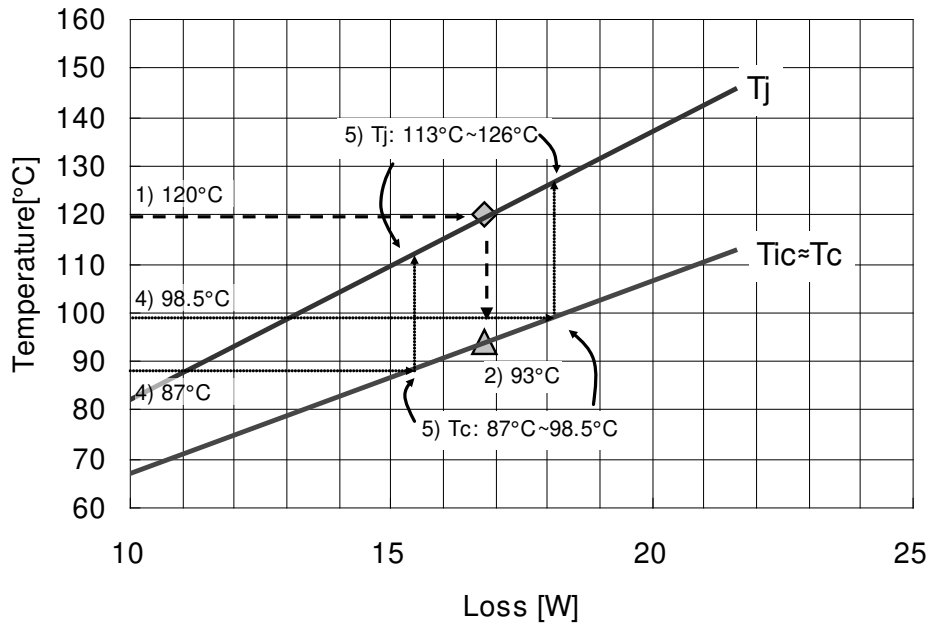
Fig.2-2-15 Relationship of Tj, Tc, Tic(Enlarged graph of Fig.2-2-14)
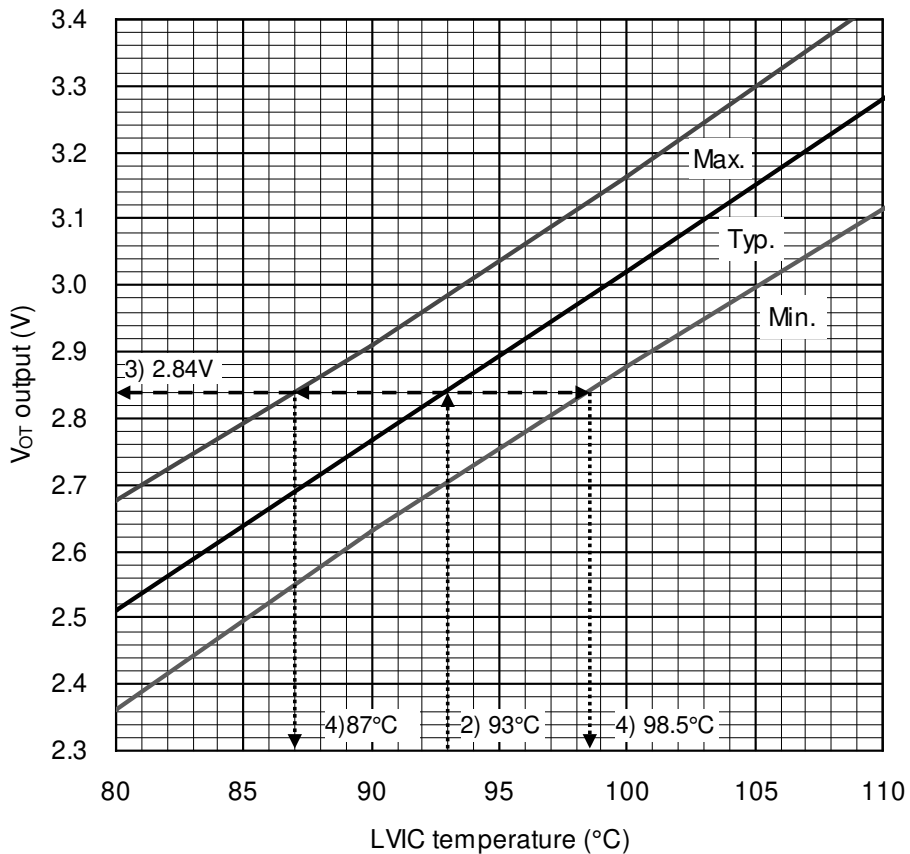
Fig.2-2-16 V_{OT} output vs. LVIC temperature (Enlarged graph of Fig.2-2-13)

As mentioned above, the relationship between Tic, Tc and Tj depends on the system cooling condition and control strategy, and so on. So please evaluate about these temperature relationship on your real system when considering the protection level.

If necessary, it is possible to ship the sample with the individual data of V_{OT} vs. LVIC temperature.

2.3 Package Outlines

2.3.1 Package outlines
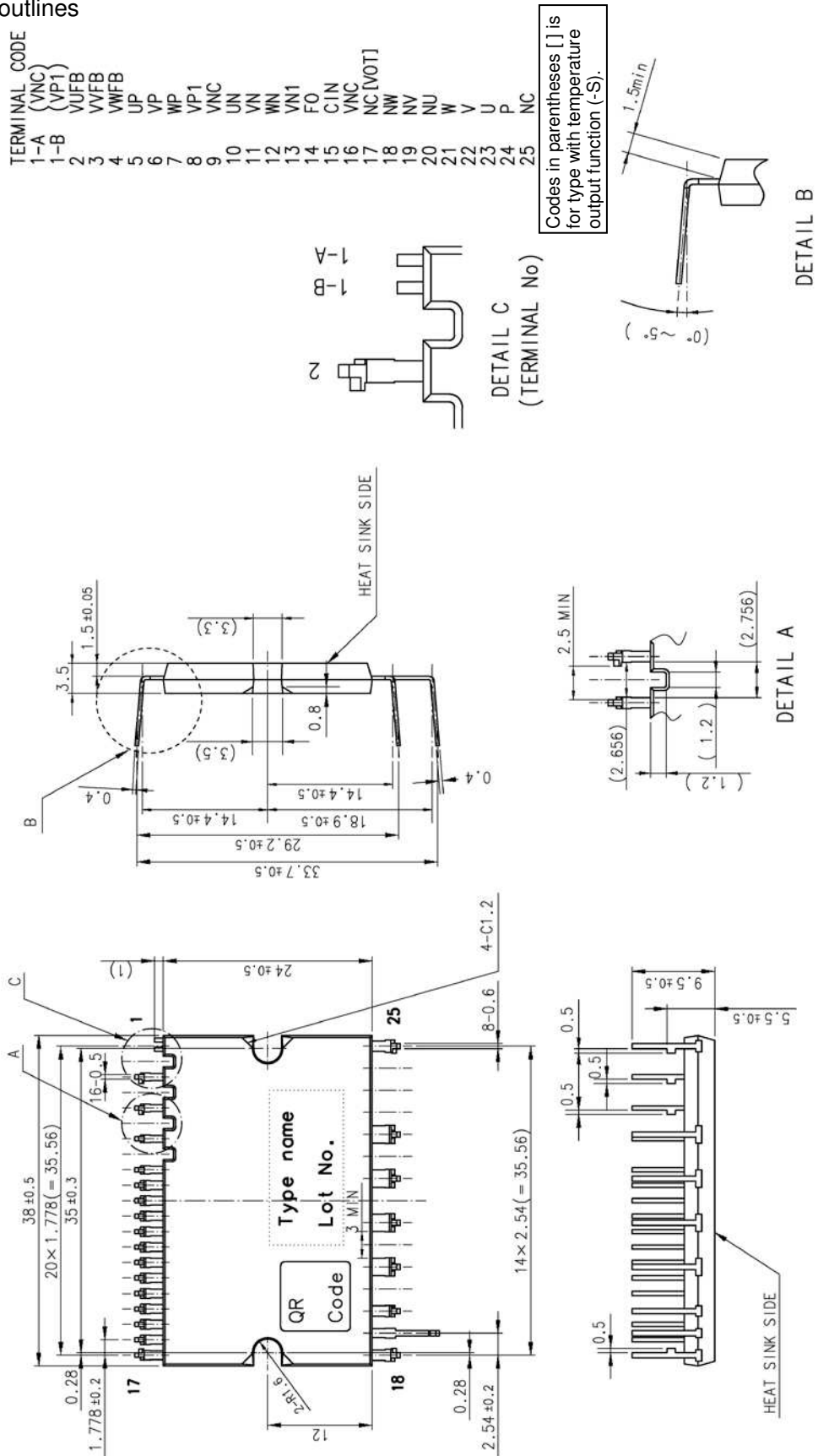
Dimensions in mm

Fig.2-3-1 Short pin type package (-S/-ST) outline drawing

TERMINAL CODE	
1-A	(VNC)
1-B	(VP1)
2	VUFB
3	VVFB
4	VWFB
5	UP
6	VP
7	WP
8	VP1
9	VNC
10	UN
11	VN
12	WN
13	VN1
14	FO
15	CIN
16	VNC
17	NC [VOT]
18	NW
19	NV
20	NU
21	W
22	V
23	U
24	P
25	NC

Codes in parentheses ( ) is for type with temperature output function (-AS).

DETAIL B

DETAIL C
(TERMINAL No)

DETAIL A

Dimensions in mm

(Note: Connect only one V_{NC} terminal to the system GND and leave another one open)
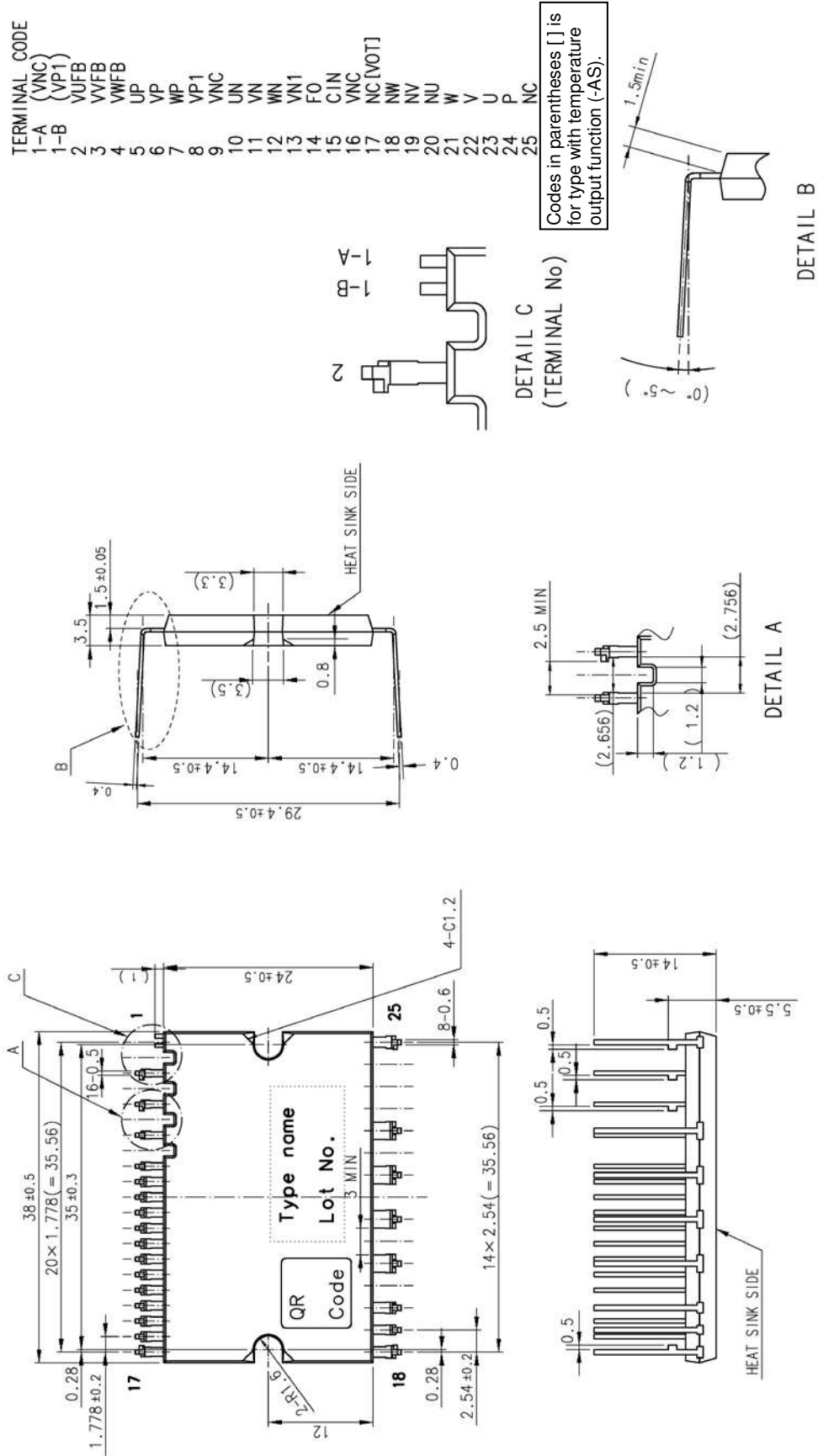
Fig.2-3-2 Long pin type package(-AS/-AST) outline drawing

TERMINAL CODE
1-A	(VNC)
1-B	(VP1)
2	VUFB
3	VVFB
4	VWFB
5	UP
6	VP
7	WP
8	VP1
9	VNC
10	UN
11	VN
12	WN
13	VN1
14	FO
15	CIN
16	VNC
17	NC [VOT]
18	NW
19	NV
20	NU
21	W
22	V
23	U
24	P
25	NC

Codes in parentheses [ ] is for type with temperature output function (-CS).

DETAIL B

1.5min

(0~5°)(0~5°)

DETAIL C (TERMINAL No)

1-B 1-A

2

Dimensions in mm

DETAIL A

(2.756)

(2.656)

(1.2)

(1.2)

1.5 ±0.05

3.5

0.8

(3.5)

14.4±0.5

18.9±0.5

14.4±0.5

29.2±0.5

33.7±0.5

0.4

0.4

B

4-C1.2

24±0.5

(1)

8-0.6

16-0.5

14×2.54(=35.56)

20×1.778(=35.56)

35±0.3

38±0.5

0.28

1.778±0.2

17

18

0.28

2.54±0.2

12

2-R1.6

Type name

Lot No.

3 MEN

QR Code

1

25

0.5

9.5±0.5

5.5±0.5

0.5

0.5

HEAT SINK SIDE

(Note: Connect only one V_{NC} terminal to the system GND and leave another one open)

Fig.2-3-3 Zigzag pin type package(-CS/-CST) outline drawing

2.3.2 Marking

The laser marking specification of DIP Ver.5 is described in Fig.2-3-4. Mitsubishi Corporate crest, Type name, Lot number, and QR code mark are marked in the upper side of module.
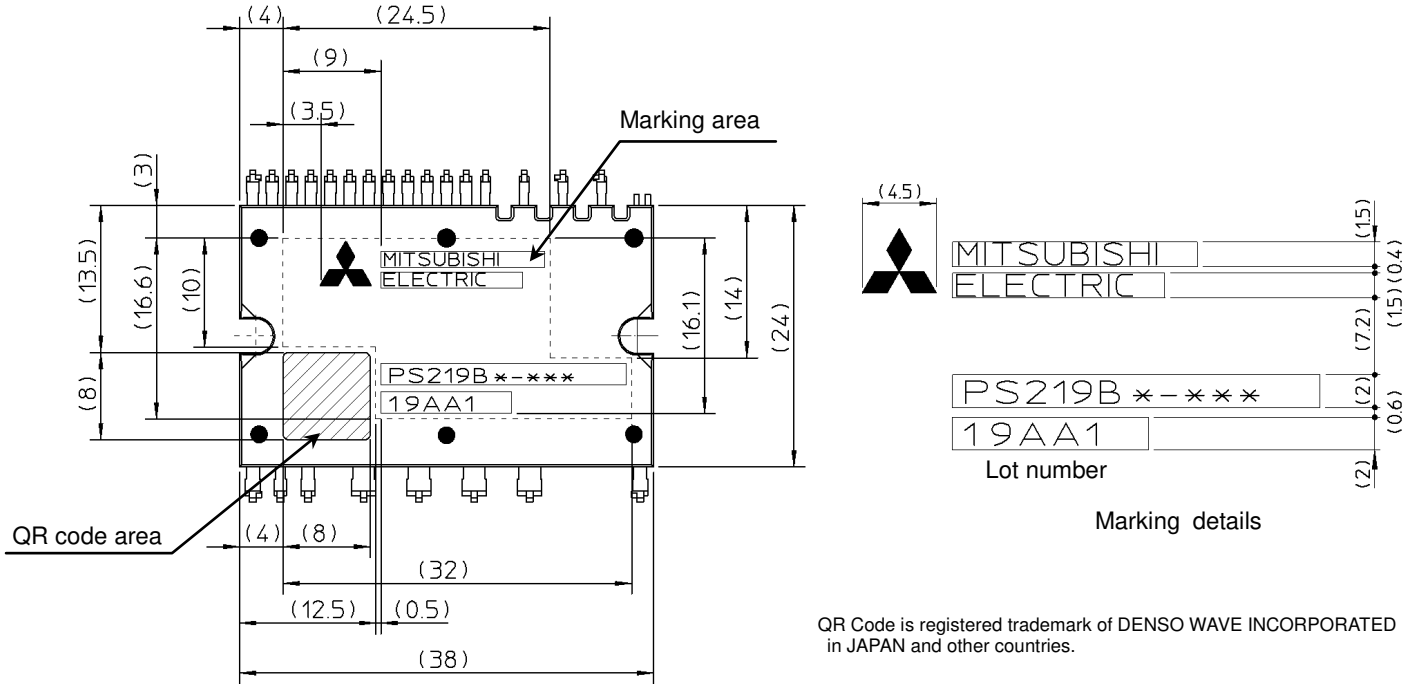
Fig.2-3-4 Laser marking view

The Lot number indicates production year, month, running number and country of origin.
The detailed is described as below.

(Example)   C 1 9 AA1

→ Running number
→ Product month (however O: October, N: November, D: December)
→ Last figure of Product year (e.g. 2011)
→ Factory identification
    No mark : Manufactured at the factory in Japan
    C   : Manufactured at the factory A in China
    H   : Manufactured at the factory B in China