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Data Sheet, DS1, Jan. 2003

IPAC-X

ISDN PC Adapter Circuit

PSB/PSF 21150, V 1.4

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Edition 2003-01-30

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Page	Subjects (major changes since last revision)
Chapter 1	Comparison IPAC/IPAC-X
Chapter 3.3.7.2	S- Transceiver Synchronization New
Chapter 3.3.11	Test Functions extended
Chapter 3.7.1.1	CDA Handler Description extended
Chapter 3.7.5.1	TIC Bus Access Control: Note added
Chapter 5.6	IOM-2 Interface Timing: Explanation added
Chapter 5.7.2	Parallel Microcontroller Interface Timing: Explanation added
Chapter 5.10	S-Transceiver
Chapter 5.11	Recommended Transformer Specificatio: Changed
Chapter 5.12	Line Overload Protection added
Chapter 5.13	EMC/ESD added

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1 Overview

The ISDN PC Adapter Circuit Extended IPAC-X integrates all necessary functions for a host based ISDN access solution on a single chip. It is based on the IPAC PSB 2115, and provides enhanced features and functionality.

It includes the S-transceiver (Layer 1), an HDLC controller for the D-channel and two protocol controllers for each B-channel. They can be used for HDLC protocol or transparent access.

The system integration is simplified by several configurations of the parallel microcontroller interface selected via pin strapping. They include multiplexed and demultiplexed interface selection as well as the optional indirect register access mechanism which reduces the number of necessary registers in the address space to 2 locations. The IPAC-X also provides a serial control interface (SCI).

The FIFO size of the cyclic B-channel buffers is 128 bytes per channel and per direction, with programmable block size (threshold). Besides TE mode the S-transceiver supports other terminal relevant operation modes like line termination subscriber side (LT-S) and line termination trunk side (LT-T). A multi-line ISDN solution to support both S and U line coding is simplified as well as multi-line solution with up to 3 S-interfaces.

An auxiliary I/O port has been added with interrupt capabilities on two input lines. These programmable I/O lines may be used to connect peripheral components to the IPAC-X which need software control or have to forward status information to the host.

Three programmable LED outputs can be used to indicate certain status information, one of them is capable to indicate the activation status of the S-interface automatically.

The IPAC-X is produced in advanced CMOS technology.

Table 1 Comparison of the IPAC-X with the Previous Version IPAC:

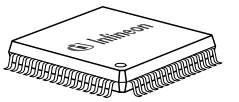
	IPAC-X PSB 21150	IPAC PSB 2115
Operating modes	TE, LT-T, LT-S, NT, Int. NT	TE, LT-T, LT-S, Int. NT
Supply voltage	3.3 V ± 5 %	5 V ± 5 %
Technology	CMOS	CMOS
Package	P-MQFP-64 / P-TQFP-64	P-MQFP-64 / P-TQFP-64
Transceiver Transformer ratio for the transmitter receiver	 1:1 1:1	 2:1 2:1
Test Functions	- Dig. loop via Layer 2 (TLP) - Layer 1 disable (DIS_TR) - Analog loop (LP_A-bit, EXLP-bit, ARL)	- Dig. loop via Layer 2(TLP) - Layer 1 disable (TEM) - Analog loop (ARL)
Microcontroller Interface	Serial interface (SCI) 8-bit parallel interface: Motorola Mux Siemens/Intel Mux Siemens/Intel Non-Mux direct/ indirect Addressing	Not provided 8-bit parallel interface: Motorola Mux Siemens/Intel Mux Siemens/Intel Non-Mux
Crystal	7.68 MHz	7.68 MHz
Buffered 7.68 MHz output	Provided	Provided
Controller data access to IOM-2 timeslots	All timeslots; various possibilities of data access	Restricted access to B- and IC-channel
Data control and manipulation	Various possibilities of data control and data manipulation (enable/ disable, shifting, looping, switching)	B- and IC-channel looping
IOM-2		
IOM-2 Interface	Double clock (DCL), bit clock pin (BCL), serial data strobe 1 (SDS1) serial data strobe 2 (SDS2)	Double clock (DCL), bit clock (BCL), serial data strobe (SDS)

	IPAC-X PSB 21150	IPAC PSB 2115
Monitor channel programming	Provided (MON0, 1, 2, ..., 7)	Provided (MON0 or 1)
C/I channels	CI0 (4 bit), CI1 (4/6 bit)	CI0 (4 bit), CI1 (6 bit)
Layer 1 state machine	With changes for correspondence with the actual ITU specification	
Layer 1 state machine in software	Possible	Not possible
Support of IDSL (144kBit/s)	Provided (HDLC controller access, SDS1/2 signals active)	Not provided
D-channel HDLC support	D- and B-channel timeslots; non-auto mode, transparent mode 0-2, extended transparent mode	D-channel timeslot; auto mode, non-auto mode, transparent mode 1-3
D-channel FIFO size	64 bytes cyclic buffer per direction with programmable FIFO thresholds	2x32 bytes buffer per direction
B-channel HDLC support	D- and B-channel timeslots; non-auto mode, transparent mode 0-2, extended transparent mode	D-channel timeslot; non-auto mode, transparent mode 0,1 extended transparent mode
B-channel FIFO size	128 bytes cyclic buffer per direction for each channel with programmable FIFO thresholds	2x64 bytes buffer per direction
Reset Sources	$\overline{\text{RES}}$ Input Watchdog C/I Code Change $\overline{\text{EAW}}$ Pin Software Reset	RST Input Watchdog C/I Code Change EAW Pin
Interrupt Output Signals	$\overline{\text{INT}}$ low active (open drain) by default, reprogrammable to high active (push-pull)	Low active $\overline{\text{INT}}$

	IPAC-X PSB 21150	IPAC PSB 2115
8-bit Auxiliary Interface	Provided	Provided
PCM Interface	Not Provided	Provided
Functions FBOUT, $\overline{\text{INT0/1}}$	Provided	Provided
Reset Signals	$\overline{\text{RES}}$ input signal $\overline{\text{RSTO}}$ output signal	RES input/output signal
Pin SCLK	1.536 MHz	512 kHz
Timeslots of arbitrary lenght	not available	available (“Clock Mode 5”)

V 1.4

1.1 Features



P-MQFP-64-1

P-TQFP-64-1

- Single chip host based ISDN solution
- Based on IPAC PSB 2115, integrating ISAC-S and HSCX-TE functionality
- 8-bit parallel microcontroller interface, Motorola and Siemens/Intel bus type multiplexed or non-multiplexed, direct-/indirect register addressing
- Serial control interface (SCI)
- Microcontroller access to all IOM-2 timeslots
- Various types of protocol support (Non-auto mode, transparent mode, extended transparent mode)
- B-channel HDLC controllers with 128 byte FIFOs
- Flexible access to 18-bit timeslots (2B+D) on IOM-2 for IDSL support
- D-channel HDLC controller with 64 byte FIFOs
- IOM-2 interface in TE, LT-T, LT-S and NT mode, single/double clocks and two strobe signals
- D-channel priority handler on IOM-2 for intelligent NT applications
- Monitor channel handler (master/slave)
- IOM-2 MONITOR and C/I-channel protocol to control peripheral devices
- Full duplex 2B+D S/T-interface transceiver according to ITU-T I.430
- Conversion of the frame structure between the S/T-interface and IOM-2
- Receive timing recovery
- D-channel access control
- Activation and deactivation procedures with automatic activation from power down state
- Access to S and Q bits of S/T-interface

Type	Package
PSB/PSF 21150 H	P-MQFP-64-1
PSB/PSF 21150 F	P-TQFP-64-1

- Adaptively switched receive thresholds
- Auxiliary Interface with general purpose I/O pins and LED drivers
- Two programmable timers
- Watchdog timer
- Test loops
- Sophisticated power management for restricted power mode
- Power supply 3.3 V
- 3.3 V output drivers, inputs are 5 V safe
- Advanced CMOS technology

1.2 Logic Symbol

The logic symbol gives an overview of the IPAC-X functions. It must be noted that not all functions are available simultaneously, but depend on the selected mode.

Pins which are marked with a " * " are multiplexed and not available in all modes.

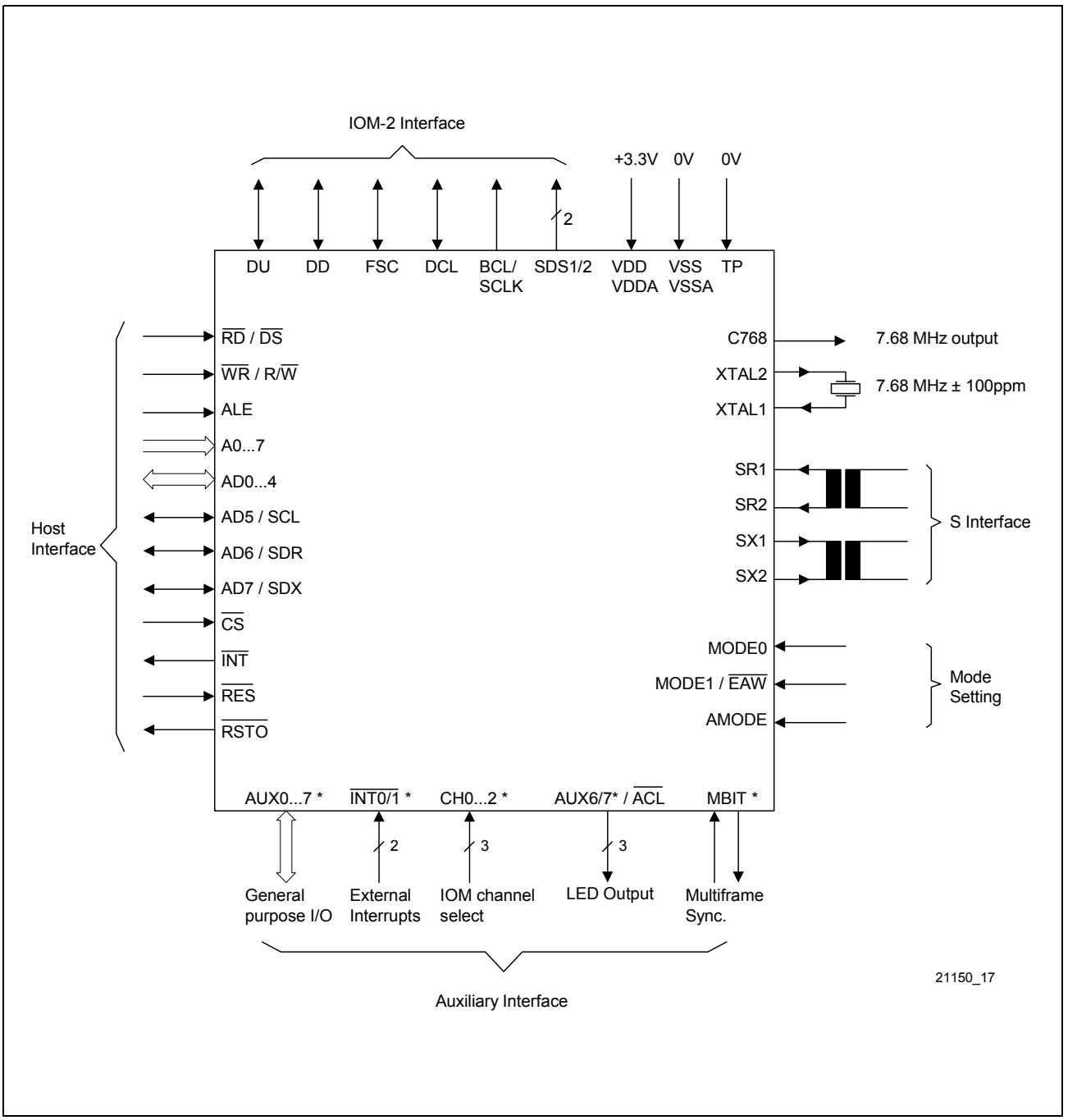


Figure 1 Logic Symbol of the IPAC-X

1.3 Typical Applications

The IPAC-X can be used in a variety of applications like

- ISDN PC adapter card for S interface (**Figure 2**)
- ISDN PC adapter card for U or S interface (**Figure 3**)
- ISDN voice/data terminal (**Figure 4**)
- ISDN stand-alone terminal with POTS interface (**Figure 5**)

An ISDN adapter card for a PC is built around the IPAC-X using a USB, PCI or ISA Plug and Play interface device depending on the required PC interface. The IPAC-X can be connected to any bus interface logic as it provides a standard 8-bit parallel µC interface and a serial control interface (SCI).

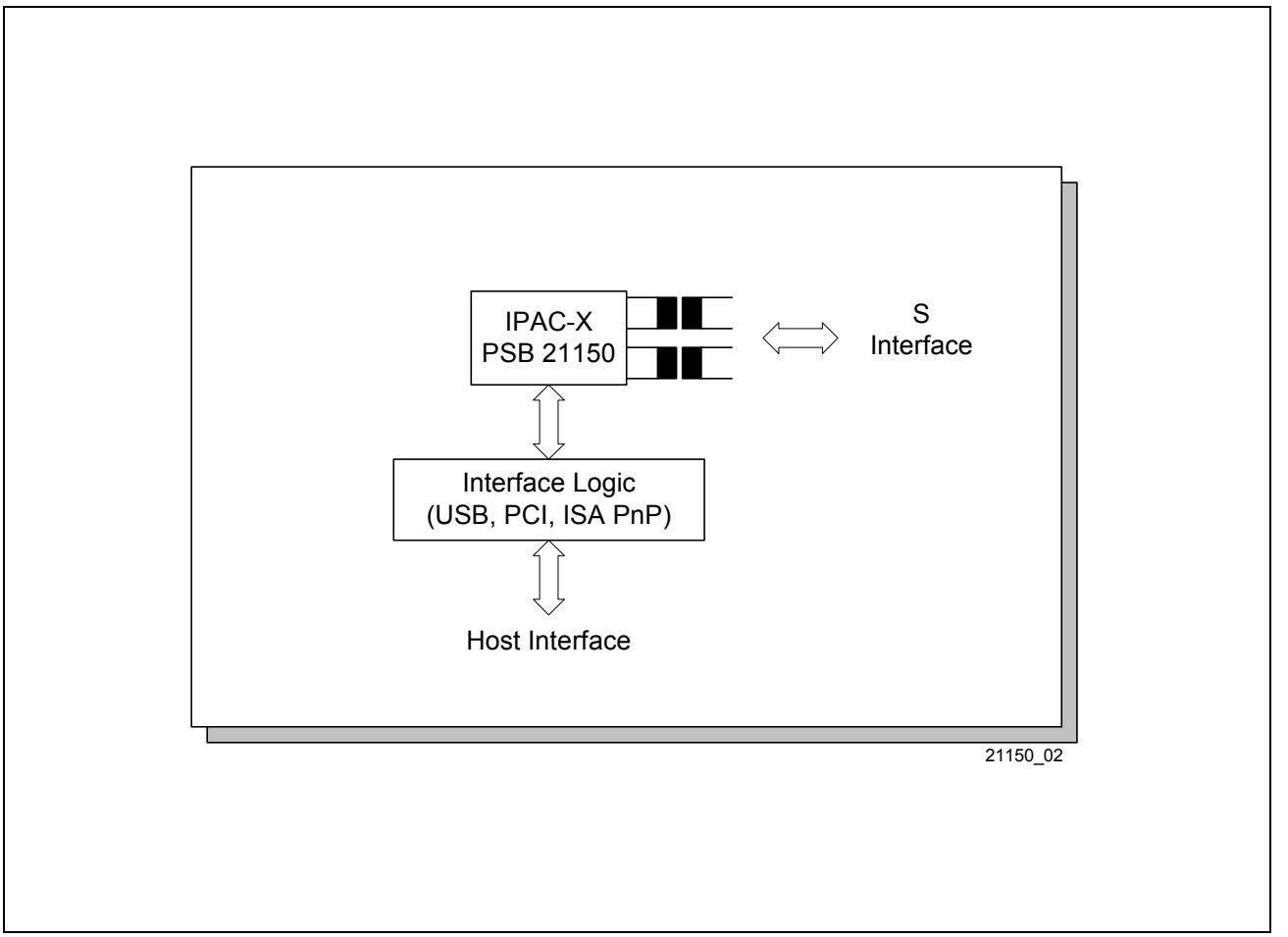


Figure 2 ISDN PC Adapter Card for S Interface

An ISDN adapter card which supports both U and S interface may be realized using the IPAC-X together with the PSB 21911 IEC-Q TE. The S interface may be configured for TE or LT-S mode supporting intelligent NT applications.

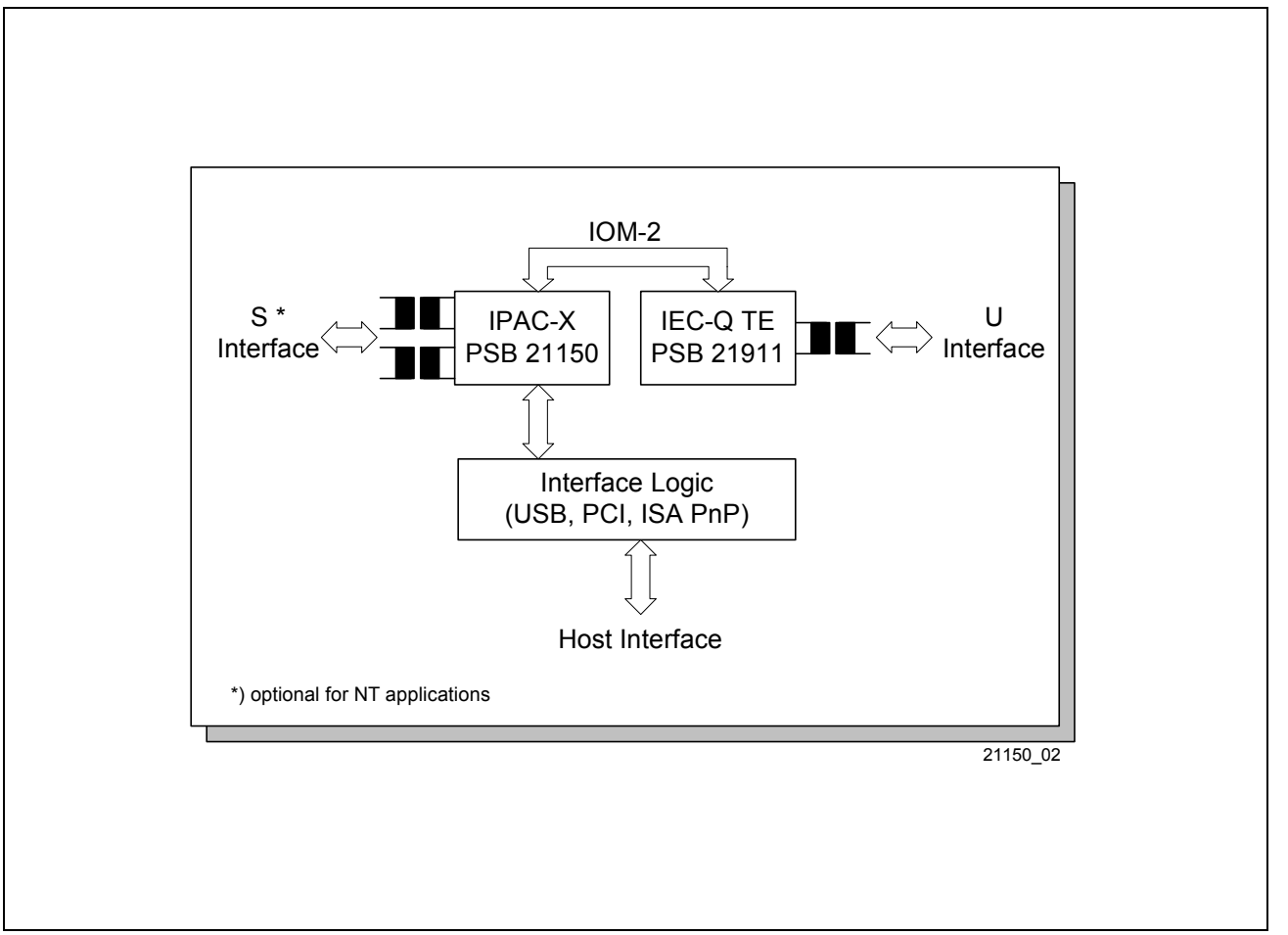


Figure 3 ISDN PC Adapter Card for U or S Interface

The figure below shows a voice data terminal developed on a PC card where the IPAC-X provides its functionality as data controller and S interface within a two chip solution. During ISDN calls the PSB 2163 ARCOFI-SP provides speakerphone functions and includes a DTMF generator. Additionally, a DTMF generator of keypad may be connected to the auxiliary interfce of the IPAC-X.

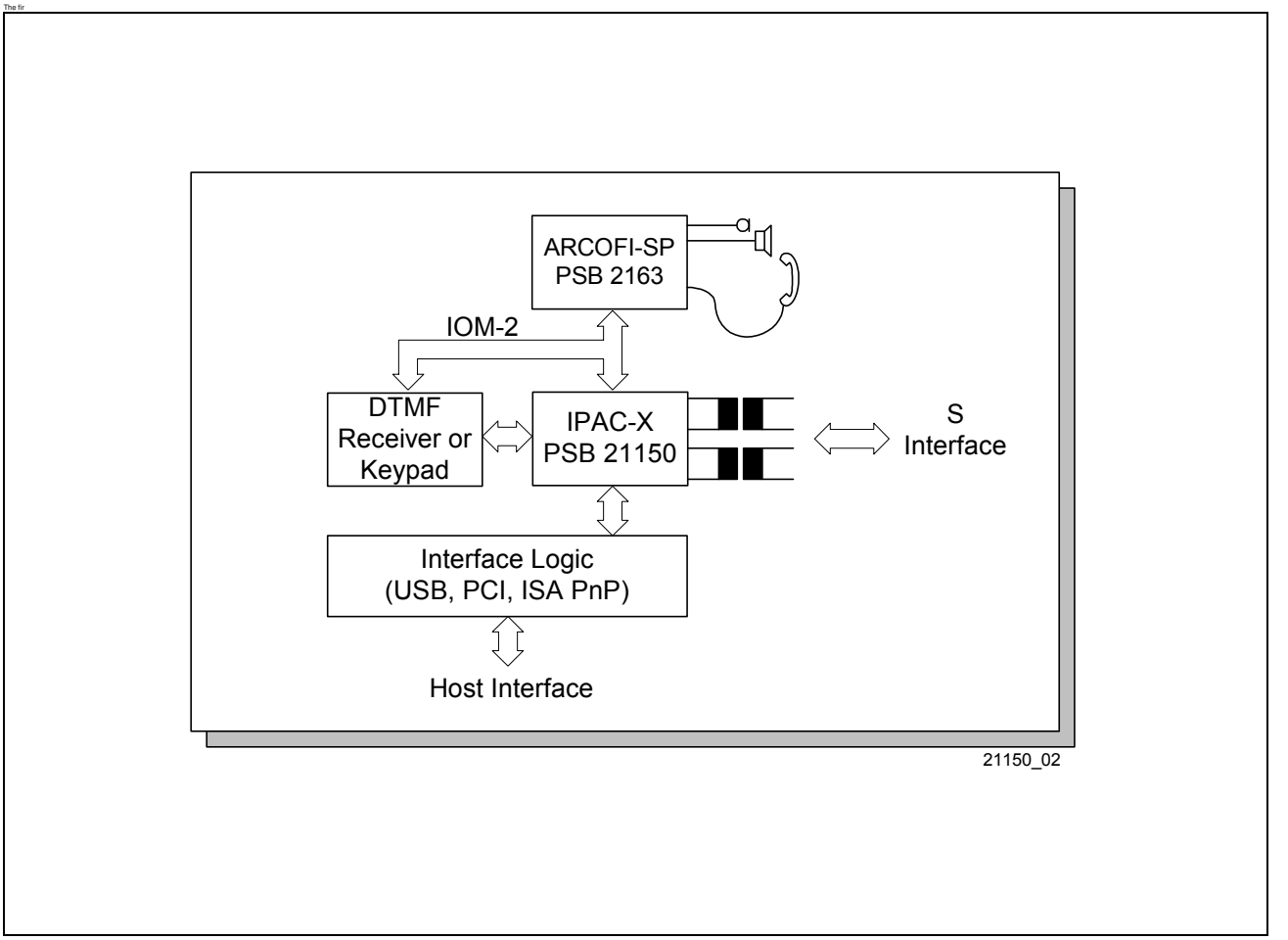


Figure 4 ISDN Voice/Data Terminal

The IPAC-X can be integrated in a microcontroller based stand-alone terminal that is connected to the communications interface of a PC. The SICOFI2-TE PSB 2132 enables connection of analog terminals (e.g. telephone or fax) to the dual channel POTS interface.

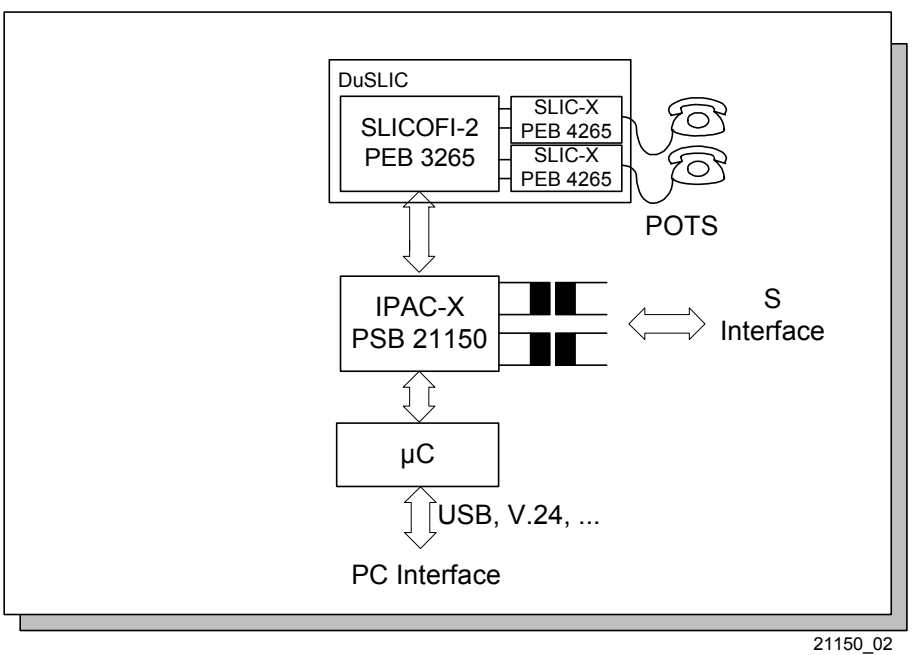


Figure 5 ISDN Stand-Alone Terminal with POTS Interface

2 Pin Configuration

P-MQFP-64-1
P-TQFP-64-1

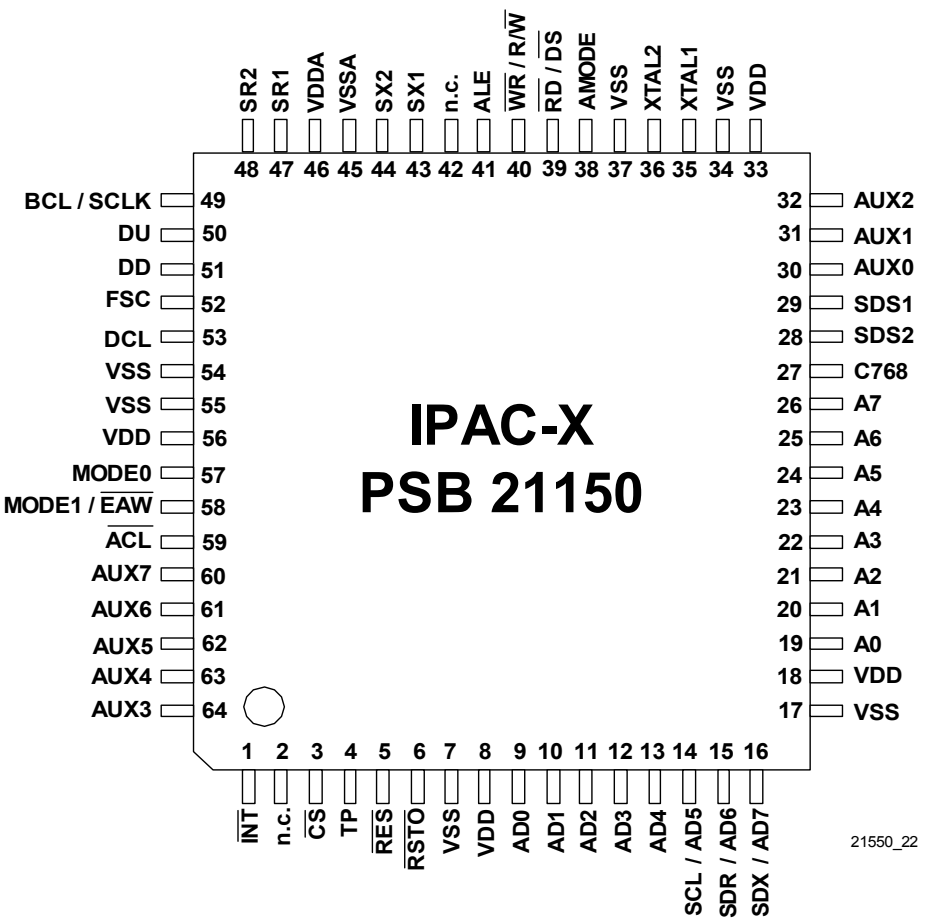


Figure 6 Pin Configuration of the IPAC-X

Table 2 IPAC-X Pin Definitions and Functions

Pin No. MQFP-64 TQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
Host Interface			
19 20 21 22 23 24 25 26	A0 A1 A2 A3 A4 A5 A6 A7	I I I I I I I I	• **Non-Multiplexed Bus Mode:** **Address Bus** Address bus transfers addresses from the microcontroller to the IPAC-X. For indirect address mode only A0 is valid (A1-A7 to be connected to VDD). • **Multiplexed Bus Mode:** Not used in multiplexed bus mode. In this case A0-A7 should directly be connected to VDD.
9 10 11 12 13	AD0 AD1 AD2 AD3 AD4	I/O I/O I/O I/O I/O	• **Multiplexed Bus Mode:** **Address/data bus** Transfers addresses from the microcontroller to the IPAC-X and data between the microcontroller and the IPAC-X. • **Non-Multiplexed Bus Mode:** **Data bus** Transfers data between the microcontroller and the IPAC-X.
14	AD5 SCL	I/O I	• **Multiplexed Bus Mode:** **Address/data bus** Address/data line AD5 if the parallel interface is selected. • **Non-Multiplexed Bus Mode:** **Data bus** Data line D5 if the parallel interface is selected. **SCI - Serial Clock** Clock signal of the SCI interface if a serial interface is selected.