Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SICOFI®2-TE Two Channel Codec Filter for Terminal Application

PSB 2132 Version 2.2

Wired Communications

Infineon technologies

Never stop thinking.

Edition 2001-02-20

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München, Germany

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

SICOFI®2-TE

Two Channel Codec Filter for Terminal Application

PSB 2132 Version 2.2

Wired Communications

Infineon technologies

Never stop thinking.

Revision History:	**Current Version 2001-02-20**	DS 1
Previous Version:	Data Sheet 07.97 DS1 (V 1.1) Delta Sheet 11.98 DS2 (V 1.4) Errata Sheet 05.98 DS1 (V 1.4)	

Page	Subjects (major changes since last revision)

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at http://www.infineon.com/

Table of Contents Page

Table of Contents **Page**

Table of Contents Page

List of Figures

List of Tables

Preface

This document provides detailed technical information about the SICOFI®2-TE. It is intended for anyone considering or using the device for system design or board layout for a broad range of analog telephony applications.

Organization of this Document

This Hardware Reference Manual is organized as follows:

- Chapter 1, Overview
  Includes a general description of the architecture, feature list, and logic symbol.
- Chapter 2, Pin Descriptions
  Illustrates the Pin Configuration and provides detailed functional descriptions.
- Chapter 3, Functional Description
  Provides a block diagram and summarizes the major functional blocks.
- Chapter 4, Operational Description
  Begins with a state diagram and description of the operating states of all two channels and concludes with detailed transmission characteristics.
- Chapter 5, Interface Descriptions
  Describes the Analog, IOM-2 PCM, Signaling, and Serial Microcontroller interfaces.
- Chapter 6, Programming Overview
  Illustrates the register model and coefficient RAM structure, provides a register map and summary, and identifies the programming command sequences.
- Chapter 7, Application Hints
  Describes the development system available for the PSB 2132, and provides guidelines and schematics for board layout.
- Chapter 8, Electrical Characteristics and Timing Diagrams
  Provides detailed tables for the electrical characteristics and includes timing diagrams for the Analog, IOM-2 PCM, Serial Microcontroller, and Signaling interfaces.
- Chapter 9, Test Configuration
  Describes the test loops and cut-offs available for functional tests and diagnostics.
- Chapter 10, Package Outlines
  Illustrates the P-MQFP-64 package in which the PSB 2132 is manufactured.
- The Appendix
  Includes a glossary and an index.

Related Documentation

Other documentation for the PSB 2132 includes a *Product Brief*, a *Product Overview*, a *Programmer's Reference Manual*, and assorted *Application Notes*. Similar documentation is also available for the other members of the SICOFI Codec family including the PSB 2134, PEB 2466, and PEB 2266. Documentation is available by accessing our website: http://www.infineon.com/sicofi

1 Overview

The two-channel codec filter PSB 2132 SICOFI®2-TE is built around a central DSP-core which provides independent filter structures for both channels. Its analog I/O pins are used to connect to external subscriber line interface circuits (SLICs). Their signals are internally routed to the analog-to-digital and digital-to-analog converters (ADC, DAC). The signaling pins carry line status and control information to and from the SLICs. Two programmable clock outputs are available, one of which can be used for generating a ringing signal (RGEN). The SICOFI®2-TE's IOM-2 PCM Interface connects directly to a 768 kbit/s IOM-2 bus, often used in terminal equipment. The digitized voice band signals are available as A-Law or µ-Law codes within selectable 8-bit time slots.

The SICOFI®2-TE modes, features, and filter characteristics are programmed through a serial interface to a microcontroller. The access mechanism is very simple, and can be implemented with as few as three I/O ports.

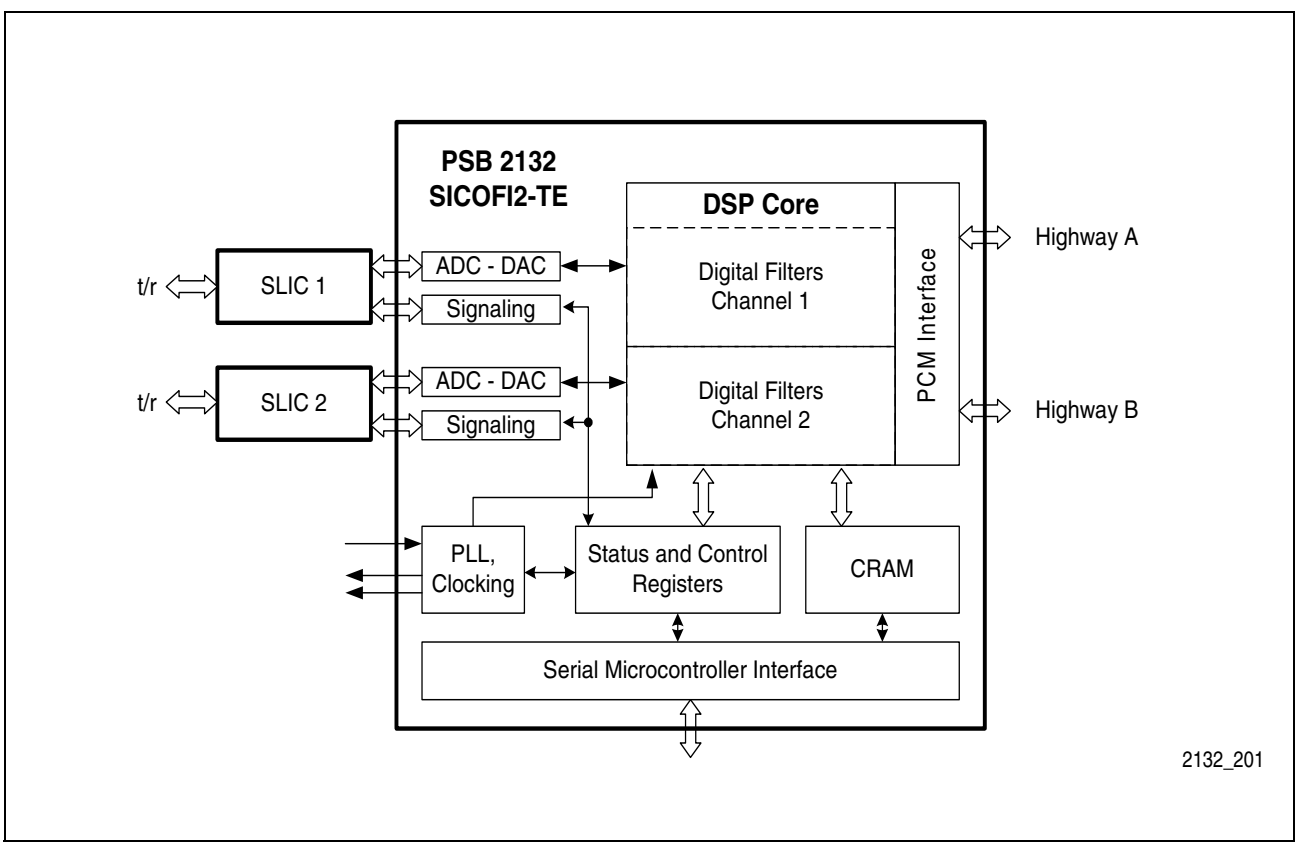


Figure 1 SICOFI®2-TE Architecture

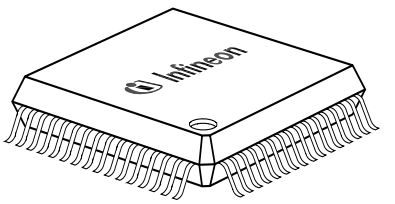
Two Channel Codec Filter for Terminal Application SICOFI®2-TE

PSB 2132

Version 2.2

CMOS

1.1 Features



P-MQFP-64

- Two-channel single chip codec with digital filters
- High analog driving capability (300 Ω, 50 pF) for direct driving of transformers
- Digital Signal Processing (DSP) technique
- Programmable digital filters to adapt transmission behavior, especially for:
  - AC impedance matching
  - Transhybrid balancing
  - Frequency response
  - Signal levels
  - A/µ-Law compression and expansion
- Fulfills international (e.g. ITU-T Q.552, G.712) and country-specific requirements
- High performance ADC and DAC for excellent linearity and dynamic gain
- Programmable Analog Interface to electronic SLICs or transformer solutions
- Seven SLIC-signaling I/O pins per channel with programmable debouncing
- IOM-2 compatible PCM interface (1.536 MHz DCL, 768 kHz Bit Clock)
- Easy to use 4-pin Serial Microcontroller Interface (SPI compatible) for read/write access
- Single supply voltage (5 V)
- Advanced low-power mixed-signal CMOS technology
- Two programmable tone generators per channel (DTMF possible)
- Level metering function for system tests and for analog input signal testing
- Advanced on-chip functions for device and system diagnostics and manufacturing test
  - Five digital loops
  - Four analog loops
- Support tools include:
  - Hardware development board — STUT 2466
  - QSICOS Coefficient Calculation and Register Configuration Software
- Standard P-MQFP-64 package

Type	Package
PSB 2132 Version 2.2	P-MQFP-64

1.2 Logic Symbol

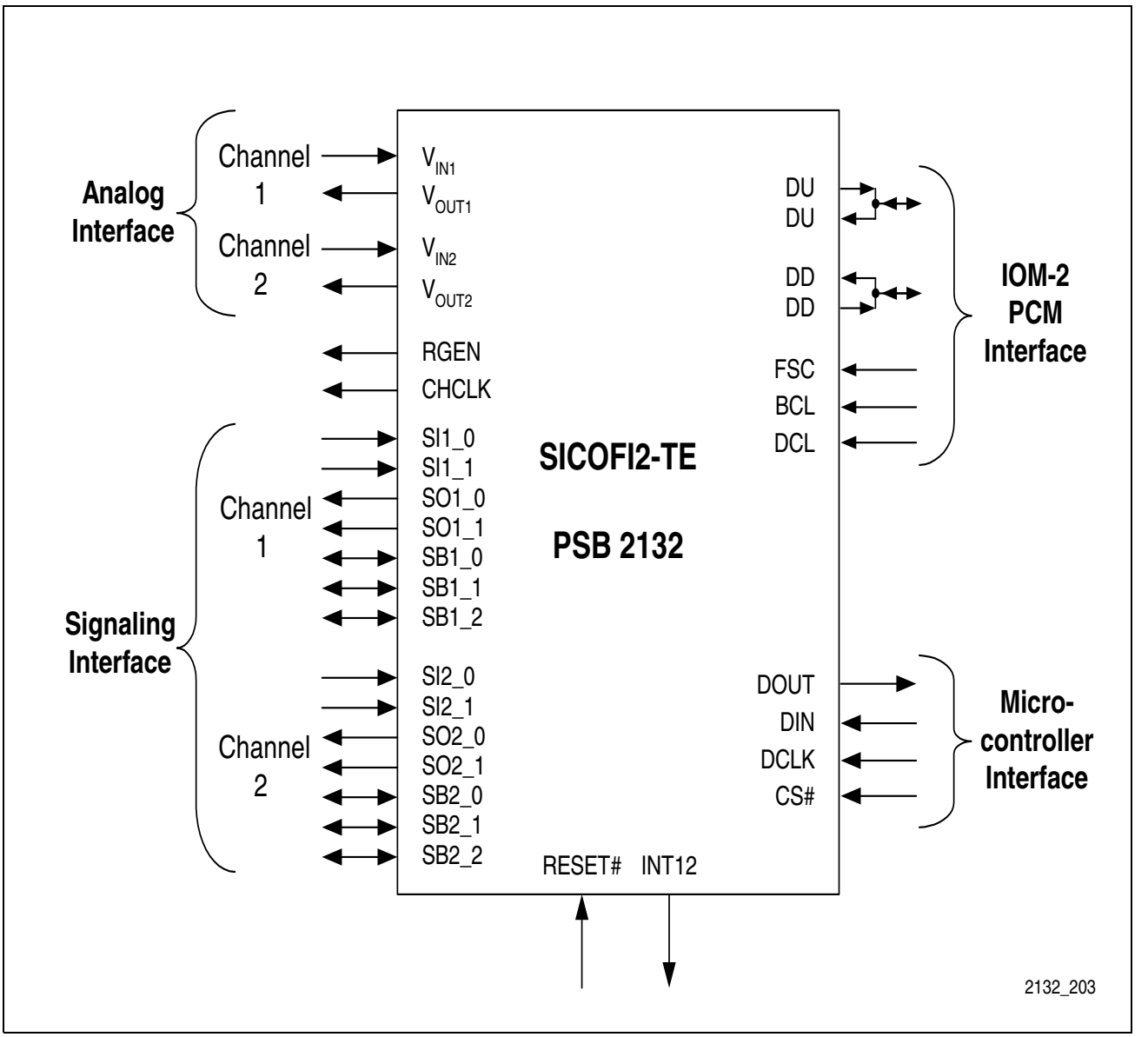


Figure 2 SICOFI®2-TE Logic Symbol

1.3 Typical Applications

Many applications will benefit from the versatility of the SICOFI®2-TE codec and filter. The inherent flexibility enables several products to be developed around one basic architecture, thus affording potentially significant savings in time to market, inventory costs, and support administration.

The following list represents some of the typical applications for which the SICOFI®2-TE codec was designed: Small PBX, Terminal Adapters, and intelligent NTs. Refer to the ***Product Overview***, **Chapter 5 Application Hints** for more information.

2 Pin Descriptions

2.1 Pin Diagram

(top view)

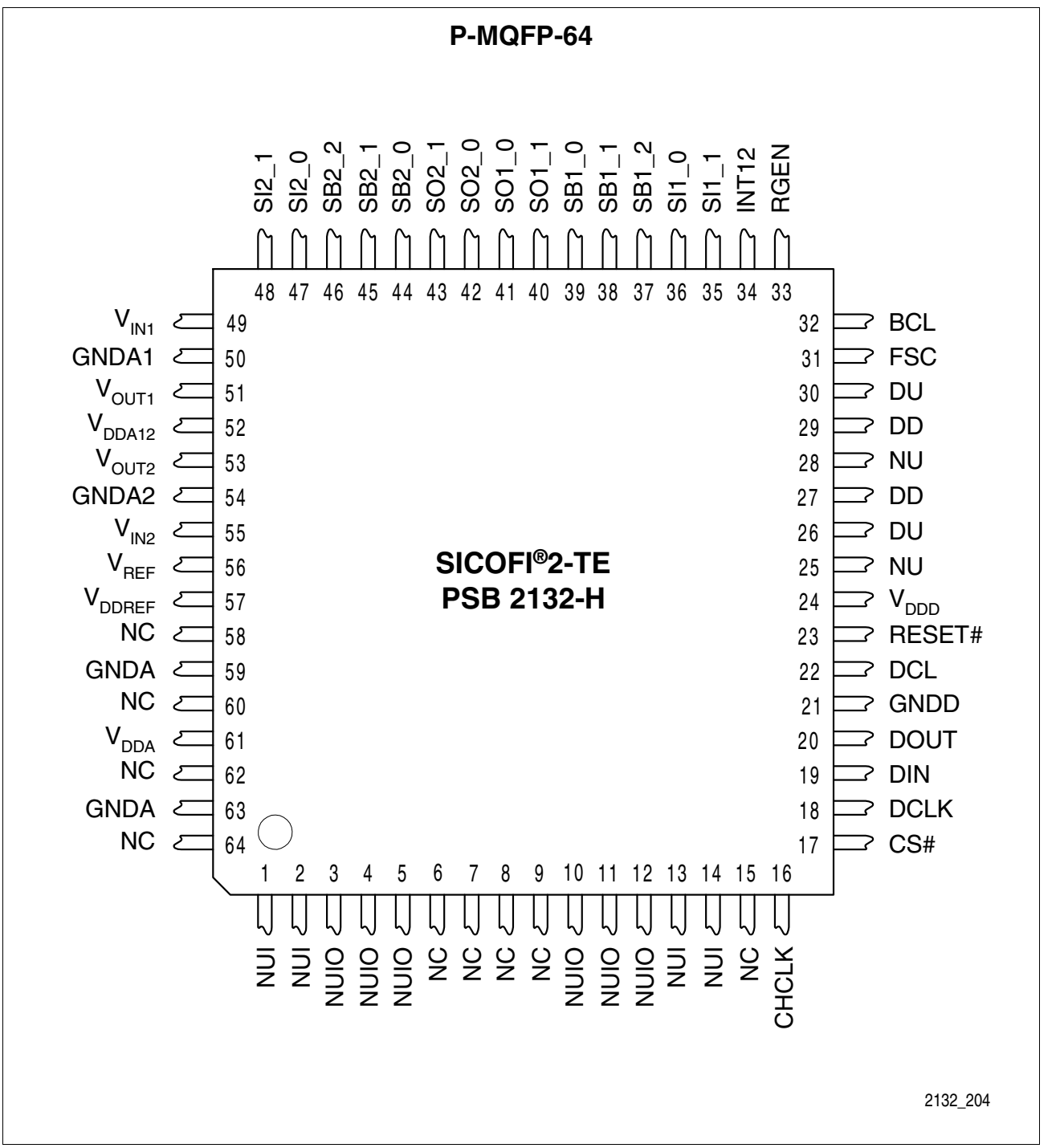


Figure 3 Pin Configuration of SICOFI®2-TE

2.2 Pin Definitions and Functions

Table 1 Pin Definitions and Functions

Pin	Symbol	Type	Function	Ch.
1, 2	NUI	I	**Non Usable Input** Pins must be tied directly to digital ground GNDD (Pin 21)	
3, 4, 5	NUIO	I/O	**Non Usable Input/Output** Pins must be tied via a pull-down-resistor to digital ground GNDD (Pin 21)	
6, 7, 8, 9	NC		**Not Connected** Pins are not connected in this device.	
10, 11, 12	NUIO	I/O	**Non Usable Input/Output** Pins must be tied via a pull-down resistor to digital ground GNDD (Pin 21)	
13, 14	NUI	I	**Non Usable Input** Pins must be tied directly to digital ground GNDD (Pin 21)	
15	NC		**Not Connected** Pin is not connected in this device.	
16	CHCLK	O	**Chopper Clock Output** Provides 256, 512, or 16,384 kHz signal; sync. to DCL.	both
17	CS#	I	**Chip Select** Microcontroller Interface Chip Select, enable to read or write; active low.	both
18	DCLK	I	**Data Clock** Microcontroller Interface data clock, shifts data from or to device; maximum clock rate 8192 kHz.	both
19	DIN	I	**Data Input** Microcontroller Interface control data input pin; DCLK determines data rate.	both
20	DOUT	O	**Data Output** Microcontroller Interface control data output pin; DCLK determines data rate: DOUT is high impedance "Z" if no data is transmitted from the SICOFI®2-TE.	both
21	GNDD	I	**Digital Ground** Ground reference for all digital signals. Internally isolated from GNDA1 (Pin 50), GNDA2 (Pin 54), and GNDA (Pins 59 and 63).	both

Pin	Symbol	Type	Function	Ch.
22	DCL	I	**Master Clock Input** 1536 kHz signal must be applied for any operation. DCL, BCL, and FSC must be synchronous.	both
23	RESET#	I	**Reset Input** Forces the device to default setting mode; active low.	both
24	V_{DDD}	I	**Digital Supply Voltage** +5 V supply for digital circuits (use 100 nF blocking cap.).	both
25	NU		**None Usable** Leave unconnected.	
26	DU	I/O/ tri-state	**IOM-2 Data Upstream** Interface together with Pin 30. Both pins must be connected together. Transmits or receives PCM data in 8-bit bursts every 125 µs. With push-pull resistor.	both
27	DD	I/O/ tri-state	**IOM-2 Data Downstream** Interface together with Pin 29. Both pins must be connected together. Transmits or receives PCM data in 8-bit bursts every 125 µs. With push-pull resistor.	both
28	NU		**None Usable** Leave unconnected.	
29	DD	I/O/ tri-state	**IOM-2 Data Downstream** Interface together with Pin 27. Both pins must be connected together. Transmits or receives PCM data in 8-bit bursts every 125 µs. With push-pull resistor.	both
30	DU	I/O/ tri-state	**IOM-2 Data Upstream** Interface together with Pin 26. Both pins must be connected together. Transmits or receives PCM data in 8-bit bursts every 125 µs. With push-pull resistor.	both
31	FSC	I	**Frame Synchronization Clock** 8 kHz; reference for individual time slots, indicates start of PCM frame; DCL, BCL and FSC must be synchronous.	both
32	BCL	I	**IOM-2 Bit Clock** Determines rate at which PCM data is shifted into or out of PCM-ports. BCL, DCL, and FSC must be synchronous. If C-MODE = 0 in XR6, single clocking mode is used; 768 kHz must be applied to BCL. If C-MODE = 1 in XR6, double clocking mode is used; 1536 kHz must be applied to BCL. The data rate at the PCM ports remains 768 kbit/s.	both

Pin	Symbol	Type	Function	Ch.
33	RGEN	O	**Ring Generator Output** Configurable output clock (2 … 28 ms) synchronous to DCL. Square-wave signal with duty cycle 1:1.	both
34	INT12	O	**Interrupt Output, Channels 1 and 2** Active high.	both
35	SI1_1	I	**Signaling Input Channel 1, Pin 1**	1
36	SI1_0	I	**Signaling Input Channel 1, Pin 0**	1
37	SB1_2	I/O	**Bi-directional Signaling, Channel 1 Pin 2**	1
38	SB1_1	I/O	**Bi-directional Signaling, Channel 1 Pin 1**	1
39	SB1_0	I/O	**Bi-directional Signaling, Channel 1 Pin 0**	1
40	SO1_1	O	**Signaling Output, Channel 1, Pin 1**	1
41	SO1_0	O	**Signaling Output, Channel 1, Pin 0**	1
42	SO2_0	O	**Signaling Output, Channel 2, Pin 0**	2
43	SO2_1	O	**Signaling Output, Channel 2, Pin 1**	2
44	SB2_0	I/O	**Bi-directional Signaling, Channel 2 Pin 0**	2
45	SB2_1	I/O	**Bi-directional Signaling, Channel 2 Pin 1**	2
46	SB2_2	I/O	**Bi-directional Signaling, Channel 2 Pin 2**	2
47	SI2_0	I	**Signaling Input, Channel 2, Pin 0**	2
48	SI2_1	I	**Signaling Input, Channel 2, Pin 1**	2
49	V_{IN1}	I	**Analog Voice (Voltage) Input, Channel 1** Requires a coupling capacitor >39 nF to the SLIC.	1
50	GNDA1	I	**Analog Ground, Channel 1** Not internally connected to GNDD or GNDA2 or GNDA.	1
51	V_{OUT1}	O	**Analog Voice (Voltage) Output, Channel 1** Requires a coupling capacitor to the SLIC. The capacitor value depends on the SLIC's input impedance. (See **Chapter 5.1**, "Analog Interface" on page 25).	1
52	V_{DDA12}	I	**Analog Supply Voltage**, **Channels 1 and 2** +5 V (100 nF blocking capacitor required).	both
53	V_{OUT2}	O	**Analog Voice (Voltage) Output, Channel 2** Requires a coupling capacitor to the SLIC. The capacitor value depends on the SLIC's input impedance. (See **Chapter 5.1**, "Analog Interface" on page 25).	2

Pin	Symbol	Type	Function	Ch.
54	GNDA2	I	**Analog Ground, Channel 2** Not internally connected to GNDD or GNDA1 or GNDA.	2
55	V_{IN2}	I	**Analog Voice (Voltage) Input, Channel 2** Requires a coupling capacitor >39 nF to the SLIC.	2
56	V_{REF}	I/O	**Reference Voltage** Must connect to a 220 nF cap. to ground.	both
57	V_{DDREF}	I	**Analog Supply Reference Voltage** +5 V (100 nF blocking capacitor required).	both
58	NC		**Not Connected** Pin is not connected in this device.	
59	GNDA	I	**Analog Ground** Internally isolated from GNDD (Pin 21), GNDA1(Pin 50), and GNDA2 (Pin 54).	
60	NC		**Not Connected** Pin is not connected in this device.	
61	V_{DDA}	I	**Analog Supply Voltage** +5 V (100 nF blocking capacitor required).	
62	NC		**Not Connected** Pin not connected in this device.	
63	GNDA	I	**Analog Ground** Internally isolated from GNDD (Pin 21), GNDA1(Pin 50), and GNDA2 (Pin 54).	
64	NC		**Not Connected** Pin is not connected in this device.	

3 Functional Description

The SICOFI®2-TE in combination with four Subscriber Line Interface Circuits (SLIC) provides four analog telephone lines. The SLIC can be either a transformer or an electronic circuit with operational amplifiers. It must have a defined input impedance towards the analog line for maximum power transfer and return loss. Also, the signal reflections that are generated by the hybrid inside the SLIC must be eliminated. Along with its other features, the SICOFI®2-TE has built-in impedance matching and transhybrid balancing to perform these tasks.

3.1 DSP-based Architecture

The impedance matching and transhybrid balancing functions are performed by loop filters between the transmit path (analog to PCM) and the receive path (PCM to analog). The filter characteristics must be adjusted according to the local requirements of each market. In the analog domain, filters must be optimized in hardware; this is generally both tedious and time-consuming. This is not the case with the DSP-based SICOFI®2-TE two-channel codec. Its integrated signal processor implements the impedance matching and transhybrid balancing functions as digital, programmable filters. It also performs frequency response corrections and level adjustments to enable the design of a truly universal and internationally applicable telephone interface. Transmission characteristics and frequency behavior are enhanced by the accuracy of the digital filters, which do not fluctuate over temperature or with age.

As an additional benefit of its DSP-based architecture, the PSB 2132 also provides two tone generators per channel. An on-chip level-metering unit allows line-characterization without extra hardware; it can also be used to detect specific tones, e.g., modem tones.

3.2 Programming and Control

A very simple Microcontroller Interface is used to program the SICOFI®2-TE functions. The same port provides access to 14 general purpose I/O pins of the Signaling Interface. This allows efficient and convenient monitoring and control of other tip/ring functions, such as on-/off-hook detection, ground-key detection, switching of ring signals and test relays. The Serial Microcontroller Interface provides a programming and control interface and is generic and non-proprietary for use with any microcontroller. It can be implemented with as few as three signal lines, since the data receive and data transmit pins may be strapped together.

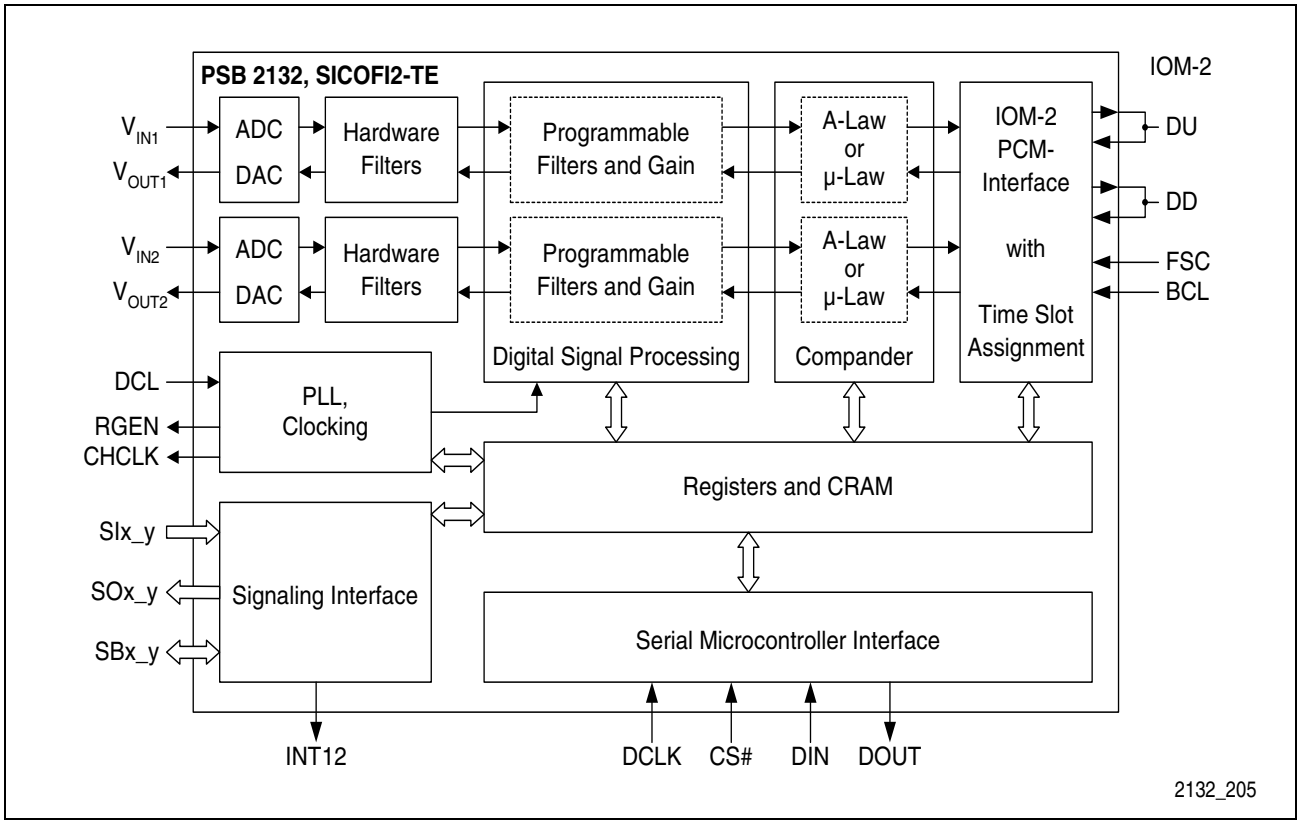


Figure 4 SICOFI®2-TE Block Diagram

Figure 4 shows the functional blocks and the interface pins of the SICOFI®2-TE:

- Two independent bi-directional voice channels;
- Oversampling sigma-delta A/D and D/A converters with excellent resolution, dynamic range, linearity, accuracy and signal-to-noise performance;
- Hardware filters for decimation and interpolation of the ADC and DAC bit stream, and pre-processing of the voice data to reduce the load of the DSP;
- DSP core with programmable, channel-independent filter structures for impedance matching, transhybrid balancing, frequency correction and level adjustments;
- Configurable A-Law or µ-Law compressor and expander units;
- An IOM-2 PCM interface with time slot assignment, one input and one output connected to DU, and one input and one output connected to DD;
- Three clock inputs, DCL, BCL, and FSC also apply to the IOM-2 PCM Interface;
- 14 signaling input and output pins, accessible through registers;
- Two interrupt outputs, one for each channel-pair 1&2, and 3&4;
- One interrupt output;
- On-chip PLL for an internal 16,384 kHz clock;
- Eight common configuration registers (XR-Registers) affecting both channels;
- Two sets of six channel-specific registers (CR-Registers);
- Coefficient RAM (CRAM) for filter coefficients storage for each channel;
- The Serial Microcontroller Interface has four signals: DIN, DOUT, DCLK, and CS#.

4 Operational Description

Each channel of the SICOFI®2-TE can be in one of two stable states: “Standby” and “Operating”. These states can be switched by programming Bit 0 (PU) in the channel-specific configuration register CR1. “Standby” is a power-saving state. Keeping any unused channels in this state reduces the overall system power dissipation. The third state, “Reset”, is transient and is reached after applying power to the device (Power On), after asserting a logic low signal to the RESET#-pin (HW-Reset), or after issuing an XOP command with Bit 7 (RST) set to "1" (SW-Reset). Both channels would be affected in any case.

4.1 Operating States

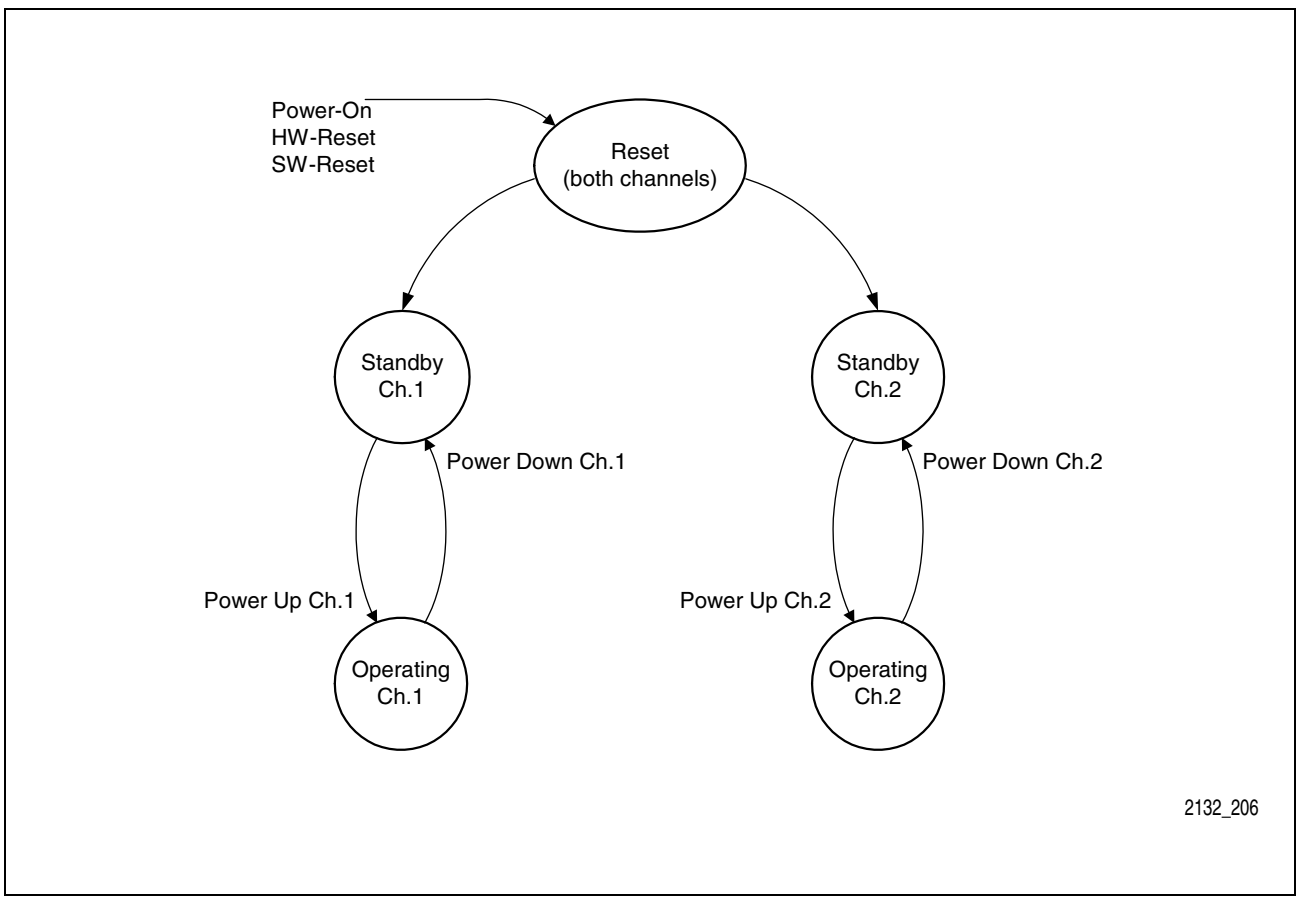


Figure 5 SICOFI®2-TE State Diagram

4.1.1 Power On

All input pins must be at GND level before applying VDD to the SICOFI®2-TE. Otherwise, the device may not enter the Reset State. In this case, the SICOFI®2-TE can be reset by HW- or SW-Reset, or can be initialized by setting all registers to zero.

4.1.2 Hardware Reset

Voltage levels lower than 1.2 V applied to Pin 23 (RESET#) for more than 3 µs will reset the SICOFI®2-TE. Spikes that are shorter than 1 µs will be ignored. When RESET# is released the SICOFI®2-TE will enter Standby State.

Table 2 Register Values and Accessibility

Register	SICOFI®2-TE State		
	Reset	Standby	Operating
CR0...CR4	00_H	user configurable	user configurable
XR0...XR7	00_H	user configurable	user configurable
CRAM	unchanged	user configurable	user configurable

Table 3 Input and Output Pin Behavior

Pin	SICOFI®2-TE State		
	Reset	Standby	Operating
DIN	ignored	serial input	serial input
DOUT	high impedance	serial output	serial output
DU, DD	inactive	inactive	receiving/transmitting PCM data during programmed time slot
V_{OUT1} , V_{OUT2}	high impedance	high impedance	analog output
V_{IN1} , V_{IN2}	ignored	ignored	analog input
SBx_y	configured as input	programmable as input or output	programmable as input or output
SOx_y	GNDD	digital output	digital output
SIx_y	ignored	digital input	digital input
RGEN	high	programmable frequency	programmable frequency
CHCLK	high	programmable freq. (not 16,384 kHz)	programmable frequency

Note: The 1536 kHz DCL clock must be applied for all device functions.

Table 4 Power Dissipation

No. of Channels Operating	Typical Power Dissipation
None	2.5 mW
1	70 mW
2	90 mW

4.2 Transmission Characteristics

4.2.1 Overload Point

The overload point of the SICOFI®2-TE A/D converters is at 2.223 V. This is the peak amplitude of a sine wave level of 1.572 Vrms. Higher input signal levels will be distorted. Theoretical load capacities for A-Law and µ-Law encoded signals are defined in ITU-T Recommendation G.711. These values correspond to the SICOFI®2-TE overload point:

Table 5 Maximum Signal Levels

Encoding Law	IOM-2 PCM Interface	Analog Interface
	Theoretical Load Capacity (according to ITU-T G.711)	Max. Sine Wave Level (SICOFI®2-TE Overload Point)
A-Law	3.14 dBm0	1.572 Vrms
µ-Law	3.17 dBm0	

4.2.2 0 dBm0-Levels

The analog voltage levels corresponding to a 0 dBm0 sine wave signal can be calculated from the maximum signal levels shown in **Table 5**. The results are shown in **Table 6**.

Table 6 Analog Voltage Levels Corresponding to 0 dBm0-Level

Encoding Law	Analog Sine Wave Level corresponding to 0 dBm0 PCM Level
A-Law	1.572 Vrms*10^(-3.14/20) = 1.095 V rms
µ-Law	1.572 Vrms*10^(-3.17/20) = 1.091 V rms

Note: Periodic PCM codes for a 1 kHz sine wave signal with 0 dBm0 level can be found in ITU-T G.711.

4.2.3 Compressor Gain Relative to Coding Law

The **µ-Law** compressor unit of the SICOFI®2-TE automatically adds 1.94 dBm0 gain, which has to be considered for the total gain calculation. The accumulated gain of all programmable transmit filters (AX1+AX2+FRX) must not exceed 6 dB if the device is set to µ-Law operation. If the device is set to A-Law operation, then the accumulated gain must not exceed 8 dB.

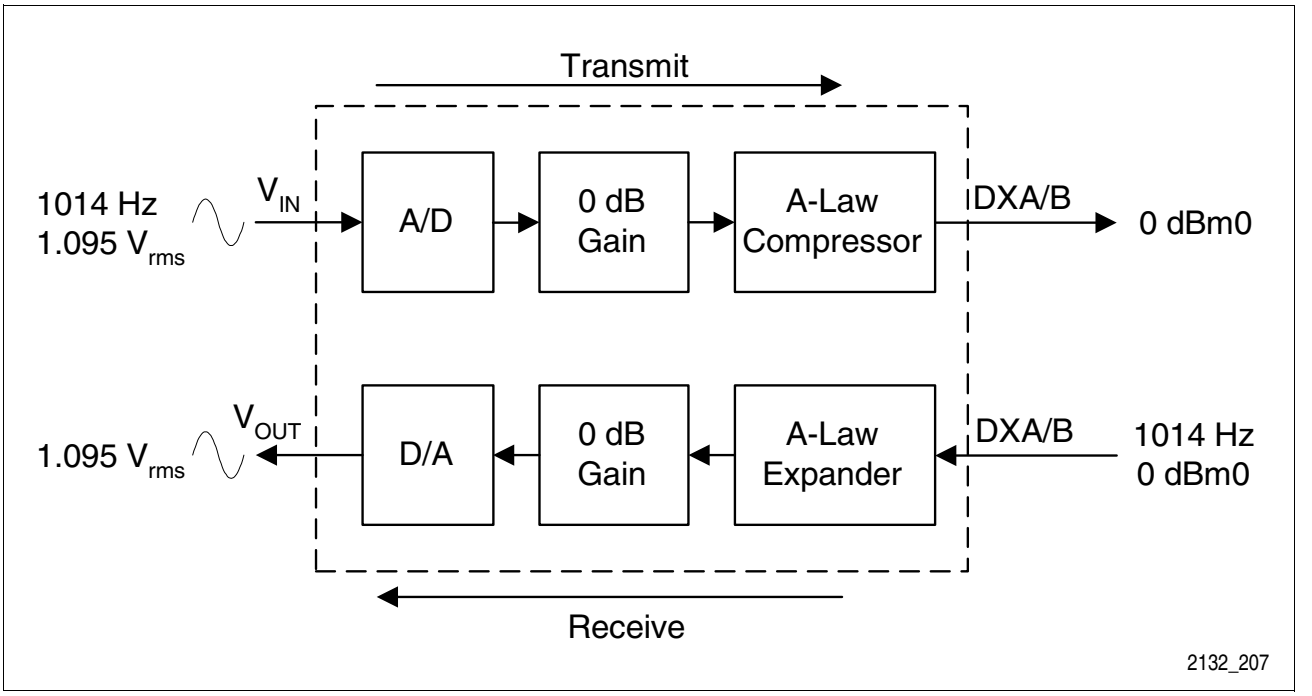


Figure 6 Analog and PCM Signal Levels in A-Law Mode

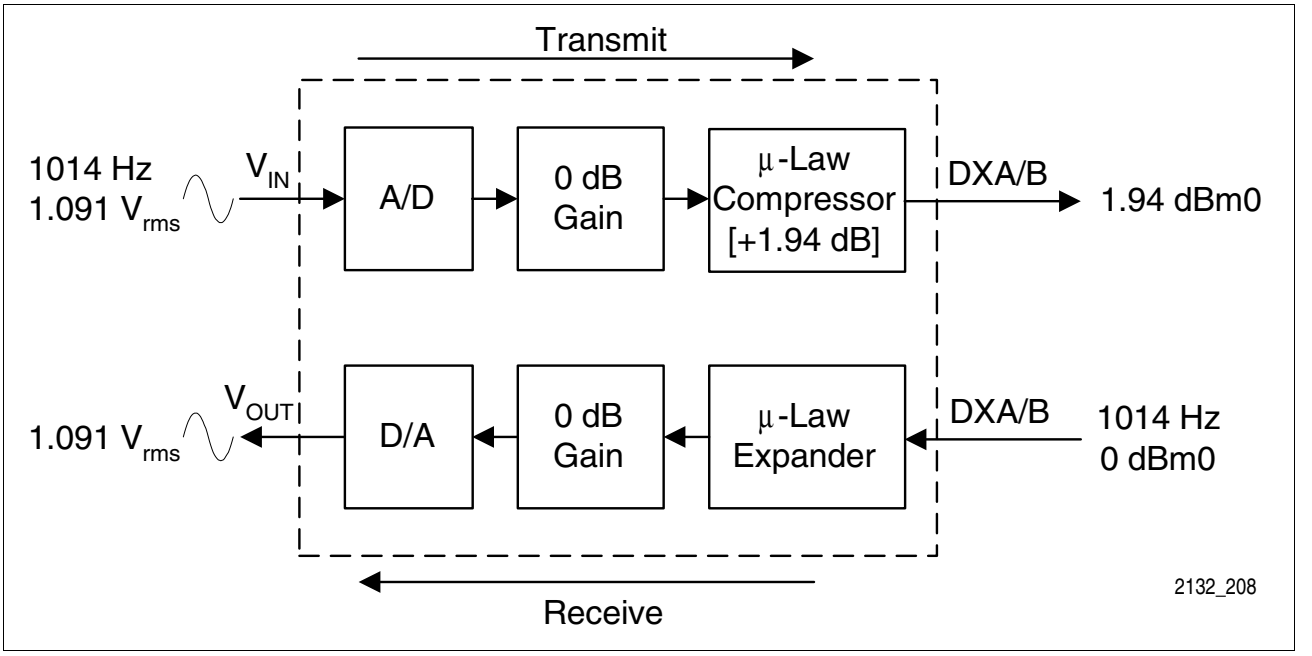


Figure 7 Analog and PCM Signal Levels in µ-Law Mode

4.2.4 Operating Conditions

The figures in this document are based on the subscriber-line board requirements. Proper adjustment of the programmable filters (transhybrid balancing, impedance matching, frequency-response correction) requires a complete knowledge of the analog environment in which the SICOFI®2-TE is to be used. Unless otherwise stated, the transmission characteristics are guaranteed within the following operating conditions:

- T_A = 0 °C to 70 °C;
- V_{DD} = 5 V ± 5%;
- GNDA1,2,3,4 = GNDD = 0 V;
- Load on V_{OUT}: R_L > 300 Ω; C_L < 50 pF;
- H(IM) = H(TH) = 0;
- H(R1) = H(FRX) = H(FRR) = 1;
- HPR and HPX enabled;
- AR = 0 to –8 dB (AR = AR1 + AR2 + FRR + R1);
- AX = 0 to +8 dB for A-Law,
  AX = 0 to +6 dB for µ-Law (AX = AX1 + AX2 + FRX);
- f = 1014 Hz; 0 dBm0; A-Law or µ-Law;
- AGX = 0 dB, +6.02 dB; and
- AGR = 0 dB, –6.02 dB.

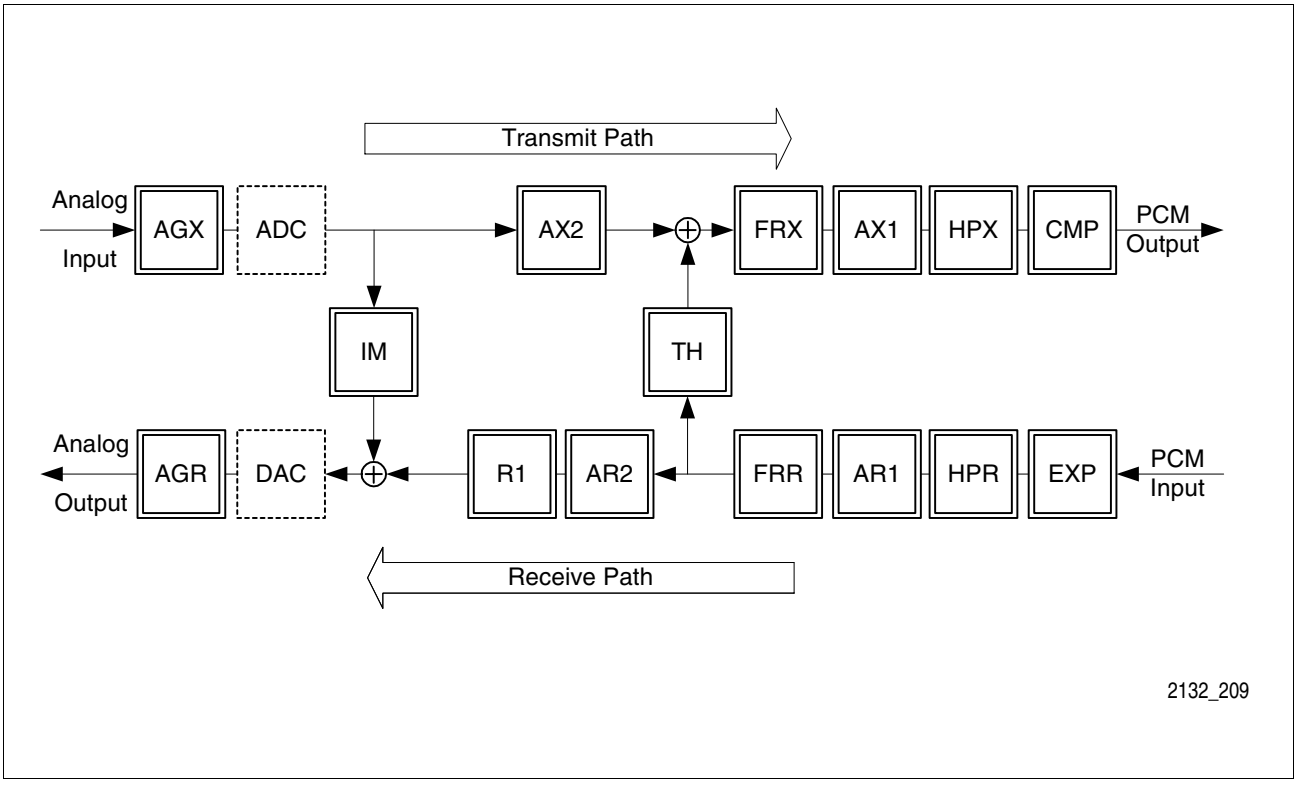


Figure 8 Simplified Signal Flow Diagram