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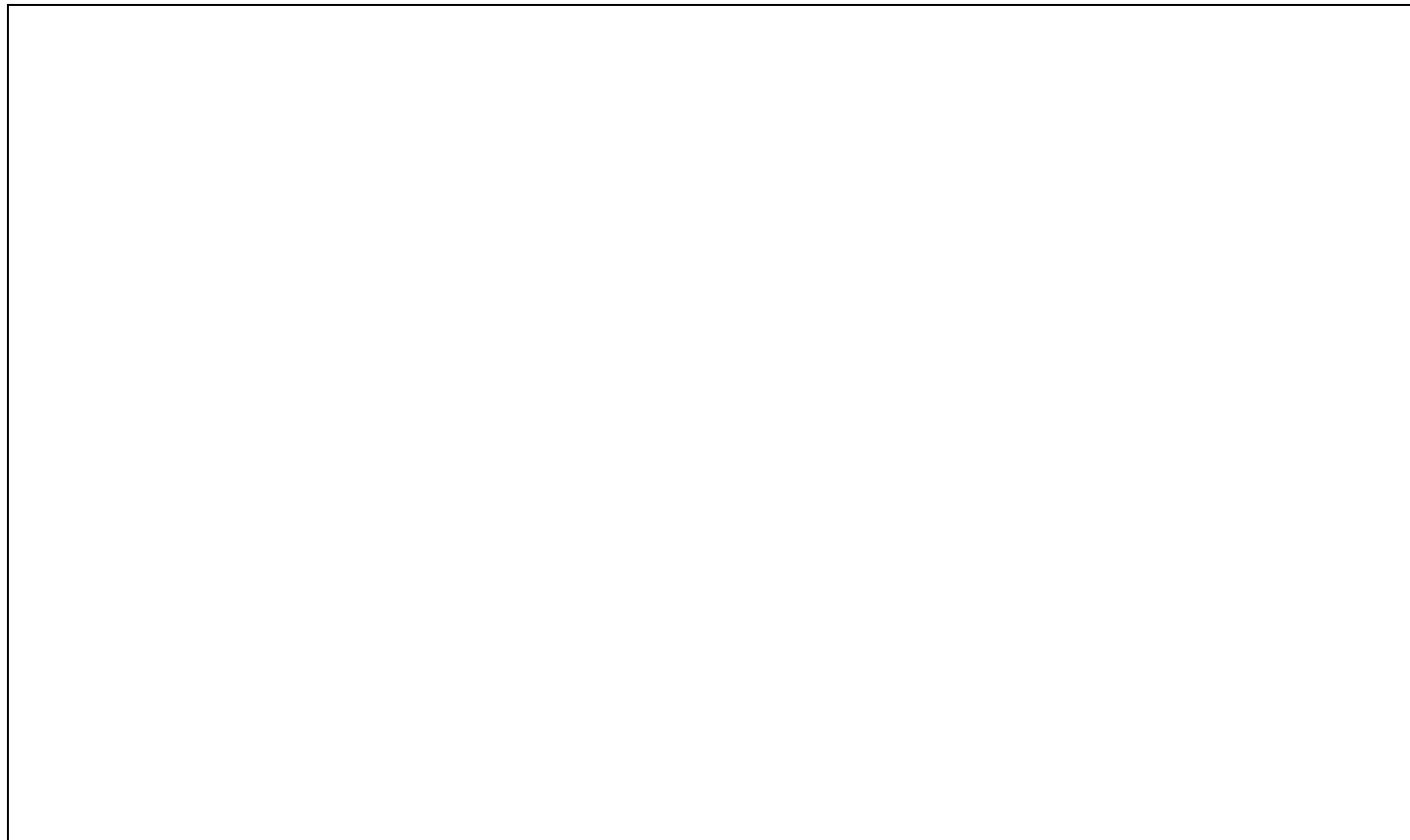
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SIEMENS

ICs for Communications

Two Channel Codec Filter for Terminal Applications
SICOFI®2-TE

PSB 2132 Version 1.2

Four Channel Codec Filter for Terminal Applications
SICOFI®4-TE

PSB 2134 Version 1.2

Data Sheet   09.97

PSB 2132		
Revision History:		**Current Version: 09.97**
Previous Version:		Preliminary Data Sheet 02.97
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
		Feature list updated

IOM®, IOM®-1, IOM®-2, SICOFI®, SICOFI®-2, SICOFI®-4, SICOFI®-4µC, SLICOFI®, ARCOFI® , ARCOFI®-BA, ARCOFI®-SP, EPIC®-1, EPIC®-S, ELIC®, IPAT®-2, ITAC®, ISAC®-S, ISAC®-S TE, ISAC®-P, ISAC®-P TE, IDEC®, SICAT®, OCTAT®-P, QUAT®-S are registered trademarks of Siemens AG.

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1 Overview

The Signal Processing Codec Filter for terminal applications PSB 2132/4 SICOFI2/4-TE is a special derivative of the SIEMENS programmable codec-filter-IC family designed for terminal applications featuring two or four POTS interfaces.

It can be directly connected to the IOM-2 interface in terminal mode running at 1.536 MHz clock rate. PCM data is transfered using the bit clock signal at 768 kHz.

Programming of internal registers is done via the serial microcontroller interface.

Only two external capacitors per channel are needed to complete the functionality of the PSB 2132/4. The internal level accuracy is based on a very accurate bandgap reference. The frequency behaviour is mainly determined by digital filters, which do not have any fluctuations. As a result of the new ADC- and DAC- concepts linearity is only limited by second order parasitic effects. Although the device works only from one single 5 V supply there is a very good dynamic range available.

The PSB 2132/4 is a DSP based codec which allows the integration of filters and tone generators besides the regular A- or u-law conversion. In addition it integrates I/O extentions to the microcontroller and provides the necessary I/O pins to control the SLIC or discrete SLIC replacement. Interrupts are generated to the microcontroller if changes (e.g. Off-Hook detection) have been occured. The PSB 2132/4 provides a ring frequency output pin. This pin has a programmable clock frequency to meet the European and US ringing frequency requirements using only one external divider.

The IOM-2 data lines DU and DD can both be used for transmitting or receiving voice data. The position of each receive and transmit timeslot is programmable. Internal communication between analog ports is supported by programming each channel to the same timeslot but reversing the data lines. Thus the transmitted PCM data is transmitted by one port and received by the second port via the same timeslot. An additional IC for switch matrix is eliminated.

The PSB 2132/4 is specially of interest for applications, which need to serve different country specific characteristics on the POTS interface. Since all filters are programmable, adaptation to these country specific requirements may be done only by software parameters using the same hardware.

SIEMENS

Two Channel Codec Filter for Terminal Applications SICOFI®2-TE **PSB 2132**

Four Channel Codec Filter for Terminal Applications SICOFI®4-TE **PSB 2134**

Preliminary Data **CMOS**

1.1 Features

- Single chip programmable CODEC and FILTER to handle two or four POTS interfaces
- IOM-2 compatible interface (1.536 MHz DCL, 768 kHz Bit clock)
- Internal communication between POTS interfaces
- Programmable I/O lines for signaling information per channel
- Programmable ring generator output
- Two programmable tone generators per channel
- Serial microcontroller interface
- Digital signal processing technique
- High analog driving capability (300 Ω) for direct driving of transformers

- Programmable digital filters to adapt the transmission behaviour especially for
    - AC impedance matching
    - transhybrid balancing
    - frequency response
    - gain
    - A/μ-law conversion
- Single 5 V power supply
- Low power 0.9 μm analog CMOS technology
- Advanced test capabilities
- P-MQFP-64 package

P-MQFP-64
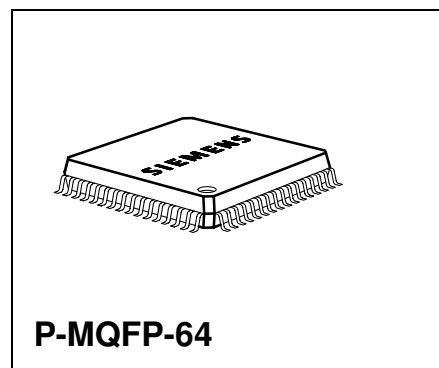
1.2 Pin Configuration

(top view)
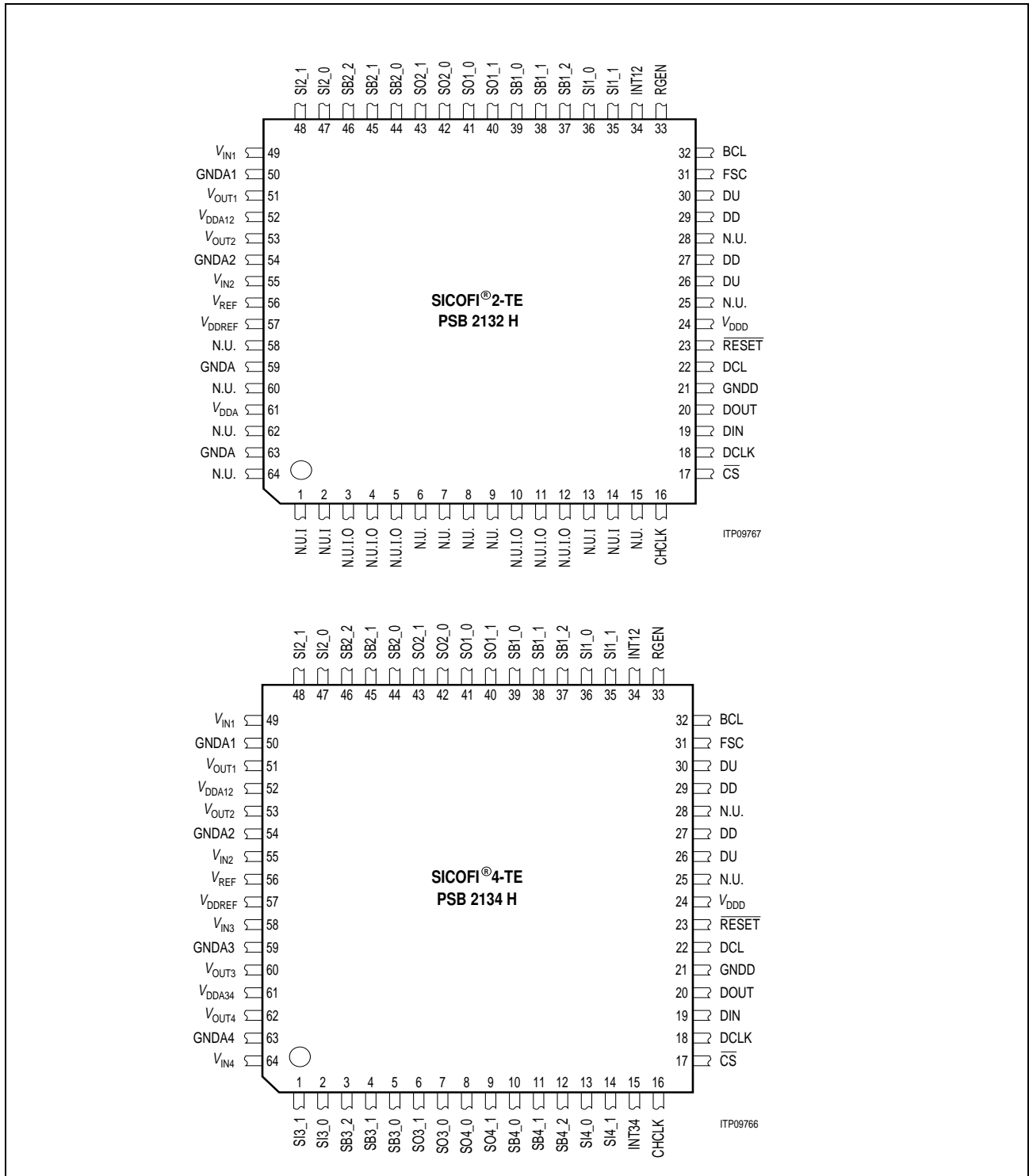
Figure 1

1.3   Pin Definition and Functions

Pin No.	Symbol	Input (I) Output (O)	Function

Common Pins for all Channels

Pin No.	Symbol	Input (I) Output (O)	Function
24	V_{DDD}	I	+ 5 V supply for the digital circuitry [1]
21	GNDD	I	Ground Digital, not internally connected to GNDA1,2,(3,4) All digital signals are referred to this pin
52	V_{DDA12}	I	+ 5 V Analog supply voltage for channel 1 and 2 [1]
56	V_{REF}	I/O	Reference voltage, has to be connected to a 220 nF cap. to ground, can also be used as virtual ground for analog inputs and outputs (high-ohmic buffer needed !!!)
57	V_{DDREF}	I	+ 5 V Analog supply voltage (100 nF cap. required)
31	FSC	I	Frame synchronization clock, 8 kHz, identifies the beginning of the frame, individual time slots are referenced to this pin, FSC must be synchronous to DCL and BCL
32	BCL	I	IOM-2 bit clock 768 kHz, determines the rate at which PCM data is shifted into or out of the PCM-ports
26,30	DU	I/O	IOM-2 Data Upstream interface. Transmits or receives PCM data in 8 bit bursts. Both pins must be connected together.
27,29	DD	I/O	IOM-2 Data Downstream interface. Transmits or receives PCM data in 8 bit bursts. Both pins must be connected together.
23	$\overline{RESET}$	I	Reset input - forces the device to default mode, active low
22	DCL	I	Master clock input 1536 kHz, synchronous to FSC, must be available if the SICOFI2/4-TE is operating
17	$\overline{CS}$	I	μ-Controller interface: chip select enable to read or write data, active low
18	DCLK	I	μ-Controller interface: data clock, shifts data from or to device, the maximum clock rate is 8192 kHz

Pin No.	Symbol	Input (I) Output (O)	Function
19	DIN	I	μ-Controller interface: control data input pin, DCLK determines the data rate
20	DOUT	O	μ-Controller interface: control data output pin, DCLK determines the data rate, DOUT is high 'Z' if no data is transmitted from the SICOFI2/4-TE
33	RGEN	O	Ring generator output, provides a programmable (2 … 28 ms) output signal (synchronous to DCL)
16	CHCLK2	O	Chopper Clock output, provides a 256, or 512 or 16384 kHz signal, is synchronous to DCL
34	INT12	O	Interrupt output pin for channel 1 and 2, active high
Dedicated pins for PSB 2132			
61	V_{DDA}	I	+ 5 V Analog supply voltage [1]
59,63	GNDA	I	Ground analog for unused analog I/O pins
1,2,13, 14	N.U.I	I	None usable input, tie directly to GNDD
3,4,5, 10,11, 12	N.U.I.O	I/O	None usable input/output, tie via a pull-down-resistor to GNDD.
6,7,8,9, 15,25, 28,58, 60,62, 64	N.U.		None usable, leave unconnected
Dedicated pins for PSB 2134			
61	V_{DDA34}	I	+ 5 V Analog supply voltage for channel 3 and 4[1]
15	INT34	O	Interrupt output pin for channel 3 and 4, active high

Pin No.	Symbol	Input (I) Output (O)	Function

Specific Pins for Channel 1

Pin No.	Symbol	Input (I) Output (O)	Function
50	GNDA1	I	Ground Analog for channel 1, not internally connected to GNDD or GNDA2,3,4
49	V_{IN1}	I	Analog voice (voltage) input for channel 1, has to be connected to the SLIC by a 39 nF cap.
51	V_{OUT1}	O	Analog voice (voltage) output for channel 1, has to be connected to the SLIC via a cap. [2]
36	SI1_0	I	Signaling input pin 0 for channel 1
35	SI1_1	I	Signaling input pin 1 for channel 1
41	SO1_0	O	Signaling output pin 0 for channel 1
40	SO1_1	O	Signaling output pin 1 for channel 1
39	SB1_0	I/O	Bi-directional signaling pin 0 for channel 1
38	SB1_1	I/O	Bi-directional signaling pin 1 for channel 1
37	SB1_2	I/O	Bi-directional signaling pin 2 for channel 1

Specific Pins for Channel 2

Pin No.	Symbol	Input (I) Output (O)	Function
54	GNDA2	I	Ground Analog for channel 2, not internally connected to GNDD or GNDA 1,3,4
55	V_{IN2}	I	Analog voice (voltage) input for channel 2, has to be connected to the SLIC by a 39 nF cap.
53	V_{OUT2}	O	Analog voice (voltage) output for channel 2, has to be connected to the SLIC via a cap. [2]
47	SI2_0	I	Signaling input pin 0 for channel 2
48	SI2_1	I	Signaling input pin 1 for channel 2
42	SO2_0	O	Signaling output pin 0 for channel 2
43	SO2_1	O	Signaling output pin 1 for channel 2
44	SB2_0	I/O	Bi-directional signaling pin 0 for channel 2
45	SB2_1	I/O	Bi-directional signaling pin 1 for channel 2
46	SB2_2	I/O	Bi-directional signaling pin 2 for channel 2

Pin No.	Symbol	Input (I) Output (O)	Function

Specific Pins for Channel 3 (PSB 2134 only)

Pin No.	Symbol	Input (I) Output (O)	Function
59	GNDA3	I	Ground Analog for channel 3, not internally connected to GNDD or GNDA1,2,4
58	V_{IN3}	I	Analog voice (voltage) input for channel 3, has to be connected to the SLIC by a 39 nF cap.
60	V_{OUT3}	O	Analog voice (voltage) output for channel 3, has to be connected to the SLIC via a cap. [2]
2	SI3_0	I	Signaling input pin 0 for channel 3
1	SI3_1	I	Signaling input pin 1 for channel 3
7	SO3_0	O	Signaling output pin 0 for channel 3
6	SO3_1	O	Signaling output pin 1 for channel 3
5	SB3_0	I/O	Bi-directional signaling pin 0 for channel 3
4	SB3_1	I/O	Bi-directional signaling pin 1 for channel 3
3	SB3_2	I/O	Bi-directional signaling pin 2 for channel 3

Pin No.	Symbol	Input (I) Output (O)	Function

Specific Pins for Channel 4 (PSB 2134 only)

Pin No.	Symbol	Input (I) Output (O)	Function
63	GNDA4	I	Ground Analog for channel 4, not internally connected to GNDD or GNDA1,2,3
64	V_{IN4}	I	Analog voice (voltage) input for channel 4, has to be connected to the SLIC by a 39 nF cap.
62	V_{OUT4}	O	Analog voice (voltage) output for channel 4, has to be connected to the SLIC via a cap. [2]
13	SI4_0	I	Signaling input pin 0 for channel 4
14	SI4_1	I	Signaling input pin 1 for channel 4
8	SO4_0	O	Signaling output pin 0 for channel 4
9	SO4_1	O	Signaling output pin 1 for channel 4
10	SB4_0	I/O	Bi-directional signaling pin 0 for channel 4
11	SB4_1	I/O	Bi-directional signaling pin 1 for channel 4
12	SB4_2	I/O	Bi-directional signaling pin 2 for channel 4

[1] A 100 nF cap. should be used for blocking these pins, see also on page 83

[2] The value for the capacitor needed, depends on the input impedance of the 'SLIC'-circuitry. For choosing the appropriate values see figure on page 72.

2 Functional Description

2.1 System Integration

The SICOFI2/4-TE is connected to an IOM-2 compatible transceiver such as the PEB 8191 INTC-Q for U-interface or NT-applications or the PSB 2186 ISAC-S TE or PSB 2115 IPAC for S/T-interface applications. The FSC output is connected to the FSC input on the SICOFI2/4-TE. The DCL output of the transceiver is fed to the DCL input of the SICOFI2/4-TE which is used as master clock. For transferring PCM data, the bit clock signal of the transceiver (BCL, 768 kHz) is connected to the SICOFI2/4-TE.
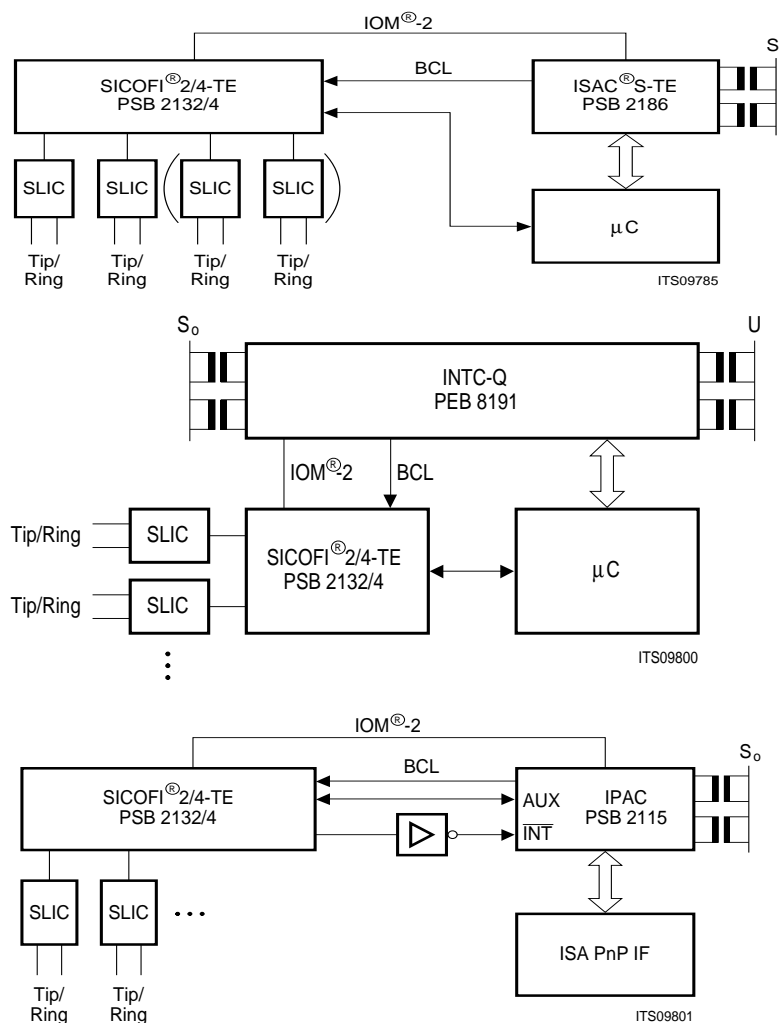

Figure 2

The microcontroller interface is connected to a microcontroller. Since the data transfer does not require duplex operation it can be connected both to SPI compatible microcontrollers (Siemens C5xx series, C161 series) as well as to Intel C51 based ones.

The SICOFI2/4-TE provides an high active interrupt output. The interrupts are caused by changes on the input lines of each channel. In order to operate it is necessary to keep DCL running all the time. If DCL is stopped in order to reduce the power consumption of the system, additional hardware is required. This hardware may be used to generate directly an interrupt to the microcontroller which may than request IOM-clocking.

Each channel serves seven I/O lines (2xO, 2xI, 3xI/O) which are used to control the inputs of the SLIC or to fed the outputs of a SLIC to the microcontroller.

The RGEN output can be used to generate the input signal of a ringing SLIC. Its frequency is programmable down to 35,7 Hz.

2.2 SICOFI®2/4-TE Principles

The SICOFI2/4-TE is designed for terminal adapters and Intelligent NT (NT1plus) applications.

It is designed to reduce the number of external components required for the integrated or discrete SLIC.

The SICOFI-2/4 TE bridges the gap between analog and digital voice signal transmission in modern telecommunication systems. High performance oversampling Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) provide the conversion accuracy required. Analog antialiasing prefilters (PREFI) and smoothing postfilters (POFI) are included. The connection between the ADC and the DAC (with high sampling rate) and the DSP, is done by specific Hardware Filters, for filtering like interpolation and decimation. The dedicated Digital Signal Processor (DSP) handles all the algorithms necessary e.g. for PCM bandpass filtering, sample rate conversion and PCM companding. The PCM-interface handles digital voice transmission, a serial µC-interface handles SICOFI2/4-TE feature control and transparent access to the SICOFI2/4-TE command and indication pins. To program the filters, precalculated sets of coefficients are downloaded from the system to the on-chip Coefficient-RAM (CRAM).
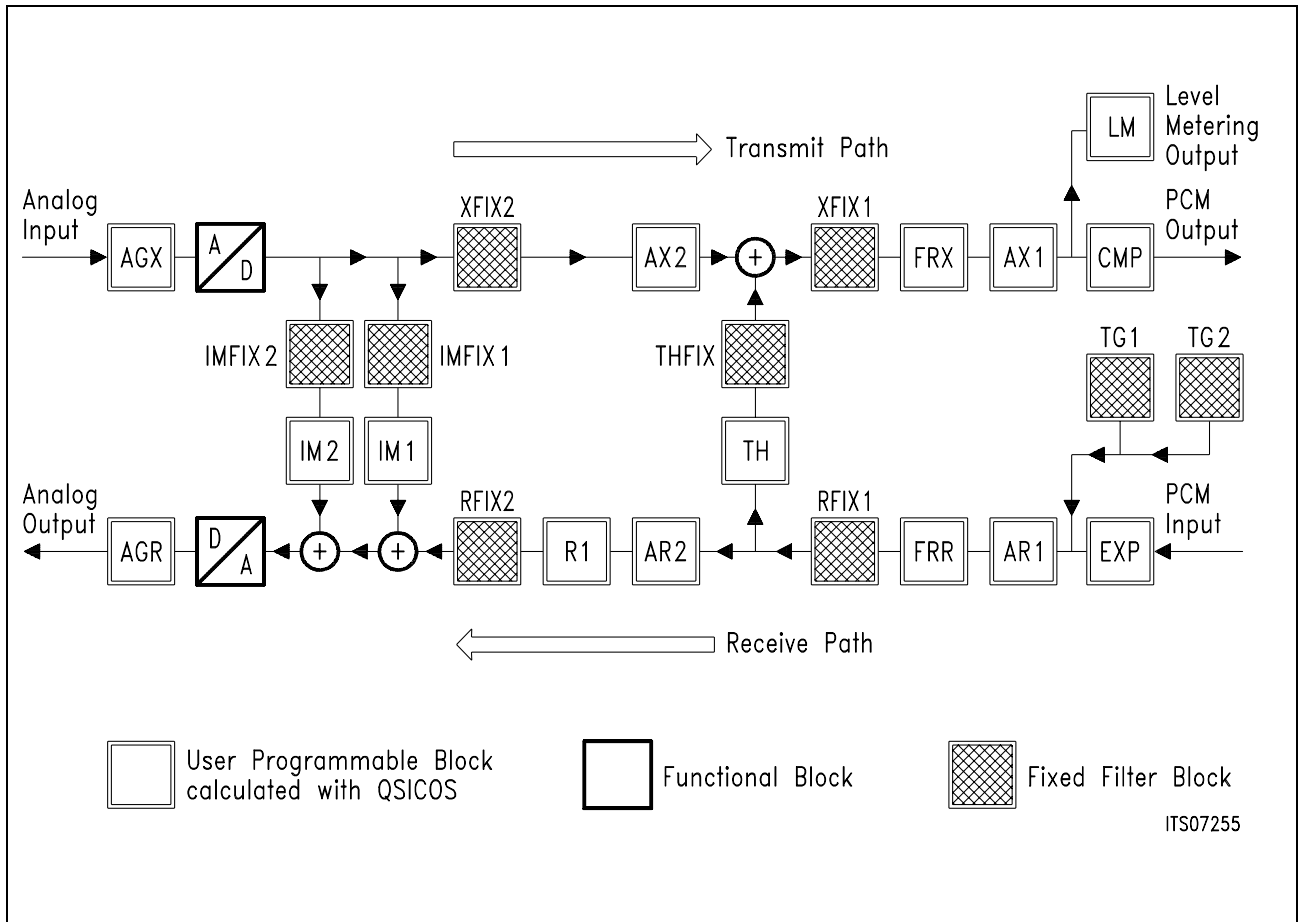
Figure 3
SICOFI®2/4-TE Signal Flow Graph (for any channel)

Transmit Path

The analog input signal has to be DC-free connected by an external capacitor because there is an internal virtual reference ground potential. After passing a simple antialiasing prefilter (PREFI) the voice signal is converted to a 1-bit digital data stream in the Sigma-Delta-converter. The first downsampling steps are done in fast running digital hardware filters. The following steps are implemented in the micro-code which has to be executed by the central Digital Signal Processor. This DSP-machine is able to handle the workload for all four channels. At the end the fully processed signal (flexibly programmed in many parameters) is transferred to the PCM- interface in a PCM-compressed signal representation.

Receive Path

The digital input signal is received via the PCM interface. Expansion, PCM-Law-pass-filtering, gain correction and frequency response correction are the next steps which are done by the DSP-machine. The upsampling interpolation steps are again processed by fast hardware structures to reduce the DSP-workload. The

upsampled 1-bit data stream is then converted to an analog equivalent which is smoothed by a POST-Filter (POFI). As the signal V_{OUT} is also referenced to an internal virtual ground potential, an external capacitor is required for DC-decoupling.

Loops

There are two loops implemented. The first is to generate the AC-input impedance (IM) and the second is to perform a proper hybrid balancing (TH). A simple extra path IM2 (from the transmit to the receive path) supports the impedance matching function.

Test Features

There are four analog and five digital test loops implemented in the SICOFI-2/4 TE. For special tests it is possible to cut off the receive and the transmit path at two different points. In addition, external test loops including the subscriber line measurement are possible using the level meatering feature.
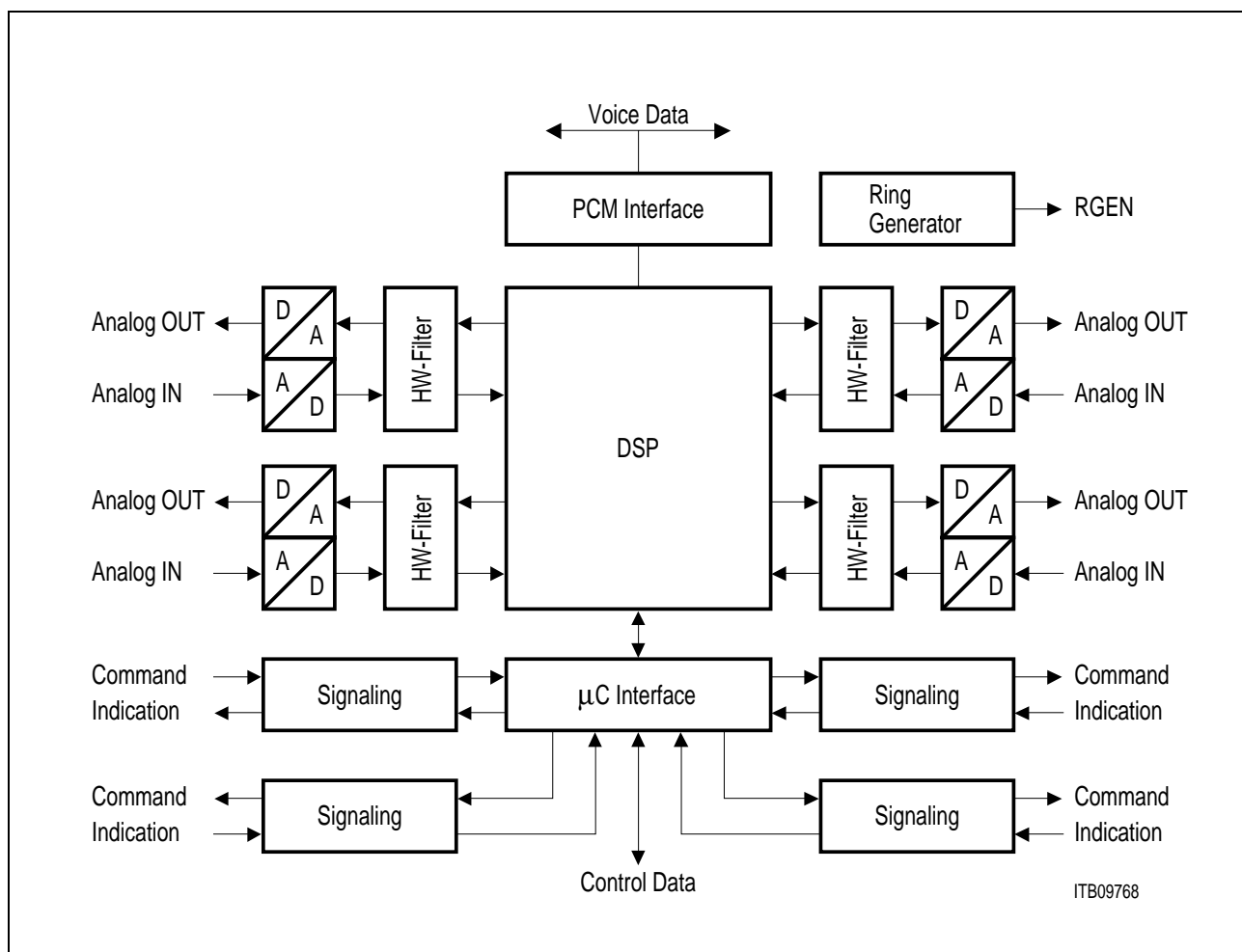

Figure 4
SICOFI2/4®-TE Block Diagram

2.3   The IOM-2 PCM-interface

One serial PCM-interface is used for transfer of A- or µ-law compressed voice data. The PCM-interface consists of 4 pins:

BCL: IOM-2 bit clock, 768 kHz

FSC: Frame Synchronization Clock, 8 kHz

DU: Data transmit or receive in data upstream direction

DD: Data receive or transmit in data downstream direction

The Frame Sync FSC pulse identifies the beginning of a receive and transmit frame for all of the two / four channels. The BCL clock is the signal to synchronize the data transfer on both lines DU and DD. Bytes in all channels are serialized to 8 bit width and MSB first. As a default setting, the rising edge indicates the start of the bit, while the falling edge is used to latch the contents of the received data.

The data rate of the interface is fixed to 768 kHz. A frame consists of 12 time slots of 8 bits each. In the Time Slot Configuration Registers CR5 and CR6 the user can select an individual time slot, and one of two data lines, for any of the voice channels. Receive and transmit time slots can also be programmed individually. An extra delay of up to 7 clocks, valid for all channels, as well as the sampling slope may be programmed (see XR6).
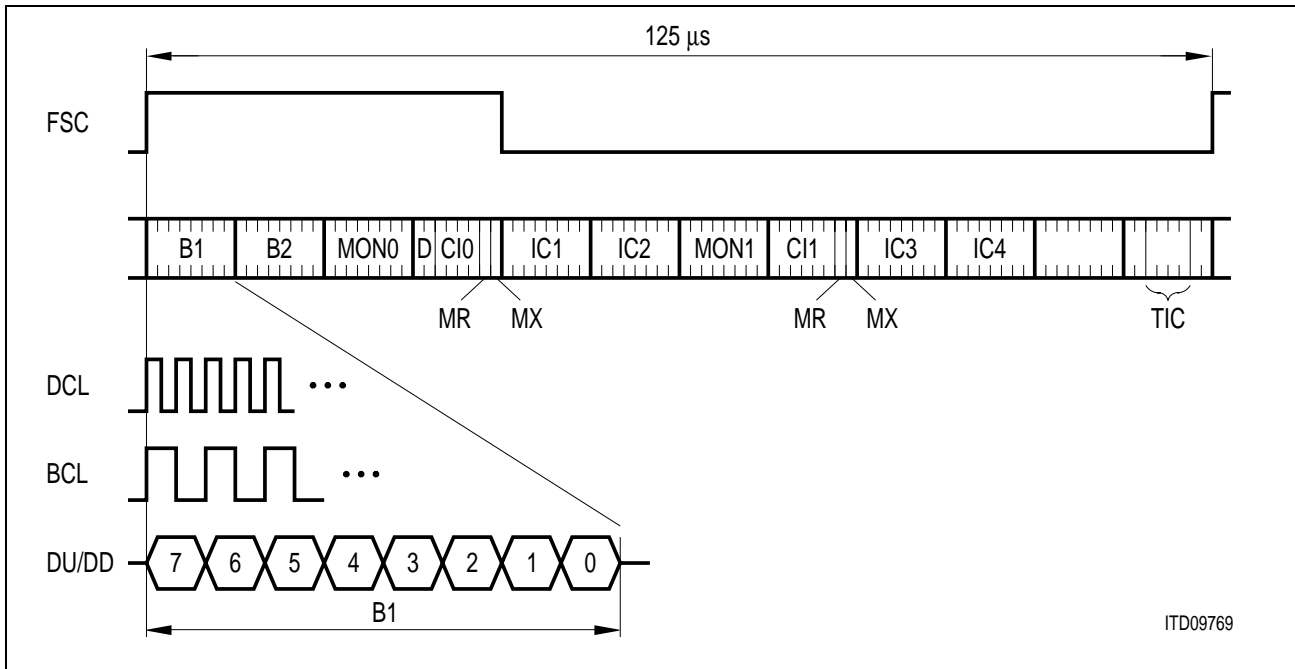
A typical example is shown below.

Figure 5
Example for IOM-2 Terminal Mode

2.4 The μ-Controller Interface

The internal configuration registers, the signaling interface, and the Coefficient-RAM (CRAM) of the SICOFI-2/4-TE are programmable via a serial μ-Controller interface.

The μ-Controller interface consists of four lines: $\overline{CS}$, DCLK, DIN and DOUT:

$\overline{CS}$ is used to start a serial access to the SICOFI-2/4-TE registers and Coefficient-RAM. Following a falling edge of CS, the first eight bits received on DIN specify the command. Subsequent data bytes (number depends on command) are stored in the selected configuration registers or the selected part of the Coefficient-RAM.
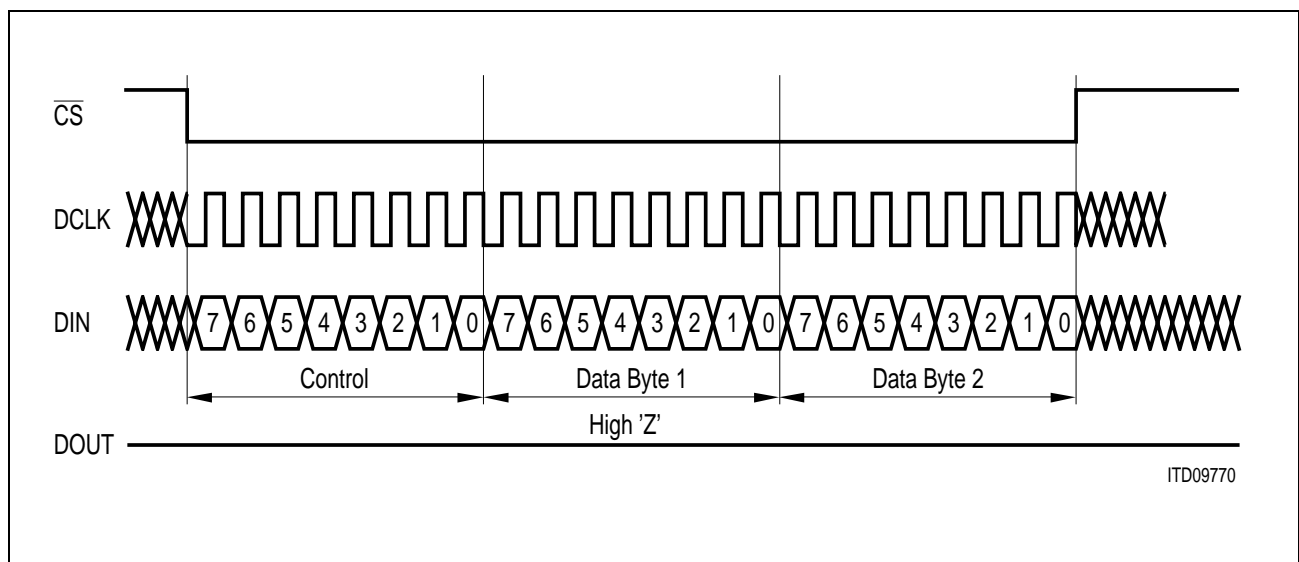

Figure 6
Example for a Write Access, with Two Data Bytes Transferred

If the first eight bits received via DIN specify a read-command, the SICOFI-2/4 TE will start a response via DOUT with its specific address byte (81_H). After transmitting this identification, the specified n data bytes (contents of configuration registers, or contents of the CRAM) will follow on DOUT.
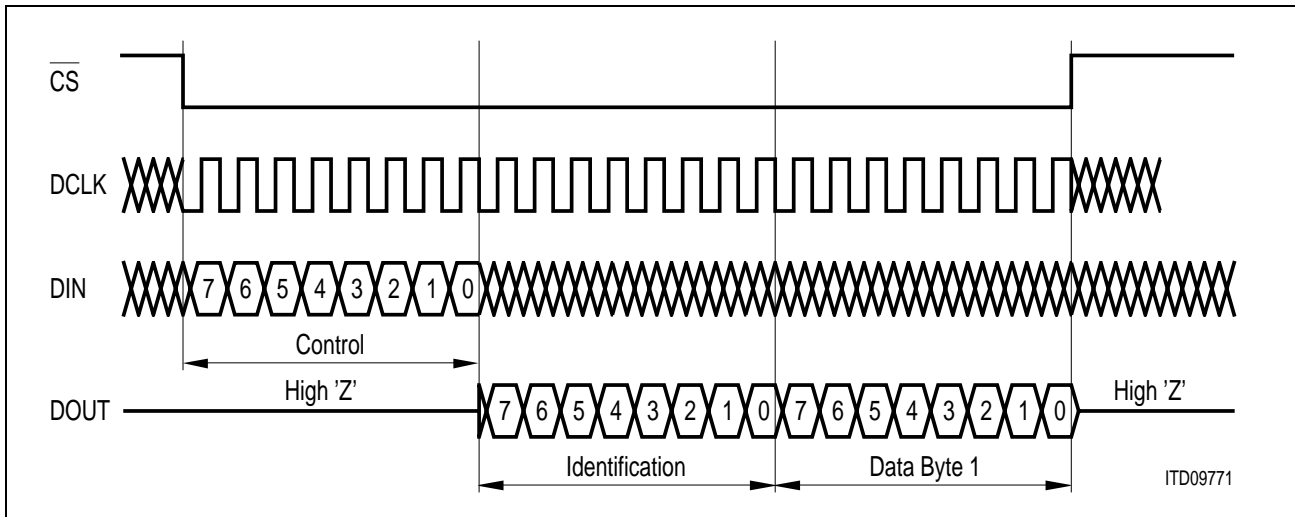
Figure 7
Example for a Read Access, with One Data Byte Transferred via DOUT

The data transfer is synchronized by the DCLK input. The contents of DIN is latched at the rising edge of DCLK, while DOUT changes with the falling edge of DCLK. During execution of commands that are followed by output data (read commands), the device will not accept any new command via DIN. The data transfer sequence is completed by setting $\overline{CS}$ to high.

To reduce the number of connections to the µP DIN and DOUT may be strapped together, and form a bi-directional data-'pin'.

For special applications a byte by byte transfer is needed. This can be done by prolonging the high time of DCLK for a user defined 'waiting time' after transferring any byte.
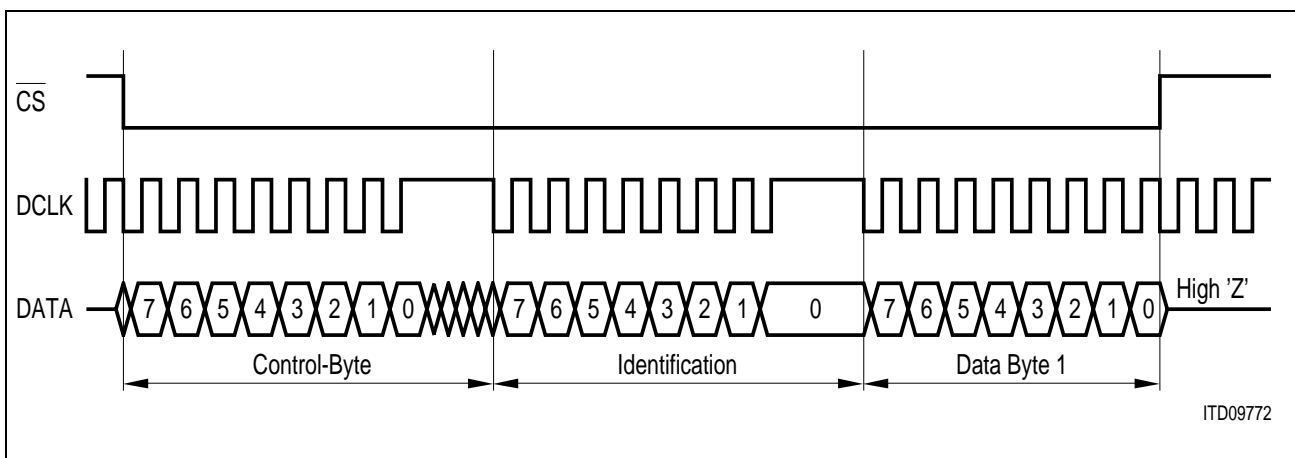

Figure 8
Example for a Write/Read Access, with a Byte by Byte Transfer, and DIN and DOUT Strapped Together

The Identification Byte is "81_H" for the PSB 2132/34.

2.5   The Signaling Interface

The SICOFI-2/4 TE signaling interface is made up of 2 input pins (SIx_0, SIx_1), two output pins (SOx_0, SOx_1) and three bi-directional programmable pins (SBx_0, SBx_1, SBx_2) per channel.
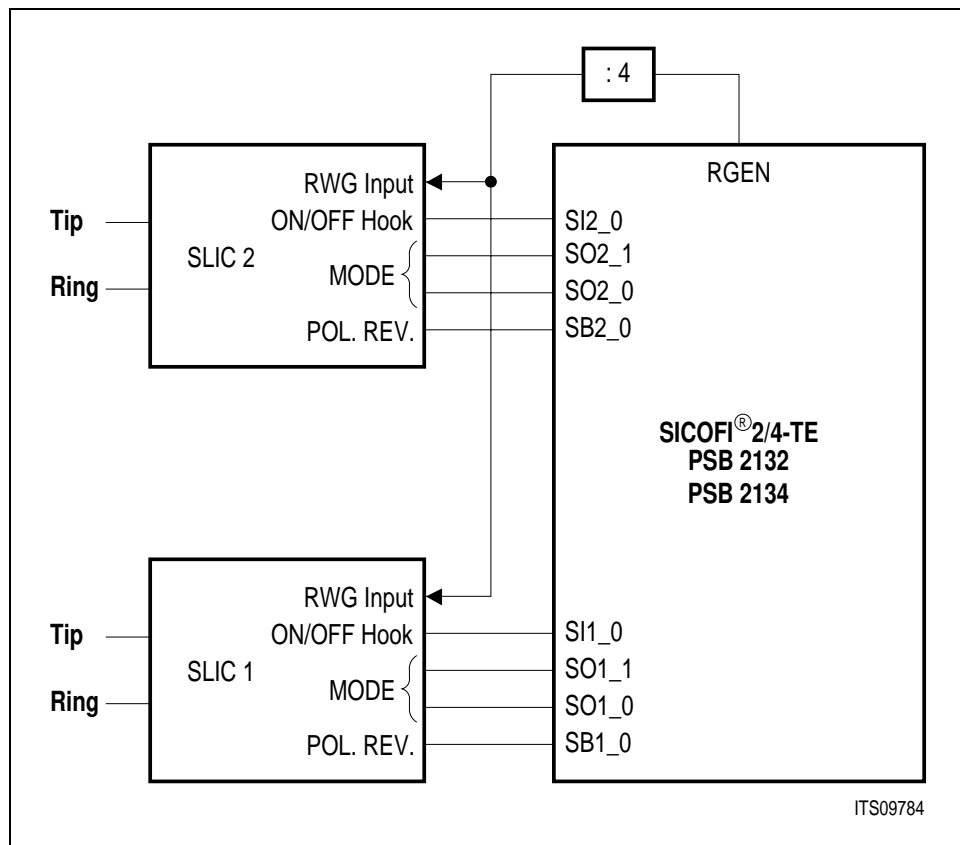

Figure 9

The purpose of these pins is to control the SLIC functions without additional ports on the host or microcontroller.
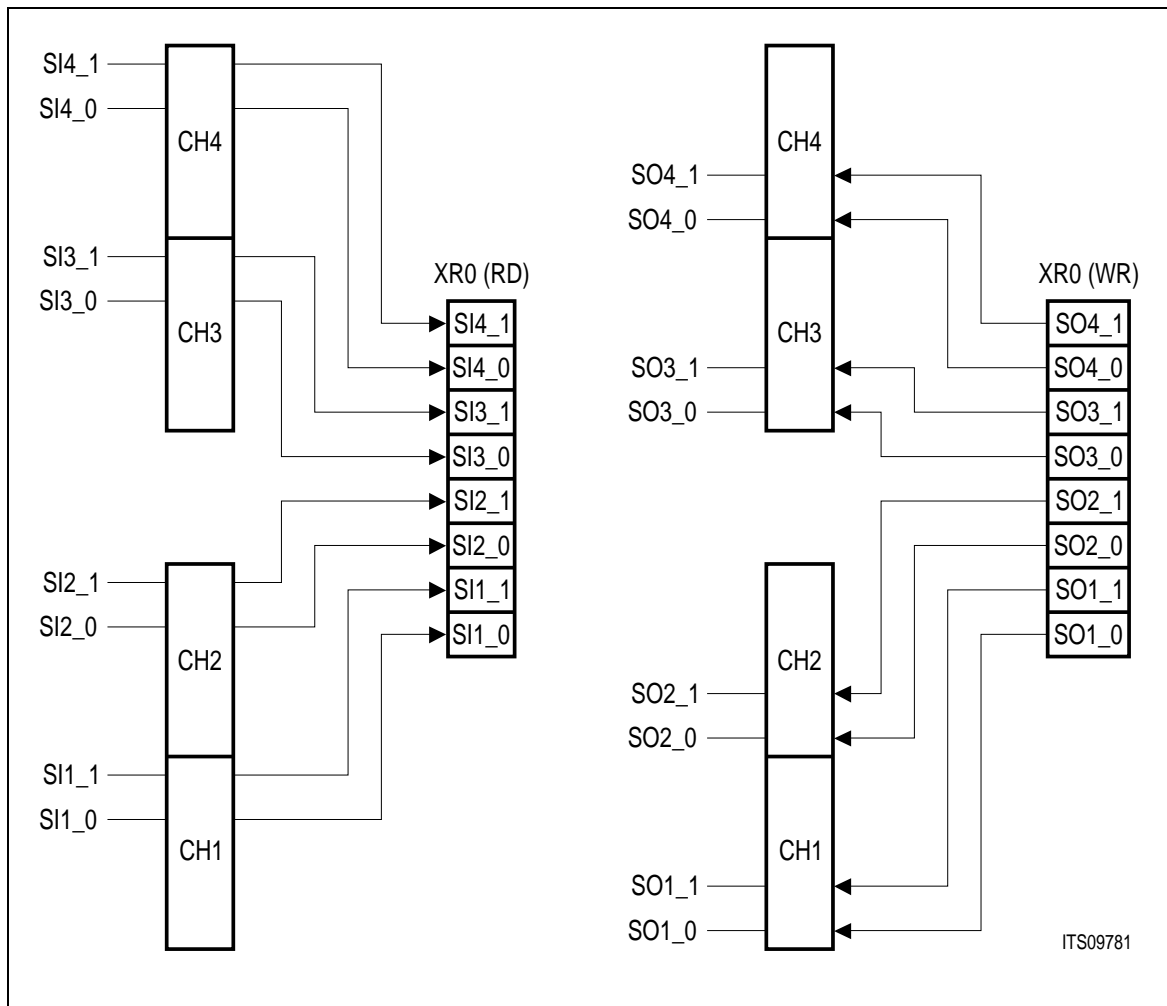
Figure 10

The status bits of all SIx_0 and SIx_1 inputs are stored in the XR0 register (RD). Similar the control bits of SOx_0 and SOx_1 are stored in the XR0 register (WR).

The bidirection status bits are arranged such that all SBx_1 and SBx_0 bits are controlled / read via the XR1 register. The correspondig direction register is the XR2 register. The third bidirectional status bit of each channel is accessed via the four most significant bits of the XR3 register while the least significant four bits specify the corresponding direction.
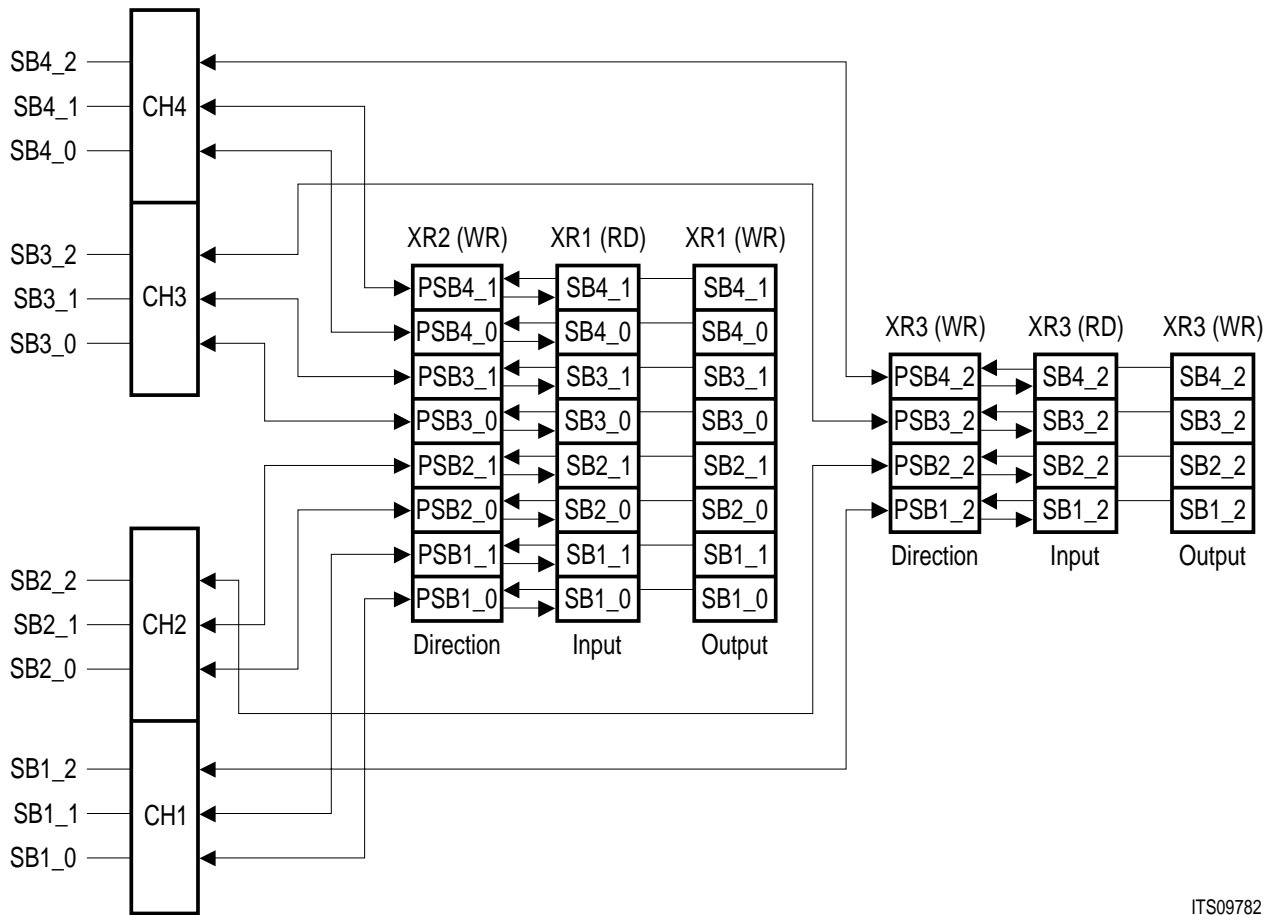
ITS09782

Figure 11

Depending on the application, the lines can be group individually to support the best software interface. E.g. if a DTMF receiver is connected to the SICOFI2/4-TE, the pins SB2_1, SB2_0,SB1_1,SB1_0 may be used for the data bus. This simplifies the software since the value can be read directly from the register.
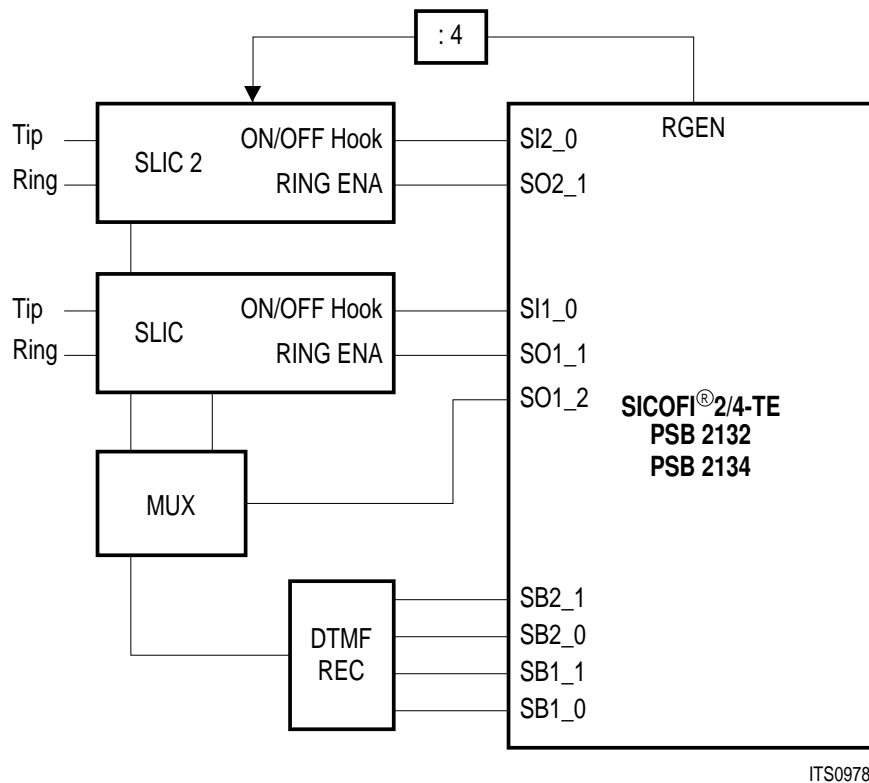
ITS09783

Figure 12

Additional two interrupt pins (INT12, INT34) are provided. If one of the input pins for channel 1 or 2, or one of the bi-directional pins for channel 1 and 2 (if programmed as inputs) changes, and being stable for the debounce time specified in Register XR4, INT12 will go from '0' to '1'. This interrupt is cleared if the appropriate registers (XR0, XR1 and XR3) are read via the serial µC-interface. Pin INT34 provides the same functionality for channel 3 and 4.

2.6 Ring Generator and Special Purpose Pin

For special purposes two additional output signals are provided by the SICOFI-2/4 TE.

RGEN (see also register XR4) will provide a programmable ring generator output of 2 to 28 ms. The output of RGEN diveded by four can be used to drive the ring input of a ringin SLIC. RGEN delivers a square-wave signal (duty cycle 1:1).

CHCLK will provide 3 different frequencies (256 kHz, 512 kHz or 16384 kHz). Both signals are only available if a valid signal is applied to the DCL-pin.

3   Programming the SICOFI®-2/4-TE

With the appropriate commands, the SICOFI2/4-TE can be programmed and verified very flexibly via the μ-Controller interface.

With the first byte received via DIN, one of 3 different types of commands (SOP, XOP and COP) is selected. Each of those can be used as a write or read command. Due to the extended SICOFI2/4-TE feature control facilities, SOP, COP and XOP commands contain additional information (e.g. number of subsequent bytes) for programming (write) and verifying (read) the SICOFI2/4-TE status.

A write command is followed by up to 8 bytes of data. The SICOFI2/4-TE responds to a read command with its specific identification and the requested information, that is up to 8 bytes of data.

3.1   Types of Command and Data Bytes

The 8-bit bytes have to be interpreted as either commands or status information stored in Configuration Registers or the Coefficient-RAM. There are three different types of SICOFI-2/4-TE commands which are selected by bit 3 and 4 as shown below.

SOP   **STATUS OPERATION:**   SICOFI2/4-TE status setting/monitoring

Bit   7   0

AD2	AD1		1	0			

XOP   **EXTENDED OPERATION:**   C/I[1)] channel configuration/evaluation

Bit   7   0

	0		1	1			

COP   **COEFFICIENT OPERATION:**   filter coefficient setting/monitoring

Bit   7   0

AD2	AD1		0				

Note: [1)] *Command/Indication (signaling) channel.*