



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



SCOUT-S

Siemens Codec with S/T
Transceiver

PSB 21381/2 Version 1.3

SCOUT-SX

Siemens Codec with S/T
Transceiver Featuring
Speakerphone Functionality

PSB 21383/4 Version 1.3

Wired
Communications



Never stop thinking.

Edition 2001-03-12

**Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München, Germany**

**© Infineon Technologies AG 2001.
All Rights Reserved.**

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

SCOUT-S

Siemens Codec with S/T
Transceiver

PSB 21381/2 Version 1.3

SCOUT-SX

Siemens Codec with S/T
Transceiver Featuring
Speakerphone Functionality

PSB 21383/4 Version 1.3

Wired
Communications



PSB 21381/2

PSB 21383/4

Revision History: 2001-03-12

DS 1

Previous Version: 09.99

Page	Subjects (major changes since last revision)
35	Figure with clock signals added
67	BCL=' 0' changed to BCL='1'
90	BCL changed from 'low' to 'high'
118	Note regarding AXI input added
169 170	BCL is inverted compared to last description (DS1); figure added
173	' <i>Rising</i> ' BCL edge changed to ' <i>falling</i> ' edge
245	Figure 95 modified
250 251	Timings added
251	Power supply currents added

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at <http://www.infineon.com>

Table of Contents		Page
1	Overview	1
1.1	Features	5
1.2	Pin Configuration	7
1.3	Logic Symbol	8
1.4	Pin Definitions and Function	9
1.5	Typical Applications	14
1.6	General Functions and Device Architecture	20
2	Interfaces	22
2.1	Microcontroller Interface	23
2.1.1	Serial Control Interface (SCI)	24
2.1.1.1	Programming Sequences	26
2.1.2	Parallel Microcontroller Interface	30
2.1.3	Interrupt Structure and Logic	32
2.1.4	Microcontroller Clock Generation	34
2.2	IOM-2 Interface	35
2.2.1	IOM-2 Frame Structure	36
2.2.2	IOM-2 Handler	37
2.2.2.1	Controller Data Access (CDA)	39
2.2.3	Serial Data Strobe Signal and strobed Data Clock	47
2.2.3.1	Serial Data Strobe Signal	47
2.2.3.2	Strobed IOM-2 Bit Clock	49
2.2.4	IOM-2 Monitor Channel	50
2.2.4.1	Handshake Procedure	52
2.2.4.2	Error Treatment	55
2.2.4.3	MONITOR Channel Programming as a Master Device	57
2.2.4.4	MONITOR Channel Programming as a Slave Device	57
2.2.4.5	MONITOR Time-Out Procedure	59
2.2.4.6	MONITOR Interrupt Logic	59
2.2.5	C/I Channel Handling	60
2.2.5.1	CIC Interrupt Logic	60
2.2.6	Settings after Reset (see also chapter 7.3)	61
2.2.7	D-Channel Access Control	62
2.2.7.1	TIC Bus D-Channel Access Control	62
2.2.7.2	S-Bus Priority Mechanism for D-Channel	64
2.2.8	Activation/Deactivation of IOM-2 Interface	67
2.3	S/T Interface	70
2.3.1	Wiring Configurations	70
2.3.2	Frame Structure	72
2.3.3	Multi-Framing	74
2.3.3.1	Interrupt Handling for Multi-Framing	75
2.3.4	Line Code	75
2.3.5	Phase Deviation	76

Table of Contents		Page
2.3.6	Data Transfer and Delay between IOM and S/T Interface	76
2.3.7	Control of Layer-1	77
2.3.7.1	Internal Layer-1 Statemachine	78
2.3.7.2	External Layer-1 Statemachine	87
2.3.8	Level Detection and Power Down	90
2.3.9	Transceiver Enable/Disable	90
2.3.10	Test Functions	91
2.3.10.1	Transceiver Tests	91
2.3.10.2	Test Signals	92
2.3.11	Transmitter Characteristics	92
2.3.12	Receiver Characteristics	93
2.3.13	Interface Circuitry	94
2.3.13.1	External Protection Circuitry	94
3	HDLC Controller	97
3.1	Message Transfer Modes	97
3.1.1	Non-Auto Mode (MDS2-0 = '01x')	98
3.1.2	Transparent Mode 0 (MDS2-0 = '110').	98
3.1.3	Transparent Mode 1 (MDS2-0 = '111').	98
3.1.4	Transparent Mode 2 (MDS2-0 = '101').	98
3.1.5	Extended Transparent Mode (MDS2-0 = '100').	98
3.2	Data Reception	98
3.2.1	Structure and Control of the Receive FIFO	98
3.2.1.1	General Description	98
3.2.1.2	Possible Error Conditions during Reception of Frames	102
3.2.1.3	Data Reception Procedure	103
3.2.2	Receive Frame Structure	105
3.3	Data Transmission	107
3.3.1	Structure and Control of the Transmit FIFO	107
3.3.1.1	General Description	107
3.3.1.2	Possible Error Conditions during Transmission of Frames	109
3.3.1.3	Data Transmission Procedure	110
3.3.2	Transmit Frame Structure	112
3.4	Access to IOM Channels	112
3.5	Extended Transparent Mode	113
3.5.1	Transmitter	113
3.5.2	Receiver	113
3.6	HDLC Controller Interrupts	114
3.7	Test Functions	115
4	Codec	116
4.1	Analog Front End (AFE) Description	117
4.1.1	AFE Attenuation Plan	118
4.2	Signal Processor (DSP) Description	120

Table of Contents		Page
4.2.1	Transmit Signal Processing	122
4.2.2	Receive Signal Processing	122
4.2.3	Programmable Coefficients for Transmit and Receive	124
4.3	Tone Generation	125
4.3.1	Four Signal Generators	125
4.3.2	Sequence Generator	125
4.3.3	Control Generator	128
4.3.4	Tone Filter	130
4.3.5	Tone Level Adjustment	132
4.3.6	DTMF Mode	132
4.4	Speakerphone Support	134
4.4.1	Attenuation Control Unit	135
4.4.2	Speakerphone Test Function and Self Adaption	136
4.4.3	Speech Detector	136
4.4.3.1	Background Noise Monitor	137
4.4.3.2	Signal Processing	138
4.4.4	Speech Comparators (SC)	139
4.4.4.1	Speech Comparator at the Acoustic Side (SCAE)	139
4.4.4.2	Speech Comparator at the Line Side (SCLE)	142
4.4.4.3	Automatic Gain Control of the Transmit Direction (AGCX)	144
4.4.5	Automatic Gain Control of the Receive Direction (AGCR)	147
4.4.6	Speakerphone Coefficient Set	150
4.5	Controlled Monitoring	152
4.6	Voice Data Manipulation	152
4.7	Test Functions	154
4.8	Programming of the Codec	155
4.8.1	Indirect Programming of the Codec (SOP, COP, XOP)	155
4.8.1.1	Description of the Command Word (CMDW)	156
4.8.2	Direct Programming of the Codec	158
4.8.2.1	CRAM Back-Up Procedure	158
4.8.3	Reference Tables for the Register and CRAM Locations	160
5	Clock Generation	169
5.1	Jitter	170
5.1.1	Jitter on IOM-2	170
5.1.2	Jitter on S	170
5.1.3	Jitter on MCLK	170
6	Reset	171
6.1	Reset Source Selection	172
6.2	External Reset Input	173
6.3	Software Reset Register (SRES)	173
6.4	Pin Behavior during Reset	173

Table of Contents		Page
7	Detailed Register Description	174
7.1	HDLC Control and C/I Registers	181
7.1.1	RFIFO - Receive FIFO	181
7.1.2	XFIFO - Transmit FIFO	181
7.1.3	ISTAH - Interrupt Status Register HDLC	182
7.1.4	MASKH - Mask Register HDLC	183
7.1.5	STAR - Status Register	183
7.1.6	CMDR - Command Register	184
7.1.7	MODEH - Mode Register	185
7.1.8	EXMR- Extended Mode Register	186
7.1.9	TIMR - Timer Register	188
7.1.10	SAP1 - SAPI1 Register	188
7.1.11	RBCL - Receive Frame Byte Count Low	189
7.1.12	SAP2 - SAPI2 Register	189
7.1.13	RBCH - Receive Frame Byte Count High	189
7.1.14	TEI1 - TEI1 Register 1	190
7.1.15	RSTA - Receive Status Register	191
7.1.16	TEI2 - TEI2 Register	192
7.1.17	TMH -Test Mode Register HDLC	193
7.1.18	CIR0 - Command/Indication Receive 0	194
7.1.19	CIX0 - Command/Indication Transmit 0	195
7.1.20	CIR1 - Command/Indication Receive 1	195
7.1.21	CIX1 - Command/Indication Transmit 1	196
7.2	Transceiver, Interrupt and General Configuration Registers	197
7.2.1	TR_CONF0 - Transceiver Configuration Register	197
7.2.2	TR_CONF1 - Receiver Configuration Register	198
7.2.3	TR_CONF2 - Transmitter Configuration Register	198
7.2.4	TR_STA - Transceiver Status Register	199
7.2.5	TR_CMD - Transceiver Command Register	200
7.2.6	SQRR- S/Q-Channel Receive Register	201
7.2.7	SQXR- S/Q-channel Transmit Register	201
7.2.8	ISTATR - Interrupt Status Register Transceiver	202
7.2.9	MASKTR - Mask Transceiver Interrupt	203
7.2.10	ISTA - Interrupt Status Register	204
7.2.11	MASK - Mask Register	205
7.2.12	MODE1 - Mode1 Register	205
7.2.13	MODE2 - Mode2 Register	208
7.2.14	ID - Identification Register	208
7.2.15	SRES - Software Reset Register	209
7.3	IOM-2 and MONITOR Handler	209
7.3.1	CDAXy - Controller Data Access Register xy	209
7.3.2	XXX_TSDPxy - Time Slot and Data Port Selection for CHxy	210
7.3.3	CDAX_CR - Control Register Controller Data Access CH1x	211

Table of Contents		Page
7.3.4	CO_CR - Control Register Codec Data	212
7.3.5	TR_CR - Control Register Transceiver Data	212
7.3.6	HCI_CR - Control Register for HDLC and CI1 Data	213
7.3.7	MON_CR - Control Register Monitor Data	213
7.3.8	SDSx_CR - Control Register Serial Data Strobe x	214
7.3.9	IOM_CR - Control Register IOM Data	215
7.3.10	MCDA - Monitoring CDA Bits	216
7.3.11	STI - Synchronous Transfer Interrupt	217
7.3.12	ASTI - Acknowledge Synchronous Transfer Interrupt	218
7.3.13	MSTI - Mask Synchronous Transfer Interrupt	218
7.3.14	SDS_CONF - Configuration Register for Serial Data Strokes	219
7.3.15	MOR - MONITOR Receive Channel	219
7.3.16	MOX - MONITOR Transmit Channel	219
7.3.17	MOSR - MONITOR Interrupt Status Register	220
7.3.18	MOCR - MONITOR Control Register	221
7.3.19	MSTA - MONITOR Status Register	222
7.3.20	MCONF - MONITOR Configuration Register	222
7.4	Codec Configuration Registers	223
7.4.1	General Configuration Register (GCR)	223
7.4.2	Programmable Filter Configuration Register (PFCR)	224
7.4.3	Tone Generator Configuration Register (TGCR)	225
7.4.4	Tone Generator Switch Register (TGSR)	226
7.4.5	AFE Configuration Register (ACR)	227
7.4.6	AFE Transmit Configuration Register (ATCR)	228
7.4.7	AFE Receive Configuration Register (ARCR)	229
7.4.8	Data Format Register (DFR)	230
7.4.9	Data Source Selection Register (DSSR)	231
7.4.10	Extended Configuration (XCR) and Status (XSR) Register	232
7.4.11	Mask Channel x Register (MASKxR)	234
7.4.12	Test Function Configuration Register (TFCR)	235
7.4.13	CRAM Control (CCR) and Status (CSR) Register	236
7.4.14	CRAM (Coefficient RAM)	237
8	Electrical Characteristics	241
8.1	Electrical Characteristics (general part)	241
8.1.1	Absolute Maximum Ratings	241
8.1.2	DC-Characteristics	241
8.1.3	Capacitances	242
8.1.4	Oscillator Specification	243
8.1.5	AC Characteristics	244
8.1.6	IOM-2 Interface Timing	245
8.1.7	Microcontroller Interface Timing	247
8.1.7.1	Serial Control Interface (SCI) Timing	247

Table of Contents		Page
8.1.7.2	Parallel Microcontroller Interface Timing	248
8.1.8	Reset	251
8.2	Electrical Characteristics (Transceiver Part)	251
8.3	Electrical Characteristics (Codec Part)	253
8.3.1	DC Characteristics	253
8.3.2	Analog Front End Input Characteristics	256
8.3.3	Analog Front End Output Characteristics	256
9	Package Outlines	258

1 Overview

The SCOUT-S or SCOUT-SX respectively integrates all necessary functions for the completion of a cost effective ISDN voice terminal solution.

Please note: Throughout the whole document “SCOUT™” refers to “SCOUT™-S” and “SCOUT™-SX”

The SCOUT combines the functionality of the ARCOFI®-BA PSB 2161 (Audio Ringing Codec Filter Basic Function) or ARCOFI®-SP PSB 2163 (Audio Ringing Codec Filter with Speakerphone) respectively and the ISAC®-S TE PSB 2186 (ISDN Subscriber Access Controller for Terminals) on a single chip.

The SCOUT-S is suited for the use in basic ISDN voice terminals just as it is, and in combination with an additional device on the modular IOM®-2 interface, in high end featurephones e.g. with acoustic echo cancellation.

The SCOUT-SX PSB 21383 is an extended SCOUT-S PSB 21381 which provides the speakerphone performance of the ARCOFI-SP PSB 2163.

The transceiver implements the subscriber access functions for an ISDN terminal to be connected to a four wire S/T interface. It covers complete layer-1 and basic layer-2 functions for digital terminals.

The codec performs encoding, decoding, filtering functions and tone generation (ringing, audible feedback tones and DTMF signal). An analog front end offers three analog inputs and two analog outputs with programmable amplifiers.

The IOM-2 interface allows a modular design with functional extensions (e.g. acoustic echo cancellation, tip/ring extension, modem extension, answering machine, video or data terminal) by connecting other voice/data devices to the SCOUT.

In the P-MQFP-44 package (PSB21381/3) only a serial microcontroller interface (SCI) is supported.

In the P-MQFP-64 package (PSB21382/4) a serial and parallel microcontroller interface are supported. A clock signal and a reset input and output pin complete the microcontroller interface.

The SCOUT is a CMOS device and operates with a 3.3 V or 5 V supply.

Comparison of the SCOUT with the two chip solution ISAC-S TE and ARCOFI-BA; -SP

	SCOUT	ISAC-S TE / ARCOFI
Operating modes	TE	TE
Supply voltage	3.3V ± 5 % or 5V ± 5 %	5V ± 5 %
Technology	CMOS	CMOS, BICMOS
Package	P-MQFP-44, P-MQFP-64	P-MQFP-64 / P-DSO-28
Transceiver		
Transformer ratio for receiver and transmitter	1:1	2:1
Test Functions	<ul style="list-style-type: none"> - Dig. loop via Layer-2 (TLP) - Layer-1 disable (DIS_TR) - Analog loop (LP_A- bit EXLP- bit, ARL) 	<ul style="list-style-type: none"> - Dig. loop via Layer-2 (TLP) - Layer-1 disable (TEM) - Analog loop (ARL)
Microcontroller Interface	Serial (SCI) 8-bit parallel (MQFP-64): Motorola Mux Siemens/Intel Mux Siemens/Intel Non-Mux direct/ indirect Addressing	Not provided 8-bit parallel: Motorola Mux Siemens/Intel Mux Siemens/Intel Non-Mux
Microcontroller clock	Provided (7.68, 3.84, 0.96MHz, disabled)	Not provided
Register address space	256 byte (32 byte FIFO, 96 byte configuration, 128 byte CRAM)	204 byte (32 byte FIFO, 32+12 byte configuration, 128 byte CRAM)
Codec CRAM access (128 byte)	Indirect and direct addressing (general purpose RAM)	Indirect addressing
Command structure of the register access	Header/ address(command)/data	Address (command)/data
Controller data access to IOM-2 timeslots	All timeslots; various possibilities of data access	Restricted access to B- and IC-channel

Overview

	SCOUT	ISAC-S TE / ARCOFI
Data control and manipulation	Various possibilities of data control and data manipulation (enable/disable, shifting, looping, switching)	B- and IC-channel looping
IOM-2		
IOM-2 Interface	Double clock (DCL), bit clock pin (BCL), serial data strobe 1 (SDS1) serial data strobe 2 (SDS2/ \overline{RSTO})	Double clock (DCL), bit clock (BCL), serial data strobe (SDS)
Monitor channel programming	Provided (MON0, 1 or 2)	Provided (MON0 or 1)
C/I channels	CI0 (4bits), CI1 (4/6bits)	CI0 (4bits), CI1 (6bits)
Layer-1 statemachine	With changes in ISAC-S for correspondence with the actual ITU Specification	
Statemachine in software	Possible	Not possible
IDSL (144kBit/s)	Provided (HDLC, SDS)	Not provided
HDLC support	D- and B- channels; Non-auto mode, transparent mode 0-2, extended transparent mode	D-channels; auto mode, non-auto mode, transparent mode 1-3
FIFO size	64 bytes per direction with programmable FIFO thresholds	2x32 bytes per direction
Reset Sources	\overline{RST} Input Watchdog C/I Code Change \overline{EAW} Pin Software Reset	\overline{RST} Input Watchdog C/I Code Change EAW Pin
Codec		
Analog inputs	1 single ended, 2 differential	1 single ended, 2 differential
Band gap reference	Externally buffered	Internally buffered

Overview

	SCOUT	ISAC-S TE / ARCOFI
Max. AFE gain transmit (guaranteed transmission characteristics)	36 dB differential inputs 24 dB single ended input	42 dB differential inputs 24 dB single ended input
Analog gain steps earpiece	3 dB	6 dB
Speakerphone		
Status indication	Register status bits	Piezo pins
AGC initialization	Initial value	Maximum gain
Voice data manipulation	Three party conferencing (adding receive and transmit data) Voice monitoring on IOM-2	Three party conferencing (adding receive data) Voice monitoring on piezo output
Voice data formats	A-/μ-Law, 8 or 16 bit linear	A-/μ-Law, 16 bit linear
Mask register for voice data	Provided	Not provided
Tone Generator Output	Loudspeaker, earpiece	Loudspeaker, earpiece, piezo pins
Direct tone generator output to loudspeaker	Provided Tone generator signal is attenuated by -6dB compared to the ARCOFI; extended gain range (-24.5, -27.5dB) in the loudspeaker amplifier control setting	Provided
Saturation amplification of tone filter, i.e. CRAM Parameter GE	As specified	Adjusted to fix value

Siemens Codec with U_{PN} Transceiver SCOUT-S, SCOUT-SX

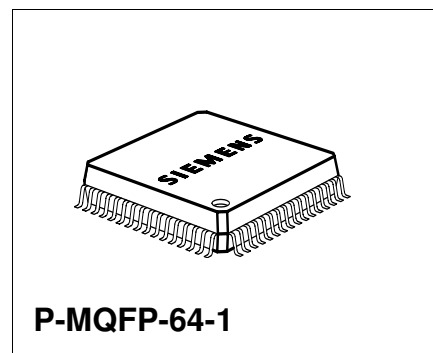
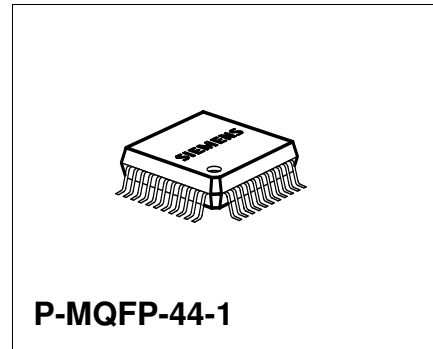
PSB 21381/2
PSB 21383/4

Version 1.3

CMOS

1.1 Features

- 8-bit parallel microcontroller interface (only PSB 21382/4 in P-MQFP-64 package), Motorola, Siemens/Intel bus type multiplexed or non-multiplexed, direct-/indirect register addressing
- Serial control interface (SCI)
- IOM-2 interface in TE mode, single/double clock, two serial data strobe signals
- Various possibilities of microcontroller data access, data control and data manipulation to all IOM-2 timeslots
- Power supply 3.3V or 5V
- Monitor channel handler (master/slave)
- Sophisticated power management for restricted power mode
- Programmable microcontroller clock output and reset (input/output) pins
- Advanced CMOS technology



Transceiver part

- Full duplex 2B+D S/T interface transceiver according to ITU-T I.430
- Conversion of the frame structure between the S/T interface and IOM-2
- Receive timing recovery
- Continuously adapted receive thresholds
- D-channel access control
- Access to S and Q bits of S/T interface

Type		Package
PSB 21381	SCOUT-S	P-MQFP-44-1
PSB 21383	SCOUT-SX	P-MQFP-44-1
PSB 21382	SCOUT-S	P-MQFP-64-1
PSB 21384	SCOUT-SX	P-MQFP-64-1

Overview

- Activation and deactivation procedures with automatic activation from power down state
- HDLC controller. Operating in non-auto mode, transparent mode 0-2 or extended transparent mode. Access to B1, B2 or D channels or the combination of them e.g. for 144 kbit/s data transmission (2B+D)
- FIFO buffer with 64 bytes per direction and programmable FIFO thresholds for efficient transfer of data packets
- Implementation of IOM-2 MONITOR and C/I-channel protocol to control peripheral devices
- Realization of layer-1 statemachine in software possible
- Watchdog timer
- Programmable reset sources
- Test loops and functions

Codec part

- Applications in digital terminal equipment featuring voice functions
- Digital signal processing performs all CODEC functions
- Fully compatible with the ITU-T G.712 and ETSI (NET33) specification
- PCM A-Law/ μ -Law (ITU-T G.711) and 8/16-bit linear data; maskable codec data
- Flexible configuration of all internal functions
- Three analog inputs for the handset microphone, the speakerphone and the headset
- Two differential outputs for a handset earpiece (200 Ω) and a loudspeaker (50 Ω for 5V power supply, 25 Ω for 3.3V power supply)
- Flexible test and maintenance loopbacks in the analog front end and the digital signal processor
- Independent gain programmable amplifiers for all analog inputs and outputs
- Full digital speakerphone (SCOUT-SX only) and loudhearing support without any external components (speakerphone test and optimization function is available)
- Enhanced voice data manipulation for features like:
 - Three-party conferencing
 - Voice monitoring
- Two transducer correction filters
- Side tone gain adjustment
- Flexible DTMF, tone and ringing generator
- Direct and indirect CARAM access

1.2 Pin Configuration

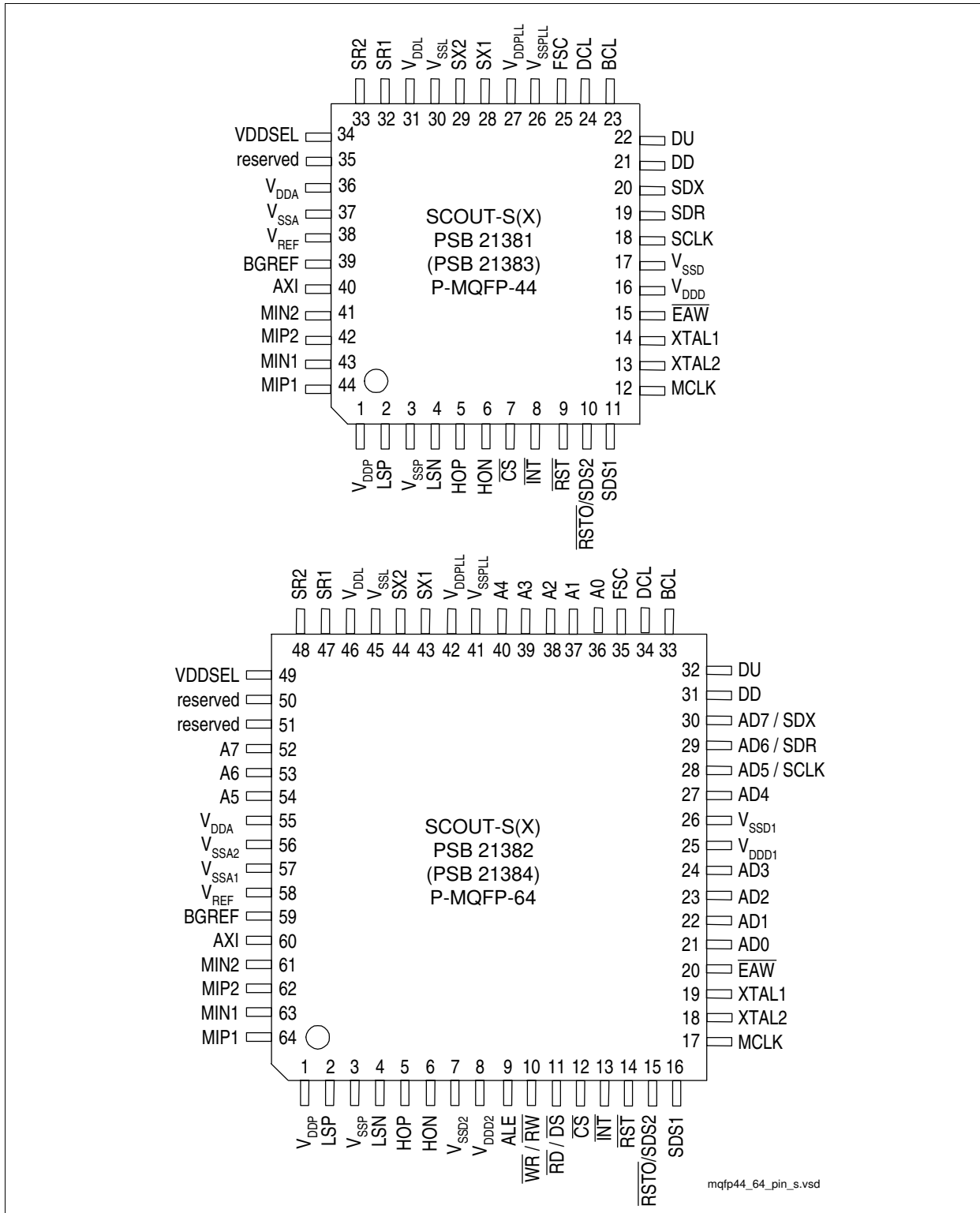


Figure 1
Pin Configuration

1.3 Logic Symbol

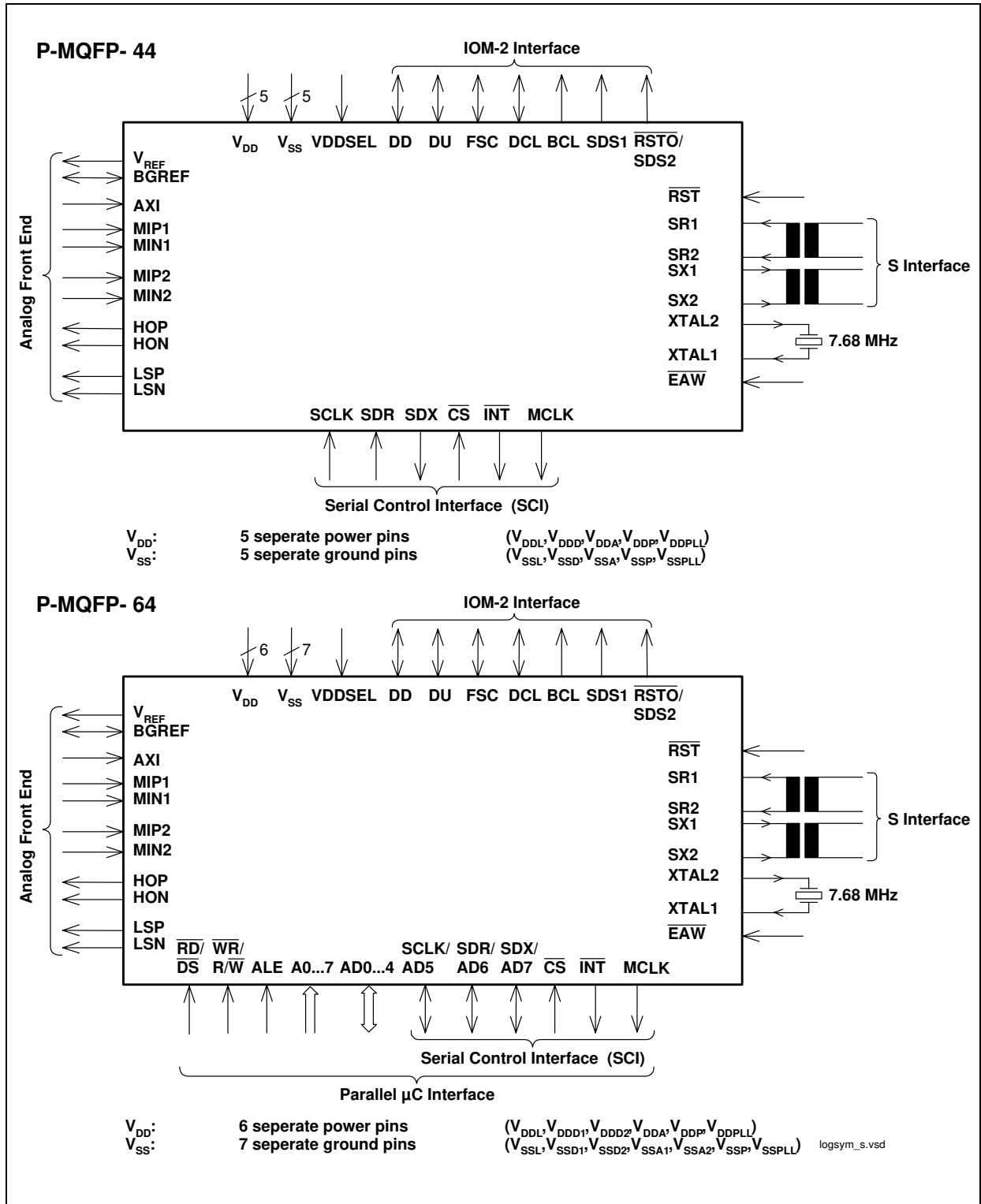


Figure 2
Logic Symbol of the SCOUT in P-MQFP-44 and P-MQFP-64

1.4 Pin Definitions and Function

Table 1

Pin No. MQFP-44	Pin No. MQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
				Power supply (3.3 V or 5 V ± 5 %)
31	46	V_{DDL}	—	Supply voltage for line driver
16		V_{DDD}	—	Supply voltage for digital parts
	25	V_{DDD1}		
	8	V_{DDD2}		
36	55	V_{DDA}	—	Supply voltage for analog parts
1	1	V_{DDP}	—	Supply voltage for loudspeaker
27	42	V_{DDPLL}	—	Supply voltage for internal PLL
30	45	V_{SSL}	—	Ground for line driver
17		V_{SSD}	—	Ground for digital parts
	26	V_{SSD1}		
	7	V_{SSD2}		
37		V_{SSA}	—	Ground for analog parts
	57	V_{SSA2}		
	56	V_{SSA1}		
3	3	V_{SSP}	—	Ground for loudspeaker
26	41	V_{SSPLL}	—	Ground for internal PLL
34	49	VDDSEL	I	VDD Selection '0': 3.3 V supply voltage '1': 5 V supply voltage
				IOM-2 Interface
21	31	DD	I/OD/O	Data Downstream
22	32	DU	I/OD/O	Data Upstream
25	35	FSC	I/O	Frame Synchronization Clock (8 kHz)
24	34	DCL	I/O	Data Clock I: single or double clock (programmable) O: double clock, 1.536 MHz
23	33	BCL	O	Bit Clock (768kHz)

Table 1 (cont'd)

Pin No. MQFP-44	Pin No. MQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
11	16	SDS1	O	Programmable strobe signal or bit clock
10	15	$\overline{\text{RSTO}}$ / SDS2	OD O	Reset Output (active low) Programmable strobe signal or bit clock
9	14	$\overline{\text{RST}}$	I	RESET Reset (active low)
32 33 28 29 13 14 15	47 48 43 44 18 19 20	SR1 SR2 SX1 SX2 XTAL2 XTAL1 $\overline{\text{EAW}}$	I I O O OI I I	Transceiver S-Bus receiver input S-Bus receiver input S-Bus transmitter output (positive) S-Bus transmitter output (negative) Oscillator output Oscillator or 7.68 MHz input External Awake. A low level on this input starts the oscillator from the power down state and generates a reset pulse if enabled (see chapter 7.2.12) In addition an interrupt request is generated at pin $\overline{\text{INT}}$.
8 12 7 -	13 17 12 9	$\overline{\text{INT}}$ MCLK $\overline{\text{CS}}$ ALE	OD O I I	Microcontroller Interface Interrupt request (active low) Microcontroller Clock Chip Select (active low) During reset also used as interface selection pin (see chapter 2.1) Multiplexed bus mode: Address Latch Enable Non-multiplexed bus and serial mode: Interface selection pin (see chapter 2.1)

Table 1 (cont'd)

Pin No. MQFP-44	Pin No. MQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
-	10	\overline{WR}	I	Write access in Intel bus mode (active low)
		R/\overline{W}	I	Read/write access in Motorola bus mode During reset also used as interface selection pin (see chapter 2.1)
	11	\overline{RD}	I	Read access in Intel bus mode (active low)
		\overline{DS}	I	Data strobe in Motorola bus mode (active low) During reset also used as interface selection pin (see chapter 2.1)
18	28	SCLK	I	Clock for the serial control interface
		SCLK AD5	I I/O	Serial control interface: Clock Multiplexed bus mode: Address/data line bit 5 Non-multiplexed bus mode: Data line bit 5
19	29	SDR	I	Serial Data Receive
		SDR AD6	I I/O	Serial control interface: Data receive Multiplexed bus mode: Address/data line bit 6 Non-multiplexed bus mode: Data line bit 6
20	30	SDX	OD/O	Serial Data Transmit
		SDX AD7	OD/O	Serial control interface: Data transmit Multiplexed bus mode: Address/data line bit 7 Non-multiplexed bus mode: Data line bit 7
-	21	AD0	I/O	Multiplexed bus mode: Address/data lines
	22	AD1	I/O	
	23	AD2	I/O	Non-multiplexed bus mode: Data lines
	24	AD3	I/O	
	27	AD4	I/O	

Table 1 (cont'd)

Pin No. MQFP-44	Pin No. MQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
-	36	A0	I	Multiplexed bus mode: Not used, has to be connected to V_{DD} Non-multiplexed bus mode: Address bus. For indirect address mode only A0 is valid
	37	A1	I	
	38	A2	I	
	39	A3	I	
	40	A4	I	
	54	A5	I	
	53	A6	I	
	52	A7	I	

Table 1 (cont'd)

Pin No. MQFP-44	Pin No. MQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
38	58	V_{REF}	O	Analog Frontend 2.4V Reference voltage for biasing external circuitry An external capacity of $\geq 100\text{nF}$ has to be connected
39	59	BGREF	I/O	Reference Bandgap voltage for internal references An external capacity of $\geq 22\text{nF}$ has to be connected
40	60	AXI	I	Single-ended Auxiliary Input
44	64	MIP1	I	Symmetrical differential Microphone Input 1
43	63	MIN1	I	
42	62	MIP2	I	Symmetrical differential Microphone Input 2
41	61	MIN2	I	
5	5	HOP	O	Differential Handset earpiece output for $200\ \Omega$ transducers
6	6	HON	O	
2	2	LSP	O	Differential Loudspeaker output for $50\ \Omega$ or $25\ \Omega$ loudspeaker using a power supply of 5 V or 3.3 V respectively
4	4	LSN	O	
35	50	<u>reserved</u>	I	Reserved Pins This input is not used for normal operation and must be connected to <i>VDD</i> .
	51	<u>reserved</u>	I	This input is not used for normal operation and must be connected to <i>VSS</i> .

1.5 Typical Applications

The SCOUT can be used in a variety of applications like

- ISDN voice terminal (**Figure 3**)
- ISDN voice terminal with speakerphone (**Figure 4**)
- ISDN voice terminal as featurephone with acoustic echo cancellation (**Figure 5**)
- ISDN voice terminal with tip/ring extension (**Figure 6**)
- ISDN voice terminal with answering machine (**Figure 7**)
- ISDN voice terminal with full duplex speakerphone and answering machine (**Figure 8**)
- ISDN videophone with speakerphone (**Figure 9**)
- ISDN videophone with full duplex speakerphone (**Figure 10**)
- ISDN voice/data terminal on a PC card (**Figure 11**)
- ISDN voice/data terminal with tip/ring extension (**Figure 12**)
- Terminal Adapter with dual tip/ring (**Figure 13**)

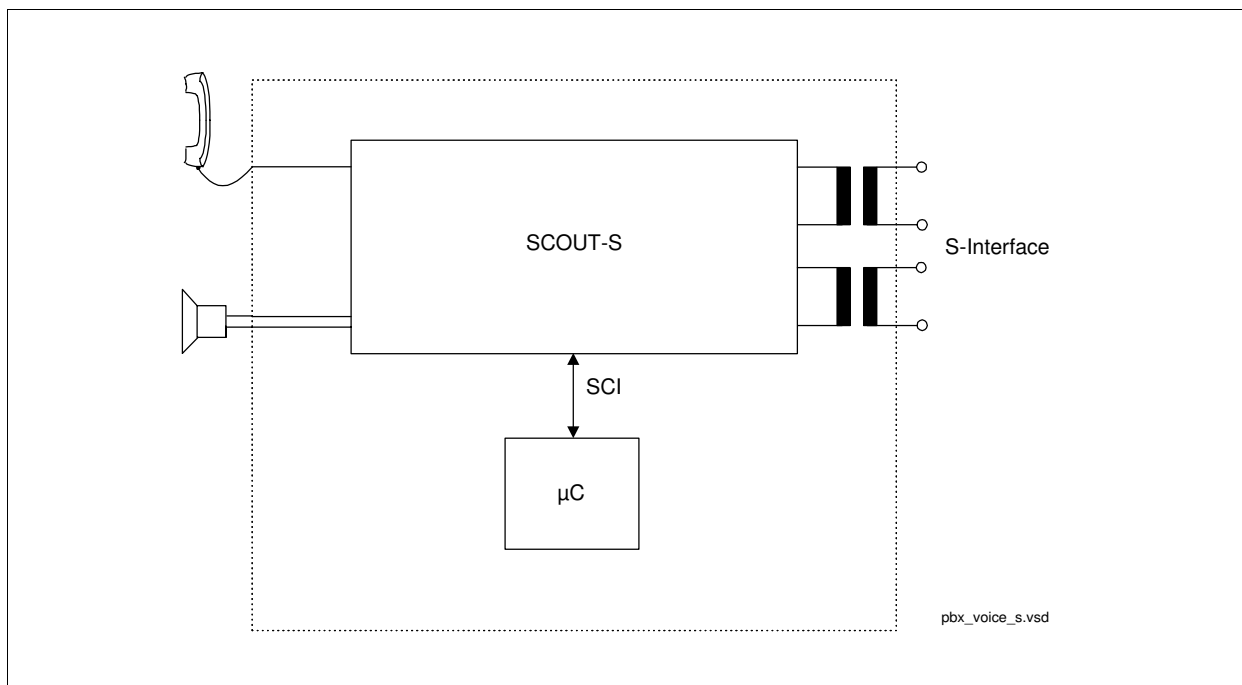


Figure 3
ISDN Voice Terminal

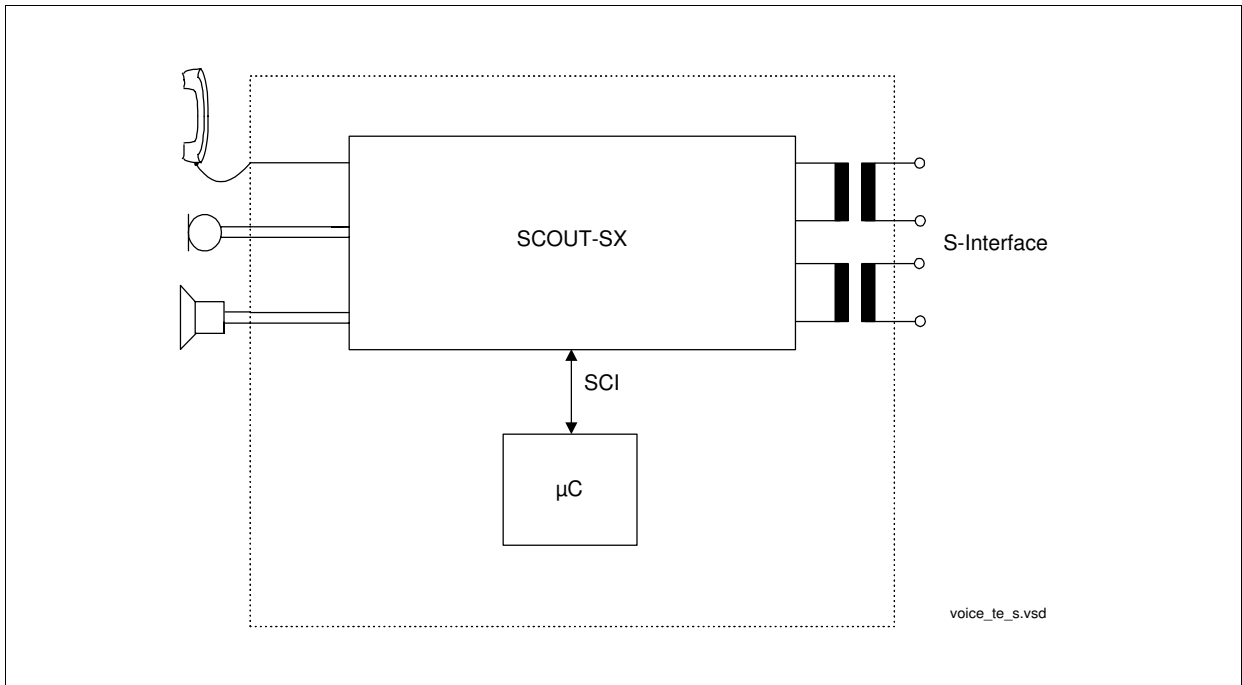


Figure 4
ISDN Voice Terminal with Speakerphone

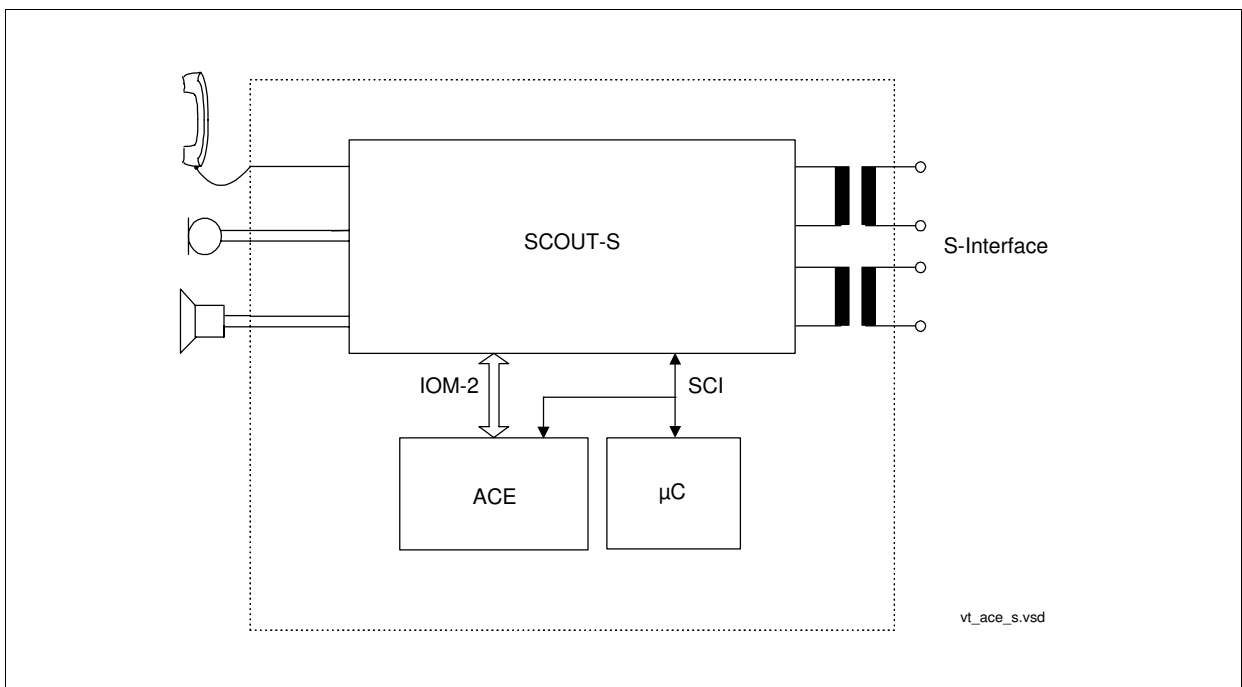


Figure 5
ISDN Voice Terminal as Featurephone with Acoustic Echo Cancellation