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Data Sheet, DS 1, Mar. 2003

# INCA-D

## Infineon Codec with DASL Transceiver and embedded Microcontroller Featuring Acoustic Echo Cancellation

## PSB 21473 Version 1.3

Wired Communications

Never stop thinking.

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**Data Sheet**

| **Revision History:** | **2003-03-31** | DS 1 |
|---|---|---|
| Previous Version: | 02.01 / Data Sheet DS3 | |

| **Page** | **Subjects (major changes since last revision)** |
|---|---|
| 52/ 173 | Reset value of SYSCON modified |
| 74 | Table entries deleted |
| 103 | HDLEN bit of register PSW removed |
| 174 | Reset value of BUSCON0 corrected |
| 181 | Reset value of WDTCON corrected |
| 232 | S0CON.RXDI bit moved to position 5 |
| 407 | Peak Detector has no output |
| 420 | Note for PIDDHWCFG added |
| 421ff | Modified formulas marked by vertical change bars |
| 507 | DSP register descriptions moved |
| 508 | Description of keyscanner interrupt generation modified |
| 515 | *14* interfaces and *6* Alternate settings supported (see vertical change bars) |
| 516 | Description regarding physical vs. logical endpoints modified |
| 516 | Figure for Configuraton 0 added |
| 550 | Bit position of AIM and IWIE |
| 559 | Description of CIAR modified |
| 560 | Reset of bits in GEPIR |
| 562 | Two bits in register CIARIE added |
| 566 | Device Detach Interrupt not available |
| 567 | Description for SUI modified |
| 583 | Sleep mode description modified |
| 608 | Reset values adapted |
| 633 | Absolute Maximum Ratings modified |
| 634ff | DC characteristics modified |
| 656 | DC characteristics of transceiver removed (informaton partly moved to DC char.) |
| 659ff | Values for ADC charateristics modified, transmission characteristics for AFE |

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**Table of Contents** **Page**

**Table of Contents** **Page**

**Table of Contents** **Page**

**Table of Contents** **Page**

**Table of Contents** **Page**

**Table of Contents** **Page**

**Table of Contents** **Page**

**Table of Contents** **Page**

**Table of Contents** **Page**

**Table of Contents** **Page**

# 1 Overview

The INCA-D integrates all necessary functions for the completion of a digital voice terminal solution.

The line transceiver of the INCA-D implements the subscriber access functions for a digital terminal to be connected to a two wire DASL interface. It covers complete layer-1 and basic layer-2 functions for digital terminals.

Different interfaces allow the connection to a variety of devices including an Full Speed USB interface for PC host communication.

The basic application of the INCA-D is the use in terminal equipment applications where microphone, loudspeaker, headset or handset can be directly connected to the Analog Frontend.

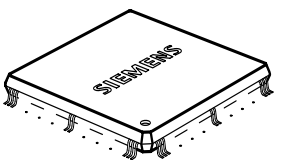
The Analog Front End and the integrated fixpoint DSP perform encoding, decoding, filtering functions and tone generation (ringing, audible feedback tones and DTMF signal). A full duplex echo cancellation mechanism provides high quality speakerphone functionality.

The INCA-D is a CMOS device and operates with a single 3.3V supply.

**Infineon Codec with DASL Transceiver and embedded Microcontroller Featuring Acoustic Echo Cancellation INCA-D** **PSB 21473**

**Version 1.3** **CMOS**

## 1.1 Features




**P-TQFP-144**

### 1.1.1 16 bit CPU, Internal RAM and Memory Interface

- Bootstrap Loader Function
- On Chip Memory: Dual Port SRAM (2 KBytes) & General Purpose SRAM (4 KBytes)
- On Chip Debug System OCDS (Level 1)
- Interrupt Controller supporting up to 27 nodes
- Peripheral Event Controller (PEC) for up to 8 channels
- External Memory Interface supporting 8 bit or 16 bit data, multiplexed and demultiplexed
- Up to 4 MBytes linear address space for external code and data
- 3 programmable Chip Selects
- Programmable Watchdog Timer

### 1.1.2 General Purpose Timer Unit

Timer Block 1:
- $f_{Timer}/4$ maximum resolution.
- 3 independent timers/counters.
- Timers/counters can be concatenated.
- 4 operating modes (timer, gated timer, counter, incremental).

Timer Block 2:
- $f_{Timer}/2$ maximum resolution.
- 2 independent timers/counters.
- Timers/counters can be concatenated.
- 3 operating modes (timer, gated timer, counter).
- Extended capture/reload functions via 16-bit Capture/Reload register CAPREL.

| Type | Package |
|---|---|
| PSB 21473 | P-TQFP-144 |

### 1.1.3 Asynchronous/Synchronous Serial Interface (ASC)

Full duplex asynchronous operating modes
- 8- or 9-bit data frames, LSB first
- Parity bit generation/checking
- One or two stop bits
- Baudrate from 1.5 MBaud to 0.3552 Baud (@24 MHz CPU clock)
- Multiprocessor mode for automatic address/data byte detection
- Loop-back capability

Half-duplex 8-bit synchronous operating mode
- Baudrate from 3 MBaud to 305.76 Baud (@ 24 MHz CPU clock)
- Double buffered transmitter/receiver

### 1.1.4 Two Serial Channel Interfaces (SSC)

- Master and slave mode operation
- Full-duplex or half-duplex operation
- Flexible data format
- Programmable number of data bits : 2 to 16 bit
- Programmable shift direction : LSB or MSB shift first
- Programmable clock polarity : idle low or high state for the shift clock
- Programmable clock/data phase : data shift with leading or trailing edge of SCLK

- Baudrate generation from 12 MBaud to 183.1 Baud (@ 24 MHz module clock)

Interrupt generation
- on a transmitter empty condition
- on a receiver full condition
- on an error condition (receive, phase, baudrate, transmit error)

### 1.1.5 USB Interface

- USB specification v1.1 compliant
- 12 Mbit/s Full-Speed Mode
- 15 Interfaces and 7 Alternate Settings supported
- 15 SW-configurable Endpoints, in addition to the bi-directional Control Endpoint 0
- Flexible Memory Management to support Endpoint Buffer Sizes of up to 64 Bytes
- Each non-Control Endpoint can be either Isochronous, Bulk or Interrupt

### 1.1.6 16 bit fixed-point DSP

- Full-duplex echo cancellation with noise reduction

- PCM A-Law/µ-Law (ITU-T G.711) and 8/16-bit linear data
- Two transducer correction filters
- Side tone gain adjustment
- Set of functional units as described (e.g. Tone Generator, DTMF Receiver)
- Access to two independent 16 bit time slots for up to three voice channels

### 1.1.7 Analog Front End

- Three differential inputs for the handset, the speakerphone and the headset microphone
- Three differential outputs for a handset ear piece (200 Ω), a headset (200 Ω) and a loudspeaker
- 80 mW @ 25 Ω or 100 mW @ 20 Ω loudspeaker driver capability
- Flexible test and maintenance loop backs in the analog front end
- Gain programmable amplifiers for all analog inputs and outputs
- PCM Codec, fully compatible with the ITU-T G.712 and ETSI (NET33) specification
- Additional summing point to add the Tone Generator output signal and the analog converted audio output from the DSP. The result is fed to the loudspeaker.

### 1.1.8 Transceiver

- Two wire DASL transceiver with AMI coded 2B+D channels

### 1.1.9 Terminal Specific Functions (TSF)

- Keypad Scanner for up to 45 keys
- LED Multiplex Unit (3*8 LEDs)

### 1.1.10 IOM-2 Handler

- IOM-2 Interface
- HDLC controller: Access to B1, B2 or D channels or the combination of them e.g. for 144 kbit data transmission (2B+D)
- 2* 64 byte FIFO buffer for efficient D-channel transfer of data packets
- Implementation of C/I-channel protocol to control peripheral devices
- Test loops and functions
- Data Control Unit for fast data transfers from IOM-2 time slots to memory and vice versa

### 1.1.11 General Features

- Power Management
- Single 15.36 MHz crystal
- On Chip PLL and a set of clock frequency divider
- 3.3V Single Supply Voltage

## 1.2 Logical Symbols

**Figure 1-1** illustrates the logical symbol of the INCA-D.

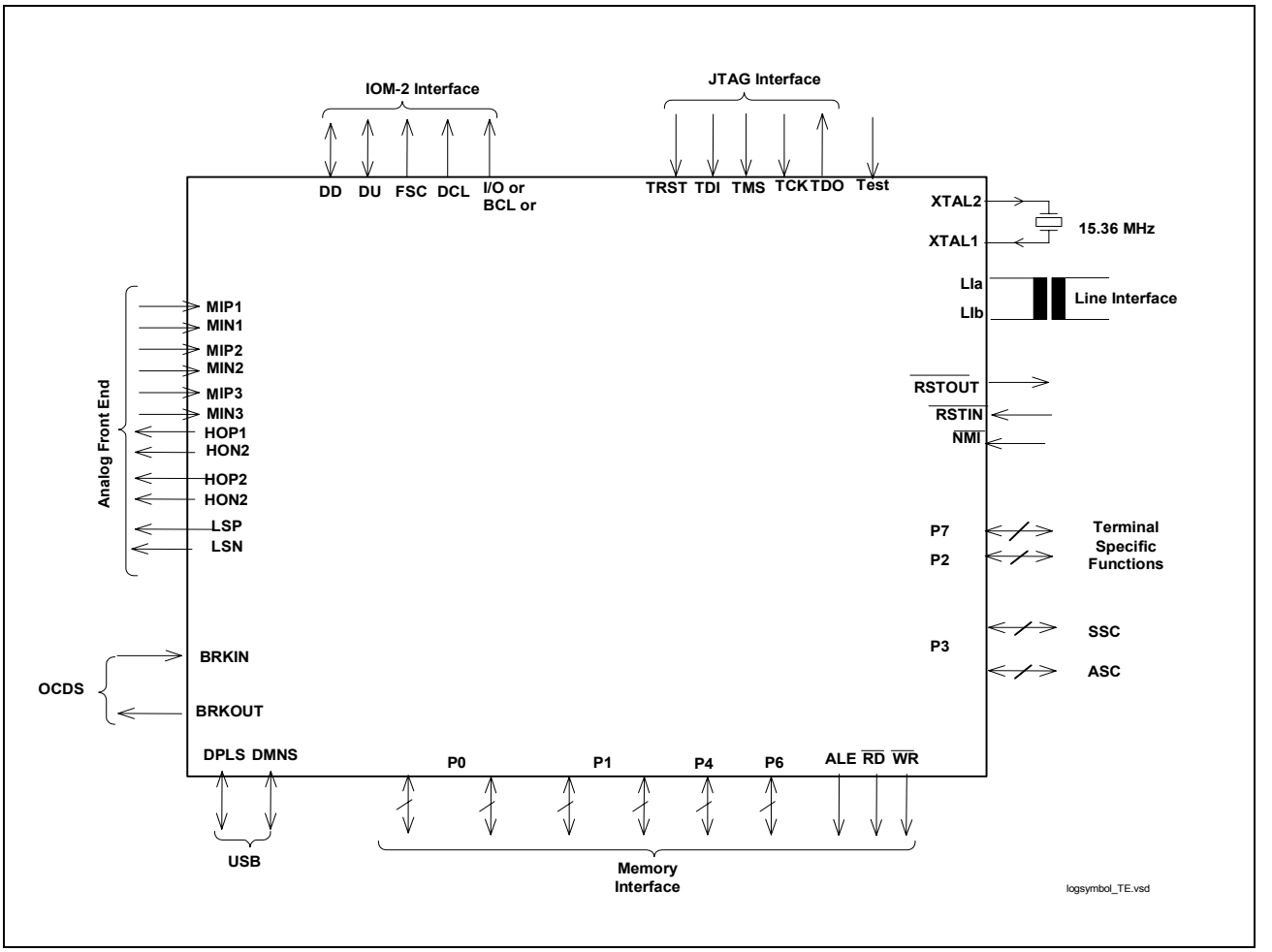



**Figure 1-1 Logical Symbol TE mode**

## 1.3 Typical Application

The following figure illustrates the typical application in which the **INCA-D** is usually used.

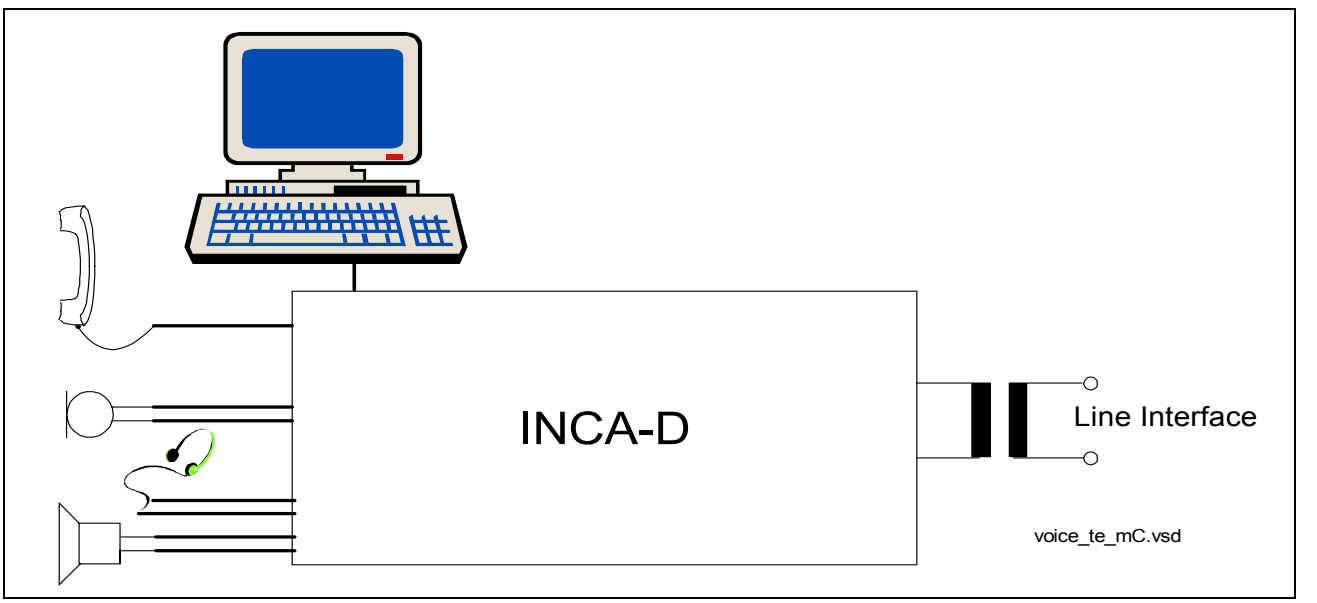



**Figure 1-2 Basic Configuration**

# 2 Pin Descriptions

## 2.1 Pin Configuration

The pin configuration of the INCA-D is shown in figure 2-1.

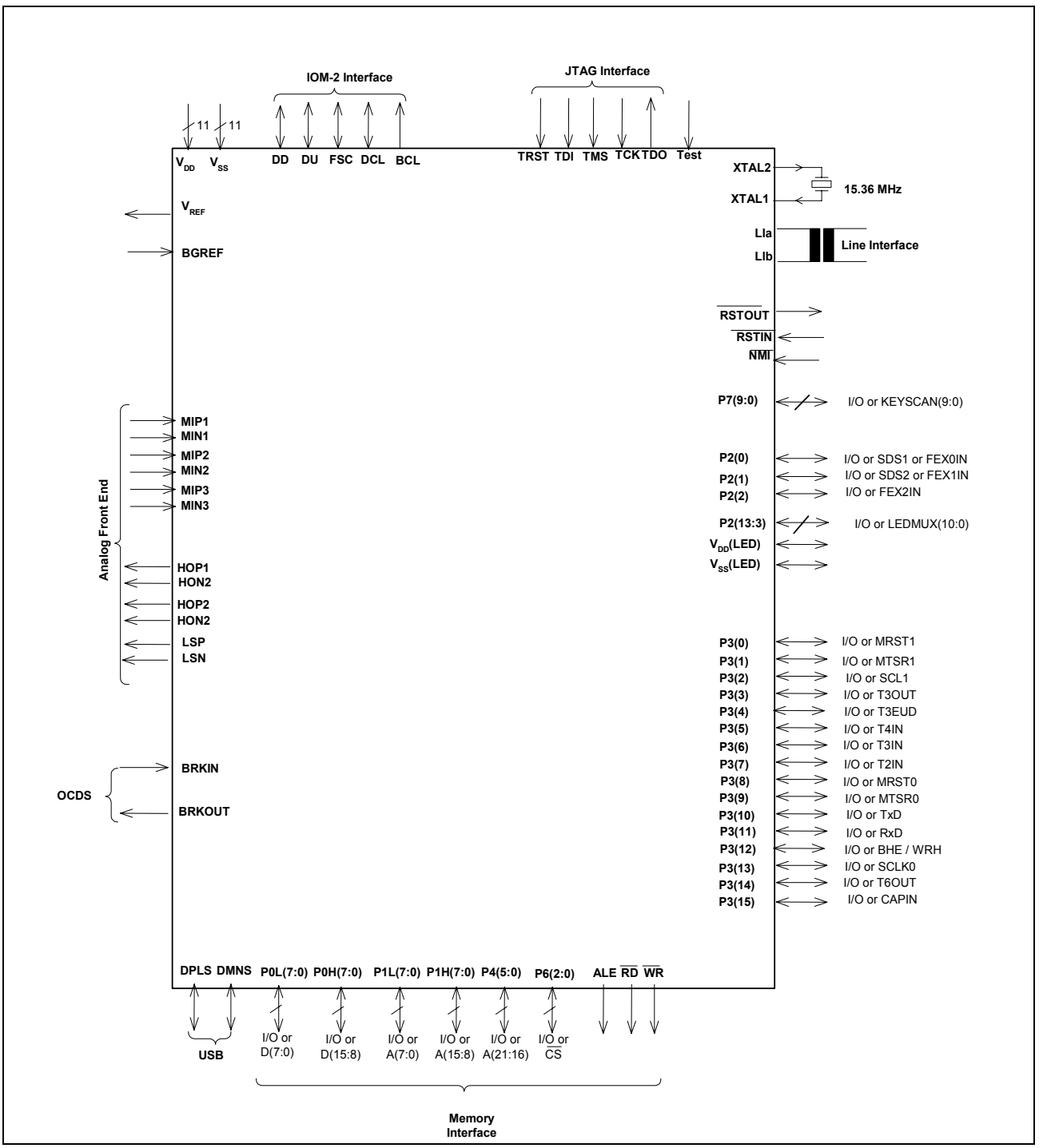



Figure 2-1 Pin Configuration

The mapping of the pin configuration to the physical device is shown in figure 2-2.

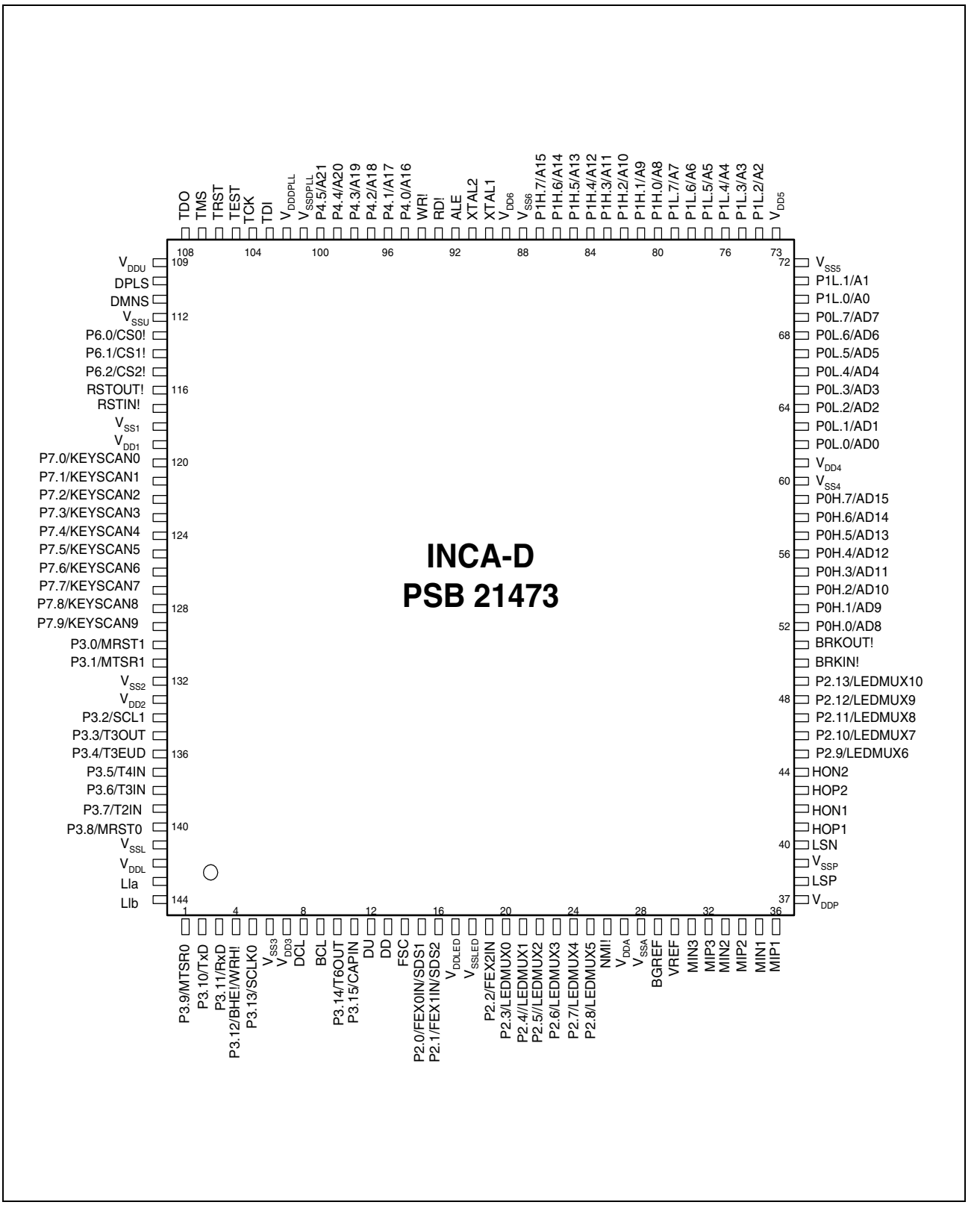



**Figure 2-2 Mapping of pins to physical device**

## 2.2 Pin Definitions and Functions

**Table 2-1 Memory Interface and Control Signals**

| Pin No. | Symbol | Input (I) Output (O) Open Drain (OD | Function |
|---|---|---|---|
| 62-69<br>52-59 | **PORT0**<br>P0L.0-P0L.7:<br>P0H.0-P0H.7: | I/O (OD) | PORT0 consists of the two 8-bit bidirectional I/O ports POL and POH. It is bitwise programmable for input or output via direction bits. It contains internal pull resistors.<br>For external memory access, PORT0 serves as the data (D) bus in demultiplexed bus modes.<br>Beside these functions, P0 serves for latching in the start-up configuration during reset. |
| 70, 71, 74-79<br>80-87 | **PORT1**<br>P1L.0-P1L.7<br>P1H.0-P1H.7 | I/O (OD) | PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bitwise programmable for input or output via direction bits. It contains internal pull resistors.<br>For external memory access PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes. |
| 95<br>...<br>100 | **PORT4**<br>P4.0-P4.5 | I/O (OD)<br>O<br>...<br>O | PORT4 is a 6-bit bidirectional I/O port. It is bitwise programmable for input or output via direction bits. It contains internal pull resistors.<br>For external memory access Port4 can be used to output the segment address lines:<br>P4.0 A16 : Least Significant Segment Address Line<br>...<br>P4.5 A21: Most Significant Segment Address Line |
| 113<br>114<br>115 | **PORT6**<br>P6.0 - P6.2 | I/O, (OD)<br>O<br>O<br>O | PORT6 is a 3-bit bidirectional I/O port. It is bitwise programmable for input or output via direction bits. It contains internal pull resistors.<br>P6.0 $\overline{CS0}$ Chip Select 0<br>P6.1 $\overline{CS1}$ Chip Select 1<br>P6.2 CS2 Chip Select 2 |

**Table 2-1 Memory Interface and Control Signals** (cont'd)

| Pin No. | Symbol | Input (I) Output (O) Open Drain (OD | Function |
|---|---|---|---|
| 93 | $\overline{RD}$ | O | External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access. (internal pull-up provided) |
| 94 | $\overline{WR}$/$\overline{WRL}$ | O | External Memory Write Strobe. In $\overline{WR}$ mode this pin is activated for every external data write access. In $\overline{WRL}$ mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection. (internal pull-up provided) |
| 92 | ALE | O | Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes. (internal pull-down provided) |

**Table 2-2 Serial Interfaces,Terminal Specific Functions**

| Pin No. | Symbol | Input (I) Output (O) Open Drain (OD) | Function |
|---|---|---|---|
| | **PORT3** P3.0 - P3.15 | I/O (OD possible at all pins) | PORT3 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits and it contains internal pull resistors.<br><br>The following PORT3 pins serve for alternate functions:<br>P3.0 MRST1 Master Receive Slave Transmit |
| 130 | | I/O | SSC1 / T5IN Timer 5 Input<br>P3.1 MTSR1 Master Transmit Slave Receive |
| 131 | | I/O | SSC1 / T4EUD Timer 4 External Up Down<br>P3.2 SCLK1 Shift Clock SSC1 / T2EUD Timer 2 External Up Down |
| 134 | | I/O | P3.3 T3OUT Timer T3 Toggle Latch Output<br>P3.4 T3EUD Timer T3 External Up Down |
| 135 | | O | P3.5 T4IN Timer T4 Input |
| 136 | | I | P3.6 T3IN Timer T3 Input |
| 137 | | I | P3.7 T2IN Timer T2 Input |
| 138 | | I | P3.8 MRST0 Master Receive Slave Transmit |
| 139 | | I | SSC0 / T6IN Timer 6 Input |
| 140 | | I/O | P3.9 MTSR0 Master Transmit Slave Receive<br>SSC0 / T5EUD Timer T5 External Up Down |
| 1 | | I/O | P3.10 TxD ASC Data transmit<br>P3.11 $\overline{\text{RxD}}$ ASC Data receive<br>P3.12 $\overline{\text{BHE}}$ External Memory High Byte Enable |
| 2 | | O | Signal $\overline{\text{WRH}}$ External Memory High Byte Write |
| 3 | | I/O | Strobe |
| 4 | | O | P3.13 SCLK0 Shift Clock SSC0 / T6EUD Timer 6 External Up Down<br>P3.14 T6OUT Timer 6 output |
| 5 | | O/I | P3.15 CAPIN GPT2 Capture Input |
| 10 | | O | |
| 11 | | I | |

**Table 2-2 Serial Interfaces,Terminal Specific Functions** (cont'd)

| Pin No. | Symbol | Input (I) Output (O) Open Drain (OD) | Function |
|---|---|---|---|
| | **PORT7** P7.0 - P7.9 | I/O (OD) | PORT7 is an 10-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. It contains internal pull resistors. As alternate function the following pins are used by the keyscanner P7.0 Keyscan of line 0 |
| 120 | | I/O | P7.1Keyscan of line 1 |
| 121 | | I/O | P7.2 Keyscan of line 2 |
| 122 | | I/O | P7.3Keyscan of line 3 |
| 123 | | I/O | P7.4 Keyscan of line 4 |
| 124 | | I/O | P7.5 Keyscan of line 5 |
| 125 | | I/O | P7.6 Keyscan of line 6 |
| 126 | | I/O | P7.7 Keyscan of line 7 |
| 127 | | I/O | P7.8 Keyscan of line 8 |
| 128 | | I/O | P7.9 Keyscan of line 9 |
| 129 | | I/O | |
| | **PORT2** P2.0- P2.13 | I/O (OD) | PORT2 is a 14-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. It contains internal pull resistors. The following pins serve for alternate functions. P2.0 FEX0IN or SDS1 P2.1 FEX1IN or SDS2 |
| 15 | | I/O | P2.2 FEX2IN |
| 16 | | I/O | P2.3 LED multiplexing line 0 |
| 19 | | I/O | P2.4 LED multiplexing line 1 |
| 20 | | O | P2.5 LED multiplexing line 2 |
| 21 | | O | P2.6 LED multiplexing line 3 |
| 22 | | O | P2.7 LED multiplexing line 4 |
| 23 | | O | P2.8 LED multiplexing line 5 |
| 24 | | O | P2.9 LED multiplexing line 6 |
| 25 | | O | P2.10 LED multiplexing line 7 |
| 45 | | O | P2.11 LED multiplexing line 8 |
| 46 | | O | P2.12 LED multiplexing line 9 |
| 47 | | O | P2.13 LED multiplexing line 10 |
| 48 | | O | |
| 49 | | O | |