Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Data Sheet, DS1, Jan. 2003

ISAC-SX TE

ISDN Subscriber Access Controller for Terminals

PSB 3186, V 1.4

Wired Communications

Infineon technologies

Never stop thinking.

Edition 2003-01-30

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
81669 München, Germany

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (**www.infineon.com**).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Data Sheet

Revision History:	**2003-01-30**	DS1
Previous Version:	Data Sheet, DS1, V1.3, 2000-08-23	

Page	**Subjects (major changes since last revision)**
Chapter 1	Comparison ISAC-S TE/ISAC-SX TE
Chapter 3.3.6.2	S- Transceiver Synchronization New
Chapter 3.3.10	Test Functions extended
Chapter 3.7.1.1	CDA Handler Description extended
Chapter 3.7.5.1	TIC Bus Access Control: Note added
Chapter 5.6	IOM-2 Interface Timing: Explanation added
Chapter 5.7.2	Parallel Microcontroller Interface Timing: Explanation added
Chapter 5.9	S-Transceiver
Chapter 5.10	Recommended Transformer Specification: Changed
Chapter 5.11	Line Overload Protection added
Chapter 5.12	EMC/ESD added

Table of Contents **Page**

Table of Contents **Page**

Table of Contents **Page**

Table of Contents **Page**

List of Figures

List of Figures

List of Tables

Page

1 Overview

The ISDN Subscriber Access Controller for Terminals ISAC-SX TE integrates a D-channel HDLC controller and a four wire S/T interface used to link voice/data terminals to the ISDN. It is based on the ISAC-S TE PSB 2186, and provides enhanced features and functionality.

The system integration is simplified by several configurations of the parallel microcontroller interface selected via pin strapping. They include multiplexed and demultiplexed interface selection as well as the optional indirect register access mechanism which reduces the number of necessary registers in the address space to 2 locations. The ISAC-SX TE also provides a serial control interface (SCI).

The FIFO size of the cyclic D-channel buffer is 64 bytes per direction with programmable block size (threshold). The S-transceiver supports terminals mode (TE), activation/ deactivation, timing recovery and D-channel access control and priority control.

One LED output which is capable to indicate the activation status of the S-interface automatically or can be programmed by the host.

The ISAC-SX TE is produced in advanced CMOS technology.

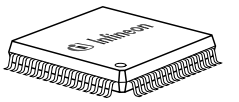
Table 1 Comparison of the ISAC-SX TE with the previous version ISAC-S TE:

	ISAC-SX TE PSB 3186	ISAC-S TE PSB 2186
Operating modes	TE	TE
Supply voltage	3.3 V ± 5%	5 V ± 5%
Technology	CMOS	CMOS
Package	P-MQFP-64 / P-TQFP-64	P-MQFP-64 / P-LCC-44 / P-DIP-40
Transceiver Transformer ratio for the transmitter receiver	 1:1 1:1	 2:1 2:1
Test Functions	- Dig. loop via Layer 2 (TLP) - Layer 1 disable (DIS_TR) - Analog loop (LP_A- bit EXLP- bit, ARL)	- Dig. loop via Layer 2(TLP) - Layer 1 disable (DIS_TR) - Analog loop (ARL)
Microcontroller Interface	Serial interface (SCI) 8-bit parallel interface: Motorola Mux Siemens/Intel Mux Siemens/Intel Non-Mux direct/ indirect Addressing	Not provided 8-bit parallel interface: Motorola Mux Siemens/Intel Mux Siemens/Intel Non-Mux
Command structure of the register access (SCI)	Header/address/data	Address/data
Crystal	7.68 MHz	7.68 MHz
Buffered 7.68 MHz output	Provided	Not provided
Controller data access to IOM-2 timeslots	All timeslots; various possibilities of data access	Restricted access to B- and IC-channel
Data control and manipulation	Various possibilities of data control and data manipulation (enable/ disable, shifting, looping, switching)	B- and IC-channel looping

	ISAC-SX TE PSB 3186	ISAC-S TE PSB 2186
IOM-2		
IOM-2 Interface	Double clock (DCL), bit clock pin (BCL), serial data strobe (SDS)	Double clock (DCL), bit clock (BCL), serial data strobe (SDS)
Monitor channel programming	Provided (MON0, 1, 2, ..., 7)	Provided (MON0 or 1)
C/I channels	CI0 (4 bit), CI1 (4/6 bit)	CI0 (4 bit), CI1 (6 bit)
Layer 1 state machine	With changes for correspondence with the actual ITU specification	
Layer 1 state machine in software	Not possible	Not possible
HDLC support	D- and B-channel timeslots; non-auto mode, transparent mode 1-3, extended transparent mode	D-channel timeslot; auto mode, non-auto mode, transparent mode 1-3
D-channel FIFO size	64 bytes cyclic buffer per direction with programmable FIFO thresholds	2x32 bytes buffer per direction
Reset Signals	$\overline{\text{RES}}$ input signal $\overline{\text{RSTO}}$ output signal	RST input/output signal
Reset Sources	$\overline{\text{RES}}$ Input Watchdog C/I Code Change $\overline{\text{EAW}}$ Pin Software Reset	RST Input Watchdog C/I Code Change EAW Pin
Interrupt Output Signals	$\overline{\text{INT}}$ low active (open drain) by default, reprogrammable to high active (push-pull)	Low active $\overline{\text{INT}}$
Pin SCLK	1.536 MHz	512 kHz

V 1.4

1.1 Features



P-MQFP-64-1

P-TQFP-64-1

- Full duplex 2B + D S/T interface transceiver according to ITU-T I.430
- Successor of ISAC-S TE PSB 2186 in 3.3 V technology
- 8-bit parallel microcontroller interface, Motorola and Siemens/Intel bus type multiplexed or non-multiplexed, direct-/indirect register addressing
- Serial control interface (SCI)
- Microcontroller access to all IOM-2 timeslots
- Various types of protocol support (Non-auto mode, transparent mode, extended transparent mode)
- D-channel HDLC controller with 2 x 64 byte FIFOs
- IOM-2 interface in TE mode, single/double clocks
- One serial data strobe signal (SDS)
- Monitor channel handler (master/slave)
- IOM-2 MONITOR and C/I-channel protocol to control peripheral devices
- Conversion of the frame structure between the S/T-interface and IOM-2
- Receive timing recovery
- D-channel access control
- Activation and deactivation procedures with automatic activation from power down state
- Access to S and Q bits of S/T-interface
- Adaptively switched receive thresholds
- Two programmable timers
- Watchdog timer
- Software Reset

Type	Package
PSB 3186 H	P-MQFP-64-1
PSB 3186 F	P-TQFP-64-1

- One LED pin automatically indicating layer 1 activated state
- Test loops
- Sophisticated power management for restricted power mode
- Power supply 3.3 V
- 3.3 V output drivers, inputs are 5 V safe
- Advanced CMOS technology

1.2 Logic Symbol

The logic symbol gives an overview of the ISAC-SX TE functions.

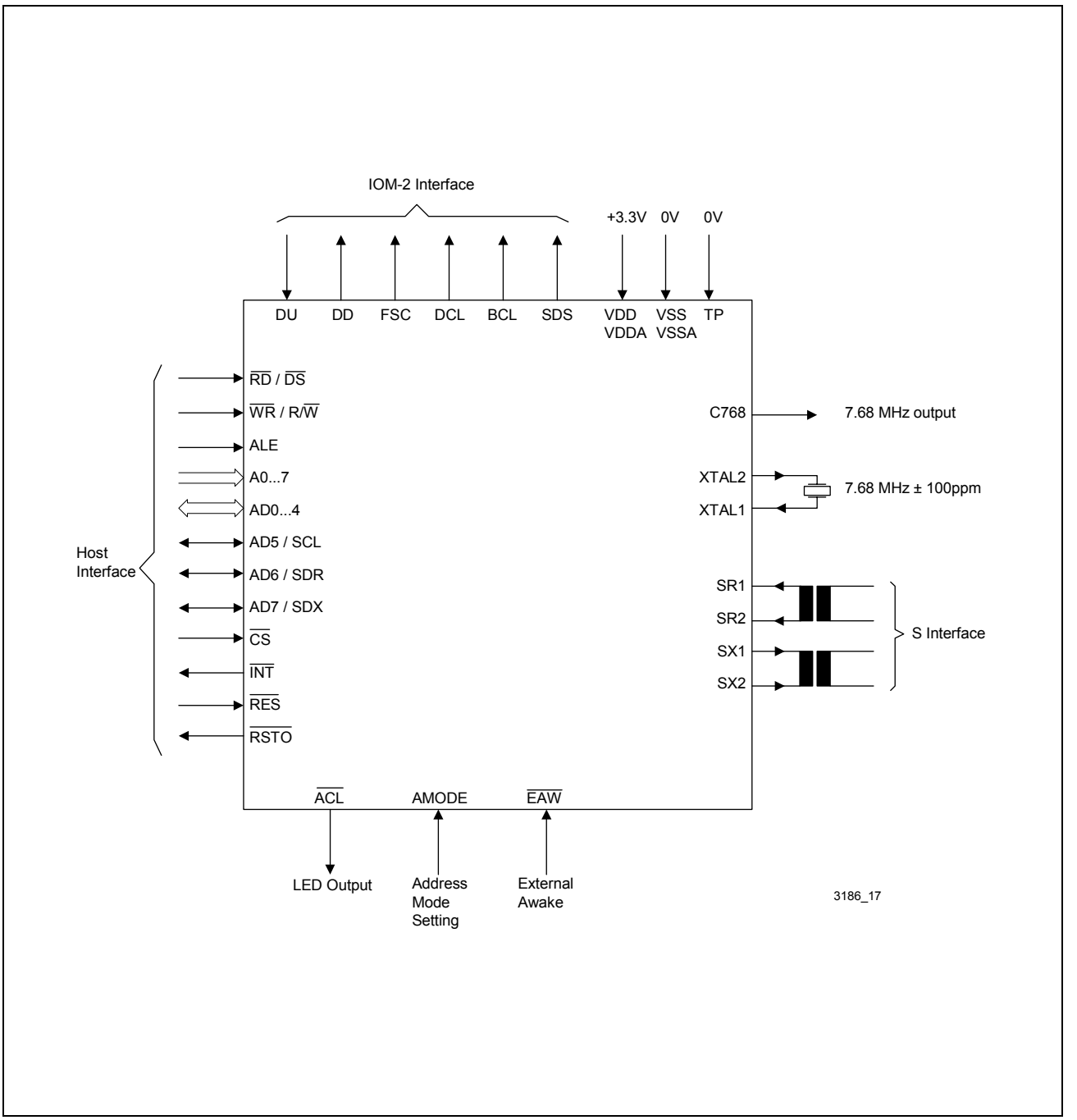


Figure 1 Logic Symbol of the ISAC-SX TE

1.3 Typical Applications

The ISAC-SX TE is designed for the user area of the ISDN basic access, especially for subscriber terminal equipment with S interface.
Figure 2 illustrates the general application fields of the ISAC-SX TE.

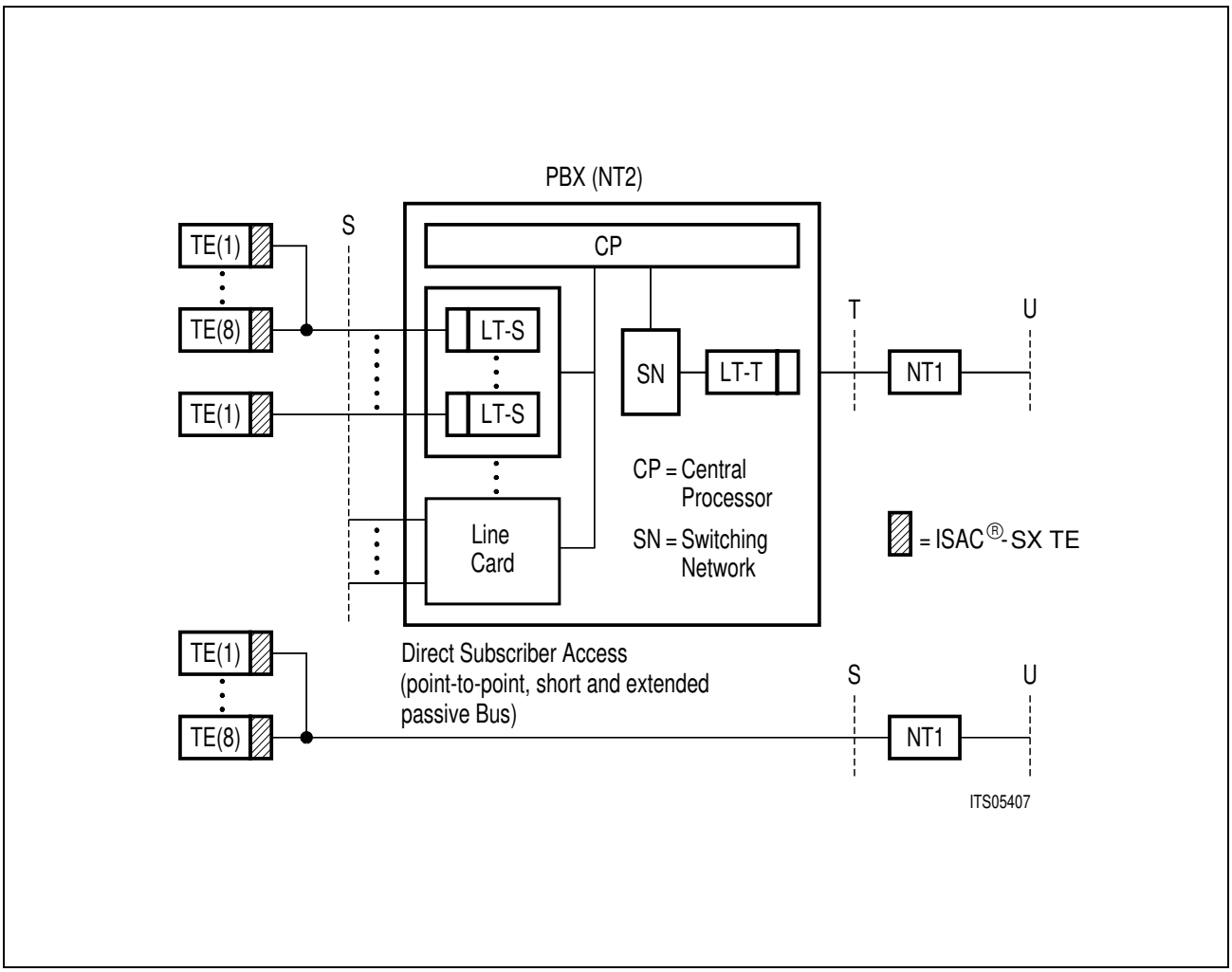


Figure 2 Applications of the ISAC-SX TE

2 Pin Configuration

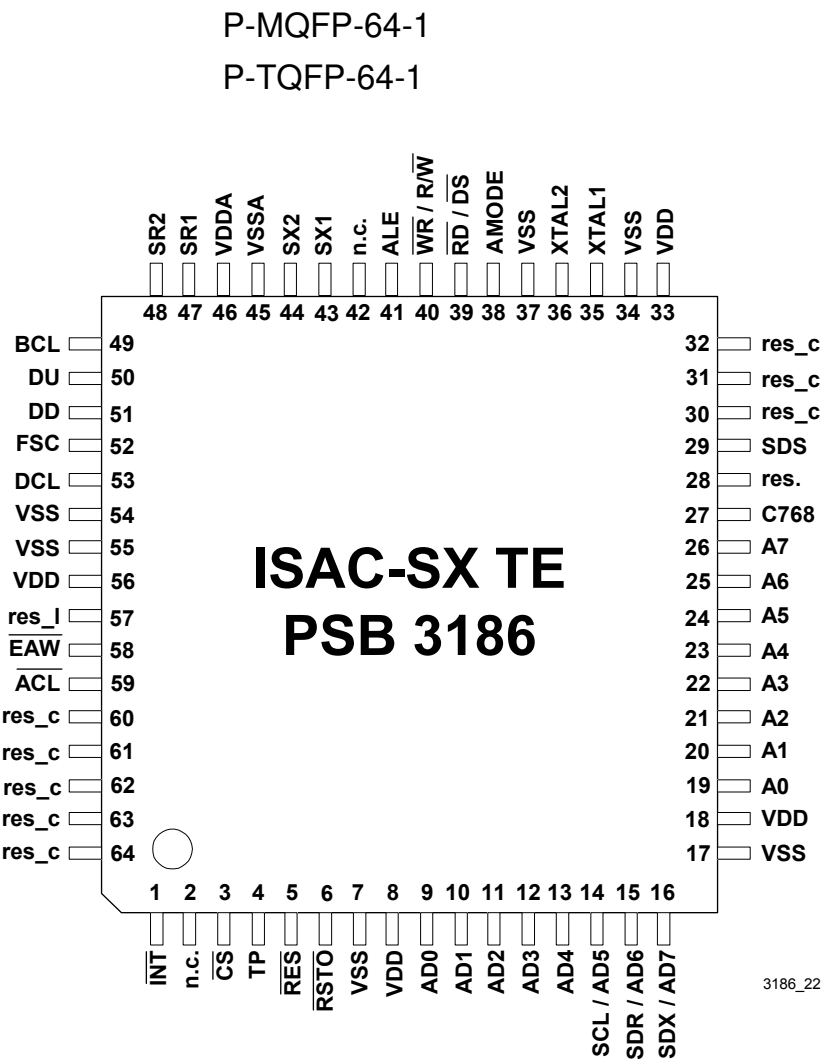


Figure 3 Pin Configuration of the ISAC-SX TE

Table 2 ISAC-SX TE Pin Definitions and Functions

Pin No. MQFP-64 TQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
Host Interface			
19 20 21 22 23 24 25 26	A0 A1 A2 A3 A4 A5 A6 A7	I I I I I I I I	• **Non-Multiplexed Bus Mode:** **Address Bus** Address bus transfers addresses from the microcontroller to the ISAC-SX TE. For indirect address mode only A0 is valid (A1-A7 to be connected to VDD). • **Multiplexed Bus Mode:** Not used in multiplexed bus mode. In this case A0-A7 should directly be connected to VDD.
9 10 11 12 13	AD0 AD1 AD2 AD3 AD4	I/O I/O I/O I/O I/O	• **Multiplexed Bus Mode:** **Address/data bus** Transfers addresses from the microcontroller to the ISAC-SX TE and data between the microcontroller and the ISAC-SX TE. • **Non-Multiplexed Bus Mode:** **Data bus** Transfers data between the microcontroller and the ISAC-SX TE.
14	AD5	I/O	• **Multiplexed Bus Mode:** **Address/data bus** Address/data line AD5 if the parallel interface is selected. • **Non-Multiplexed Bus Mode:** **Data bus** Data line D5 if the parallel interface is selected.
	SCL	I	**SCI - Serial Clock** Clock signal of the SCI interface if a serial interface is selected.

Table 2 ISAC-SX TE Pin Definitions and Functions (cont'd)

Pin No. MQFP-64 TQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
15	AD6	I/O	• **Multiplexed Bus Mode:** **Address/data bus** Address/data line AD6 if the parallel interface is selected. • **Non-Multiplexed Bus Mode:** **Data bus** Data line D6 if the parallel interface is selected.
	SDR	I	**SCI - Serial Data Receive** Receive data line of the SCI interface if a serial interface is selected.
16	AD7	I/O	• **Multiplexed Bus Mode:** **Address/data bus** Address/data line AD7 if the parallel interface is selected. • **Non-Multiplexed Bus Mode:** **Data bus** Data line D7 if the parallel interface is selected.
	SDX	OD	**SCI - Serial Data Transmit** Transmit data line of the SCI interface if a serial interface is selected.
39	$\overline{RD}$	I	**Read** Indicates a read access to the registers (Siemens/ Intel bus mode).
	$\overline{DS}$	I	**Data Strobe** The rising edge marks the end of a valid read or write operation (Motorola bus mode).
40	$\overline{WR}$	I	**Write** Indicates a write access to the registers (Siemens/ Intel bus mode).
	R/$\overline{W}$	I	**Read/Write** A HIGH identifies a valid host access as a read operation and a LOW identifies a valid host access as a write operation (Motorola bus mode).

Table 2 ISAC-SX TE Pin Definitions and Functions (cont'd)

Pin No. MQFP-64 TQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
41	ALE	I	**Address Latch Enable** A HIGH on this line indicates an address on the external address/data bus (multiplexed bus type only). ALE also selects the microcontroller interface bus type (multiplexed or non multiplexed).
3	$\overline{CS}$	I	**Chip Select** A low level indicates a microcontroller access to the ISAC-SX TE.
1	$\overline{INT}$	OD (O)	**Interrupt Request** $\overline{INT}$ becomes active low (open drain) if the ISAC-SX TE requests an interrupt. The polarity can be reprogrammed to high active with push-pull characteristic.
5	$\overline{RES}$	I	**Reset** A LOW on this input forces the ISAC-SX TE into a reset state.
38	AMODE	I	**Address Mode** Selects between direct (0) and indirect (1) register access mode.
IOM-2 Interface			
52	FSC	O	**Frame Sync** 8-kHz frame synchronization signal.
53	DCL	O	**Data Clock** IOM-2 interface data clock signal 1.536 MHz (double bit clock).
49	BCL	O	**Bit Clock** IOM-2 interface bit clock signal 768 kHz (single bit clock).
51	DD	O (OD)	**Data Downstream** IOM-2 data signal in downstream direction.

Table 2 ISAC-SX TE Pin Definitions and Functions (cont'd)

Pin No. MQFP-64 TQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
50	DU	I	**Data Upstream** IOM-2 data signal in upstream direction.
29	SDS	O	**Serial Data Strobe** Programmable strobe signal for time slot and/or D-channel indication on IOM-2.
Miscellaneous			
43 44	SX1 SX2	O O	**S-Bus Transmitter Output (positive)** **S-Bus Transmitter Output (negative)**
47 48	SR1 SR2	I I	**S-Bus Receiver Input** **S-Bus Receiver Input**
35 36	XTAL1 XTAL2	I O	**Crystal 1** Connection for a crystal or used as external clock input. 7.68 MHz clock or crystal required. **Crystal 2** Connection for a crystal. Not connected if an external clock is supplied to XTAL1.
58	$\overline{\text{EAW}}$	I	**External Awake** If a falling edge on this input is detected, the ISAC-SX TE generates an interrupt and, if enabled, a reset pulse.
59	$\overline{\text{ACL}}$	O	**Activation LED** This pin can either function as a programmable output or it can automatically indicate the activated state of the S interface by a logic '0'. An LED with pre-resistance may directly be connected to $\overline{\text{ACL}}$.
27	C768	O	**Clock Output** A 7.68 MHz clock is output to support other devices. This clock is not synchronous to the S interface.
6	$\overline{\text{RSTO}}$	OD	**Reset Output** Low active reset output, either from a watchdog timeout or programmed by the host.

Table 2 ISAC-SX TE Pin Definitions and Functions (cont'd)

Pin No. MQFP-64 TQFP-64	Symbol	Input (I) Output (O) Open Drain (OD)	Function
4	TP	I	**Test Pin** Must be connected to V_{SS}.
2, 42	n.c.	I	**not connected**
28	res.		**reserved** This pin is reserved and should be left not connected.
57	res_l	I	**reserved, connect LOW** This pin is reserved and must be connected to V_{SS}.
30, 31, 32, 60, 61, 62, 63, 64	res_c	I	**reserved, connect HIGH or LOW** These pins are reserved and must be connected either to V_{SS} or V_{DD}.
Power Supply			
8, 18, 33, 56	V_{DD}	–	**Digital Power Supply Voltage** (3.3 V ± 5 %)
46	V_{DDA}	–	**Analog Power Supply Voltage** (3.3 V ± 5 %)
7, 17, 34, 37, 54, 55	V_{SS}	–	**Digital ground** (0 V)
45	V_{SSA}	–	**Analog ground** (0 V)

3 Description of Functional Blocks

3.1 General Functions and Device Architecture

Figure 4 shows the architecture of the ISAC-SX TE containing the following functions:

- S/T-interface transceiver supporting TE mode
- Different host interface modes:
  - Parallel microcontroller interface
    (Siemens/Intel multiplexed, Siemens/Intel non multiplexed, Motorola modes)
  - Serial Control Interface (SCI)
- Optional indirect register address mode reduces number of registers to be accessed to two locations
- One D-channel HDLC-controller with 64 byte FIFOs per direction with programmable FIFO block size (threshold) of 4, 8, 16 or 32 byte (receive) and 16 or 32 byte (transmit).
- IOM-2 interface for terminal mode (TE)
- One serial data strobe signals (SDS)
- IOM handler with controller data access registers (CDA) allows flexible access to IOM timeslots for reading/writing, looping and shifting data
- Synchronous transfer interrupts (STI) allow controlled access to IOM timeslots
- MONITOR channel handler on IOM-2 for master mode, slave mode or data exchange
- C/I-channel handler and TIC bus access controller
- D-channel access mechanism
- LED connected to pin $\overline{\text{ACL}}$ indicates S-interface activation status automatically or can be controlled by the host
- Level detect circuit on the S interface reduces power consumption in power down mode
- Two timers for periodic or single interrupts (periods between 1 ms and 14.336 s)
- Clock and timing generation
- Digital PLL to synchronize the transceiver to the S/T interface
- Buffered 7.68 MHz oscillator clock output allows connection of further devices and saves another crystal on the system board
- Reset generation (watchdog timer)