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SIEMENS

ICs for Communications

Audio Ringing Codec Filter
Featuring Speakerphone Function
ARCOFI®-SP
PSB 2163

User's Manual

SIEMENS

ICs for Communications

Audio Ringing Codec Filter
Featuring Speakerphone Function

ARCOFI®-SP
PSB 2163

User's Manual 06.95

PSB 2163 **Revision History:**	**Current Version 06.95**
Previous Version:	02.94
Page	Subjects (changes since last revision)
108	Absolute Maximum Ratings
108	DC Characteristics
110	Analog Front End Characteristics
111	Transmission Characteristics Test Conditions corrected Addition of Overall Programming Range
112	IOM®-2 Bus Timing Specification of Jitter Timing

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about **"Processing Guidelines"** and **"Quality Assurance"** for ICs, see our **"Product Overview"**.

Contents **Page**

Contents (cont'd) **Page**

Introduction

The PSB 2163 ARCOFI®-SP provides the subscriber with an optimized Audio, Ringing, Codec, Filter processor solution for a digital telephone. It fulfills all the necessary requirements for the completion of a low-cost digital telephone.

Please note: Throughout this whole document "ARCOFI®" refers to ARCOFI®-SP PSB 2163.

The ARCOFI performs all coding, decoding and filtering functions according to the CCITT and ETSI (NET33) norms.

Full featured applications are possible without any external elements. All the necessary hardware and software is implemented. In addition the ARCOFI offers a speakerphone and monitoring function. This feature is completely digitally implemented in the chip.

Two transducer correction filters (one for each direction) can be programmed to correct the analog transducer frequency characteristics.

The ARCOFI provides a universal DTMF, tone and ringing generator for the receive direction. The signal forms available are DTMF, square, trapezoid and sine wave. Complex signal sequences are made possible by a control generator (e.g. pulsed three tone call in conjunction with the beat generator).

A DTMF-generator for the transmit direction is also available. If the transmit DTMF-generator is active, only a part of the receive tone generator function is possible.

This flexible tone generator concept fulfills a wide range of applications.

The interfacing to a handset mouth and earpiece is facilitated by a flexible analog front end. A loudspeaker output has also been integrated on the chip as well as a secondary input for a handsfree microphone. All analog inputs and outputs are gain programmable through software.

At the digital side an ISDN-Oriented Modular (IOM®-2) interface for terminal (TE) and non-terminal (non-TE) applications or a Serial Control/Data Interface (SCI & SDI) is realized to connect layer-1/2 devices to the ARCOFI.

The ARCOFI is a BICMOS-device, available in a P-DIP-28, P-LCC-28-R or P-DSO-28 package. It operates from a single + 5 V supply and features a power-down state with very low power consumption.

Comparison between PSB 2163 and PSB 2165

Table of main differences:

PSB 2163	PSB 2165	Comment
1-µ BICMOS technology	2-µ CMOS technology	
P-DSO-28		
	SLD-interface	
Non-TE IOM-2 interface		
Serial Control/Data Interface		
One receive channel	Two receive channels	
Digital high-pass in receive direction		
AGC in receive direction	LGA (programmable gain stage) in receive direction	
Sidetone gain stage GZ with higher resolution (two byte coefficient)	GZ with one byte coefficient	
Optimized speakerphone function		Extended coefficient space is necessary
Microphone amplifier with additional 36-dB and 42-dB gain stages		
Controlled monitoring with fixed attenuation	Controlled monitoring with programmable attenuation	
Ringing directly via loudspeaker with square-wave in 3-dB steps	Ringing via loudspeaker over the second receive path	
Tone generation unit can be switched to transmit path and added to transmit speech signals		
Additional test loops	CCITT G.714	
ETSI (NET33) & CCITT G.714		

Table of Symbols

AD	Address of the ARCOFI (IOM-2 mode)
A/D	Analog to Digital converter
ADI	ARCOFI Digital Interface
AFE	Analog Front End
AGCX	Automatic Gain Control Transmit
AGCR	Automatic Gain Control Receive
AHO	Handset Output Amplifier
AIMX	Analog Input Multiplexer control bits (ATCR)
ALC	Analog Loop via Converter (TFCR)
ALF	Analog Loop via Front End (TFCR)
ALI	Analog Loop via Interface (TFCR)
ALN	Analog Loop via Noise Shaper (TFCR)
ALS	Loudspeaker Amplifier
ALTF	Analog Loop & Test Function bits (TFCR)
ALZ	Analog Loop via Z-side tone gain stage
AMI	Microphone Amplifier
ARCOFI	Audio Ringing Codec Filter
ASP	ARCOFI Signal Processor
BM	Beat Mode bit (TGCR)
BT	Beat Tone bit (TGCR)
CAM	Chip Address Mode bit (IOM-2 two chip mode; GCR)
CCITT	International Telegraph and Telephone Consultative Committee
CG	Control Generator bit (TGCR)
CMDR	Command Register
COP	Coefficient Operation (CMDR)
CR	Configuration Register
CRAM	Coefficient RAM
$\overline{\text{CS}}$	Chip Select active low (serial control interface)
D/A	Digital to Analog converter
DCE	Double Clock Enable at DCLK pin (SDICR)
DCL	IOM-2 interface clock
DCLK	Data Clock pin (serial data interface)
DD	IOM-2 Data Downstream pin
DEC	Decimation filter
DHON	Disable pin HON (XCR)
DHOP	Disable pin HOP (XCR)
DHPR	Disable High Pass Receive bit (PFCR)
DHPX	Disable High Pass Transmit bit (PFCR)
DLN	Digital Loop via Noise Shaper (TFCR)
DLP	Digital Loop via PCM-register (TFCR)

Table of Symbols (cont'd)

DLS	Digital Loop via Signal processor (TFCR)
DLSN	Disable pin LSN (XCR)
DLSP	Disable pin LSP (XCR)
DLTF	Digital Loop & Test Function bits (TFCR)
DR	Data Receive pin (serial data interface)
DRAM	Data RAM
DSP	Digital Signal Processor
DT	Dual Tone bit (TGCR)
DTMF	Dual Tone Multi Frequency bit (TGSR)
DU	IOM-2 Data Upstream pin
DX	Data Transmit pin (serial data interface)
EP0	Earpiece
EPP0	Enable Push-Pull at pin DU/DX (SDICR)
EPP1	Enable Push-Pull at pin SA/SDX (SDICR)
EPZST	Enable PZ1/PZ2 to output internal Status conditions (TFCR)
ETF	Enable Tone Filter bit (TGCR)
ETSI	European Telecommunications Standards Institute
EVX	Enable Voice Transmit bit (GCR)
EVREF	Enable VREF buffer bit (ATCR)
EWDF	Electrical Wave Digital Filter
FR	Frequency correction Receive bit (PFCR)
FSC	IOM-2 and SDI-Frame Synchronization pin (8 kHz)
FX	Frequency correction Transmit bit (PFCR)
GR	Receive Gain bit (PFCR); Receive gain stage
GX	Transmit Gain bit (PFCR); Transmit gain stage
GZ	Z-side tone Gain bit (PFCR); Z-side tone Gain stage
HO	Handset Output
HOC	Handset Output Control bits (ARCR)
HON	Handset earpiece Output – pin
HOP	Handset earpiece Output + pin
IDENT	Identification Code
IDR	Initialize Data RAM (TFCR)
INT	Interpolation filter
IOM	ISDN-Oriented Modular
ISDN	Integrated Services Digital Network

Table of Symbols (cont'd)

LAW	A-Law/μ-Law bit (GCR)
LIN	Linear data mode (VDM; DFICR)
LS	Loudspeaker
LSC	Loudspeaker Control bits (ARCR)
LSN	Loudspeaker output – pin
LSP	Loudspeaker output + pin
MCLK	Master Clock pin (synchronized system clock)
MCLKR	Master Clock Rate (SDICR)
MI3	Microphone input
MIC	Microphone Control bits (ATCR)
MIN1/2	Microphone inputs – pins
MIP1/2	Microphone inputs + pins
NOP	No Operation (CMDR)
NOT	No Test mode (TFCR)
PABX	Private Automatic Branch Exchange
PCI	Peripheral Control Interface
PCM	Pulse Code Modulation
PM	Piezo Mode; output to digital pins PZ1/PZ2 (TGSR)
POR	Power-On Reset
PU	Power-Up bit (GCR)
RAAR	Read Automatic Attenuation Receive
RCM	Reverse Channel Mode (CMDR)
RS	Reset pin
R/W	Read/Write operation bit (CMDR)
RX	Receive path
SA-SD	PCI I/O pins; I/O-control bits (SDICR)
SCAE	Speech Comparator at the Acoustic Side
SCI	Serial Control Interface
SCLE	Speech Comparator at the Line Side
SCLK	Serial Clock pin (serial control interface)
SDI	Serial Data Interface
SDR	Serial Data Receive pin (serial control interface)
SDX	Serial Data Transmit pin (serial control interface)
SLOT	IOM-2 Slot select for TE mode (GCR)
SM	Stop Mode bit (TGCR)
SOP	Status Operation (CMDR)
SP	Speakerphone enable bit (GCR)

Table of Symbols (cont'd)

SQTR	Square/Trapezoid mode bit (TGCR)
S/T	Square/Trapezoid Generator
TE	Terminal Equipment
TG	Tone Generator bit (TGCR)
TR	Three party conferencing (VDM; DFICR)
TRL	Tone Ringing via Loudspeaker (TGSR)
TRR	Tone Ringing Receive bit (TGSR)
TRX	Tone Ringing Transmit bit (TGSR)
TS	Time-Slot Selection in SDI-mode (TSCR)
TX	Transmit path
V_{DD}	Voltage supply (+ 5 V)
V_{DDP}	Analog Voltage supply for Power amplifiers (+ 5 V)
VDM	Voice Data Manipulation bits (DFICR)
V_{REF}	Reference Voltage output pin
V_{SSA}	Analog ground (0 V)
V_{SSD}	Digital ground (0 V)
V_{SSP}	Analog ground for Power amplifiers (0 V)
WDF	Wave Digital Filter
XOP	Extended Operation (CMDR)

SIEMENS

Audio Ringing Codec Filter Featuring Speakerphone Function (ARCOFI®-SP)

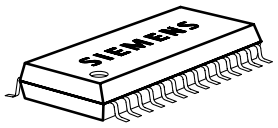
PSB 2163

Preliminary Data

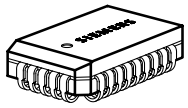
BICMOS-IC

1 Features

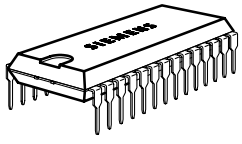
- Applications in digital terminal equipment featuring voice functions
- Digital signal processing performs all CODEC functions
- Fully compatible to the G. 714 CCITT and ETSI (NET33) specification
- PCM A-Law/μ-Law (G. 711 CCITT) and 16-bit linear data
- Flexible configuration of all internal functions
- IOM-2 interface (TE- and non-TE-mode), Serial Control Interface (SCI) and Serial Data Interface (SDI)
- Three analog inputs for the microphone in the handset, the speakerphone and the headset
- Two differential outputs for a handset earpiece (200 Ω) and a loudspeaker (50 Ω)
- 100-mW sine wave and 200-mW square wave loudspeaker driver capability
- Separate digital output for a piezo ringer
- Flexible Peripheral Control Interface (PCI) in IOM-2 TE-mode
- Flexible test and maintenance loopbacks in the analog front end and the digital signal processor
- Independent gain programmable amplifiers for all analog inputs and outputs
- Full digital speakerphone and monitoring support without any external components (speakerphone test and optimization function is available)
- Two transducer correction filters
- Side tone gain adjustment
- Flexible DTMF, tone and ringing generator
- Single 5-V power supply
- Low power consumption: standby 1 mW, operating consumption is dependent on the selected operating mode
- Advanced 1-μ BICMOS technology



P-DSO-28



P-LCC-28-R



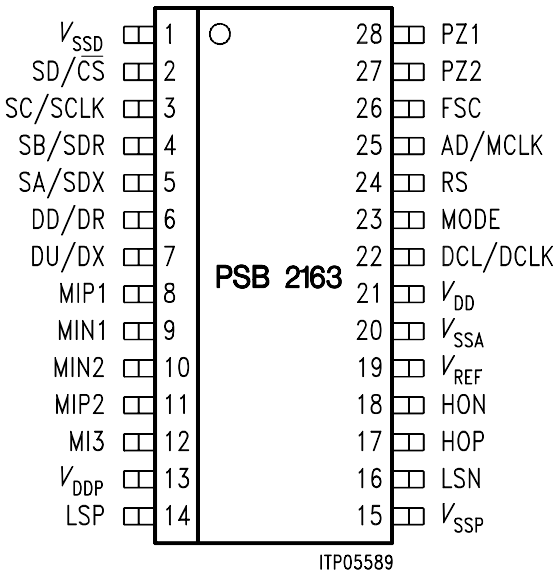
P-DIP-28

Type	Ordering Code	Package
PSB 2163-T	Q67100-H6458	P-DSO-28 (SMD)
PSB 2163-N	Q67100-H6348	P-LCC-28-R (SMD)
PSB 2163-P	Q67100-H6460	P-DIP-28

Pin Configurations

(top view)

P-DSO-28



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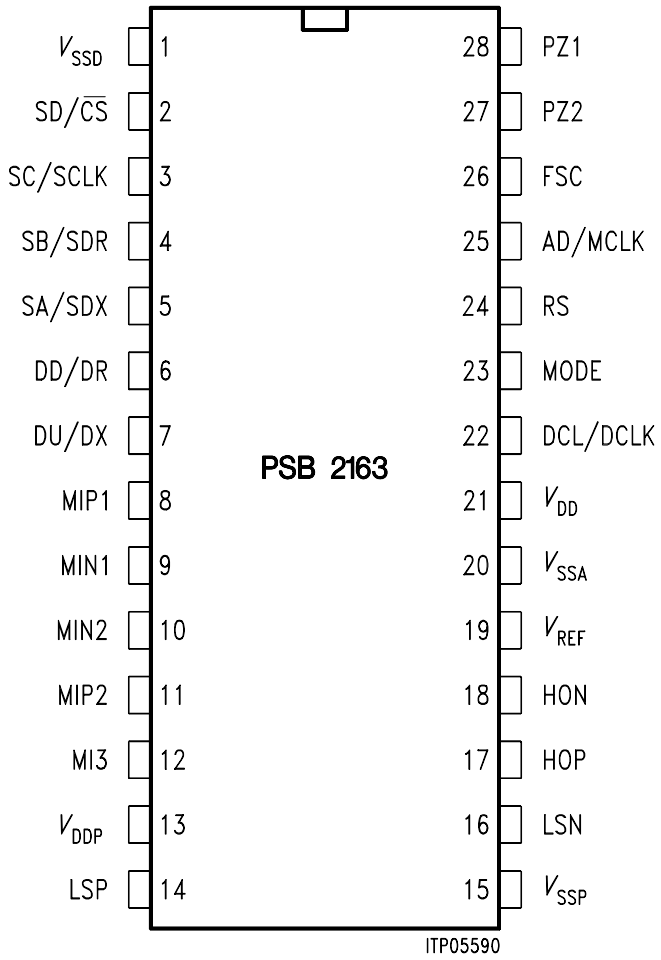
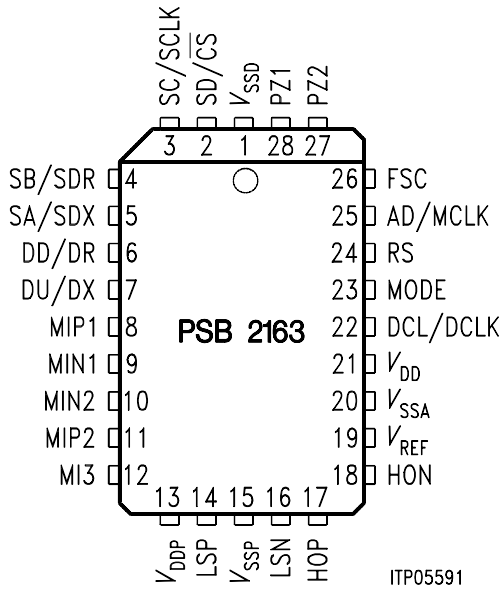


P-LCC-28-R



1.1 Pin Definitions and Functions

Pin No. P-DSO P-LCC P-DIP	Symbol	Input (I) Output (O) Open Drain (OD)	Function
21	V_{DD}	—	Power supply (5 V ± 5 %)
13	V_{DDP}	—	Power supply (5 V ± 5 %)
1	V_{SSD}	—	Digital Ground (0 V)
20	V_{SSA}	—	Analog Ground (0 V)
15	V_{SSP}	—	Analog Ground (0 V)
23	MODE	I	**Mode Selection:** IOM-2 or serial control/data interface
25	AD	I	**IOM Address:** Chip address in IOM-2 two chip mode
	MCLK	I	**Master Clock:** Synchronous system clock when serial control/data interface is selected
24	RS	I	**Reset:** A high signal on this pin forces the ARCOFI into reset state
26	FSC	I	**Frame Sync:** 8-kHz frame synchronization signal (IOM-2 and SDI-mode)
22	DCL	I	**DCL-System Clock:** 1.536 MHz supplied by the application system clock when IOM-2 mode is selected
	DCLK	I	**DCLK Data Clock:** Data clock of the serial data interface (SDI)
6	DD	I/(OD) [1]	**Data Downstream:** Receive data from layer-1 IOM-2 controlling device
	DR	I	**Data Receive:** Receive data of the serial data interface (SDI)
28	PZ1	O	**Digital Piezo Ringer Output:** When selected the tone ringer is routed to this output (PZ1 & PZ2 are in opposite phases)
27	PZ2	O	

[1] see DD/DU-voice channel swapping (XOP_D)

1.1 Pin Definitions and Functions (cont'd)

Pin No. P-DSO P-LCC P-DIP	Symbol	Input (I) Output (O) Open Drain (OD)	Function
7	DU	OD/I [1]	**Data Upstream:** Transmit data to the layer-1 IOM-2 controlling device
	DX	OD/O [2]	**Data Transmit:** Transmit data of the serial data interface (SDI)
2	SD	IO	**Programmable I/O PCI Pin SD:** This port pin is only available in IOM-2 TE-mode
	$\overline{CS}$	I	**Chip Select:** A low level indicates a microprocessor access to the ARCOFI-serial control interface (SCI)
3	SC	IO	**Programmable I/O PCI Pin SC:** This port pin is only available in IOM-2 TE-mode
	SCLK	I	**Serial Clock:** Clock signal of the serial control interface (SCI)
4	SB	IO	**Programmable I/O PCI Pin SB:** This port pin is only available in IOM-2 TE-mode
	SDR	I	**Serial Data Receive:** Receive data line of the serial control interface (SCI)
5	SA	IO	**Programmable I/O PCI Pin SA:** This port pin is only available in IOM-2 TE-mode
	SDX	OD/O [3]	**Serial Data Transmit:** Transmit data line of the serial control interface (SCI)
19	V_{REF}	O	**2.4 V Output:** Output for biasing analog single ended inputs
8	MIP1	I	**Microphone Input 1:** This highly symmetrical differential input has been designed for commonly used telephone microphones
9	MIN1	I	

[1] see DD/DU-voice channel swapping (XOP_D)
[2] programmable via bit SDICR.EPP0
[3] programmable via bit SDICR.EPP1

1.1 Pin Definitions and Functions (cont'd)

Pin No. P-DSO P-LCC P-DIP	Symbol	Input (I) Output (O) Open Drain (OD)	Function
11 10	MIP2 MIN2	I I	**Microphone Input 2:** This highly symmetrical differential input has been designed for commonly used telephone microphones
12	MI3	I	**Microphone Input 3:** This single-ended input has been designed for commonly used telephone microphones
14 16	LSP LSN	O O	**Loudspeaker Output:** LSP & LSN are differential output pins which can drive a 50-Ω loudspeaker directly; a piezo transducer can also be used for ringing signal instead of the loudspeaker
17 18	HOP HON	O O	**Handset Earpiece Output:** HOP & HON are differential output pins which can drive handset earpiece transducers directly

1.2 Logic Symbol

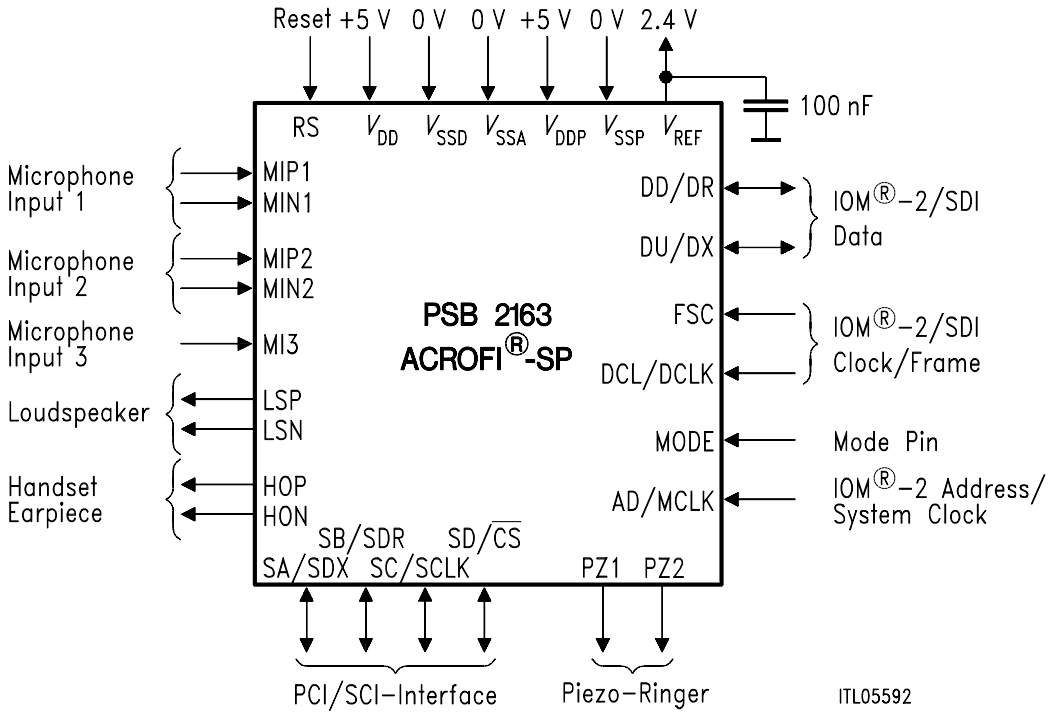


Figure 1
Logic Symbol of the ARCOFI®

1.3 Functional Block Diagram

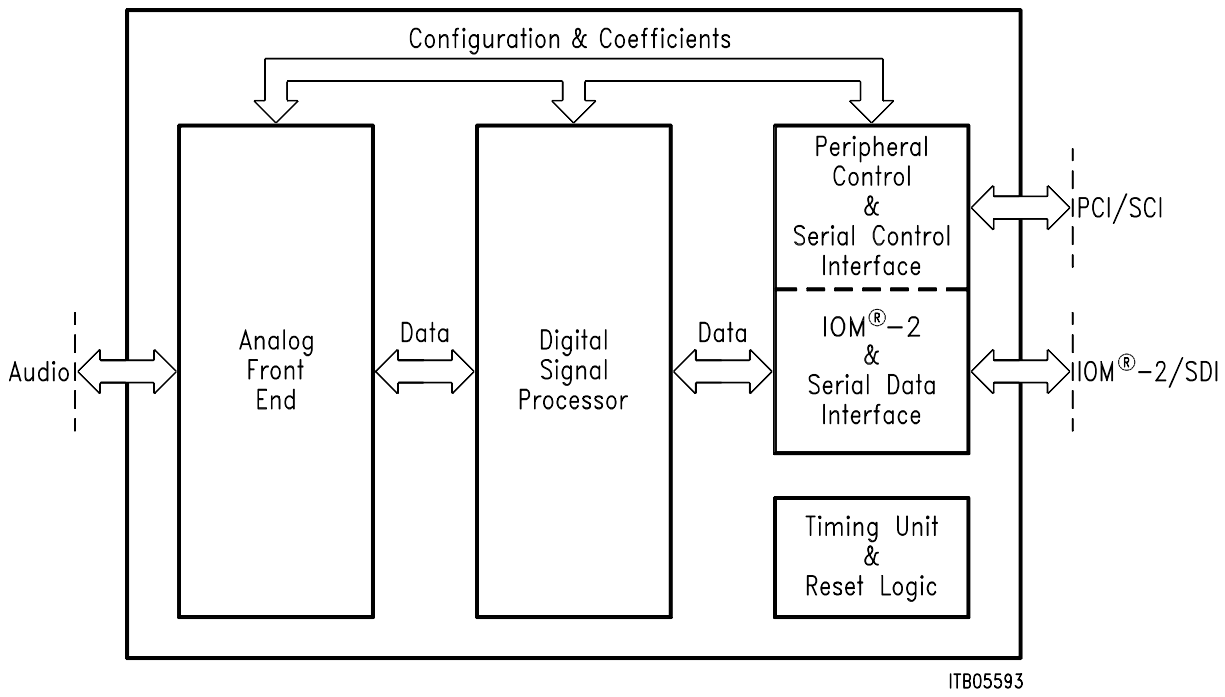


Figure 2
Block Diagram of the ARCOFI®

1.4 System Integration

The complete family of ICs for digital terminals offered by Siemens simplifies the development of these devices and gives a cost-effective solution to the design engineer. The architecture of these terminals is based on a modular interface especially conceived for ISDN and named IOM-2.

Figure 3 shows an example of an integrated multifunctional ISDN-S terminal using the ISAC®-S TE. The ISAC-S TE (ISAC-S: ISDN S-Access controller PSB 2186) provides the S interface and separates the B and D channels.

In this example one ICC (ICC: ISDN Communication Controller PEB 2070) is used to handle data packets on the D-channel. A voice processor is connected to a programmable digital signal processing codec filter (ARCOFI) via IC1 and a data encryption module to a data device via IC2. B1 is used for voice communication and B2 for data communication.

Typical terminal applications are described in the next sections.

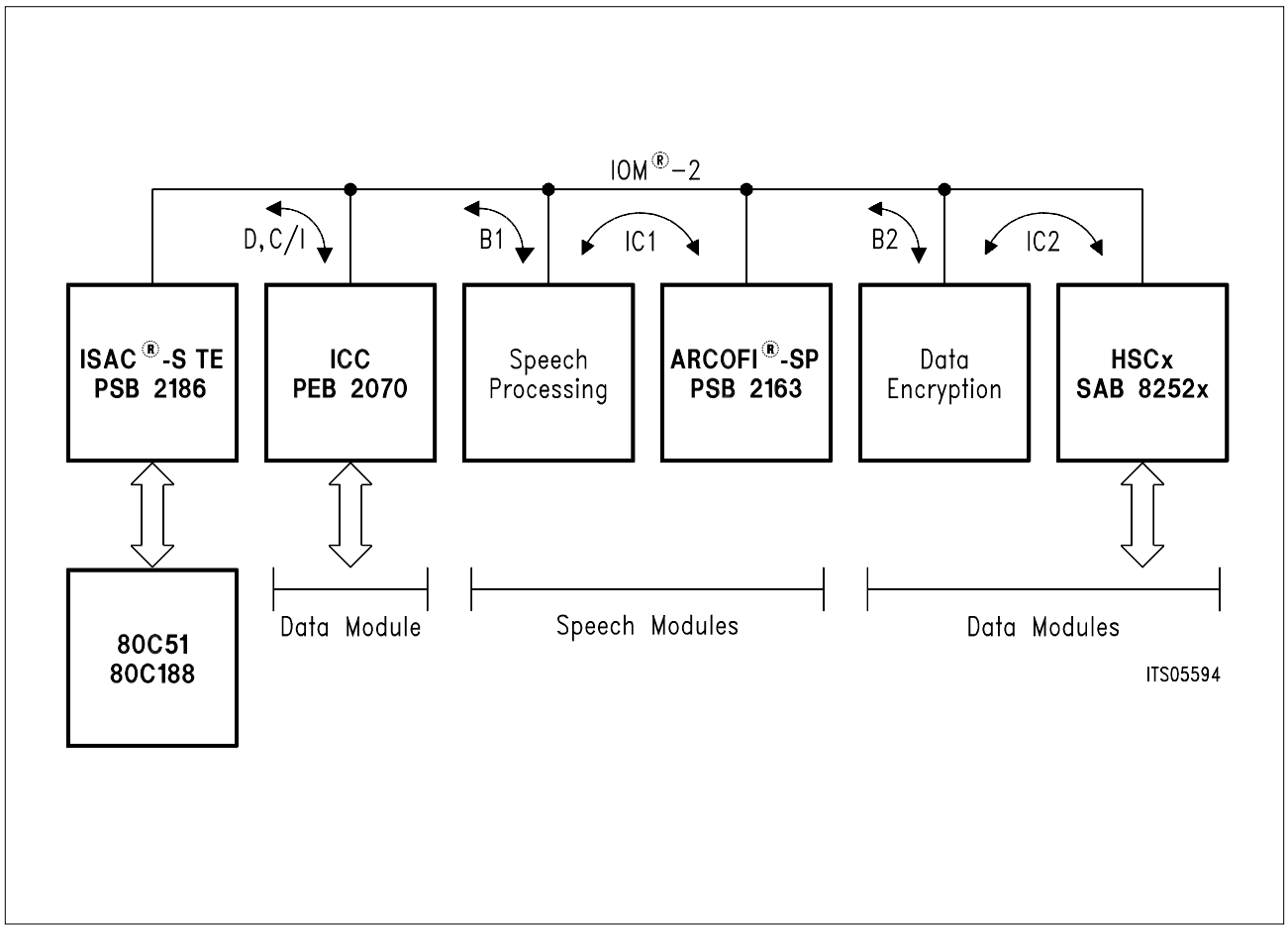


Figure 3
Example of ISDN-S Voice/Data Terminal

1.4.1 ISDN-Voice Terminal

Figure 4 shows a typical solution for a voice terminal for S interface.

The ARCOFI offers the functions of CODEC, filtering and speakerphone. It also carries out the functions of tone ringing, DTMF, and A/D- and D/A-conversions. The ARCOFI permits the direct connection of a handset and a speakerphone/loudspeaker.

The ARCOFI can be programmed and read out by the µC via the lOM-2-interface and the ISAC-S TE. The same µC supervises the keyboard functions and the function hook-on/off.

The S-interface functions such as activation/deactivation, clock recovery, clock resynchronization as well as the layer-2 functions like LAPD-protocol handling are executed by the ISDN-Subscriber Access Controller, also called ISAC-S TE PSB 2186.

A U_{K0}-interface telephone can easily be derived from the voice terminal shown on **figure 4** by replacing the ISAC-S with the ISDN-Communication Controller ICC PEB 2070 and the ISDN-Echo Cancellation Unit IEC PEB 2091.

A U_{P0}-interface telephone is obtained by interchanging the IEC with the ISDN-Burst Controller IBC PEB 2095. In this configuration the ICC PEB 2070 and the IBC PEB 2095 can be replaced by the ISAC-P TE PSB 2196.

Figure 5 shows a typical solution for a voice terminal for U_{K0}- or U_{P0}-interface.

In any case the whole terminal is power supplied either by the ISDN-Remote Power Controller IRPC PSB 2120 or by the General Purpose Power Controller GPPC PSB 2121.

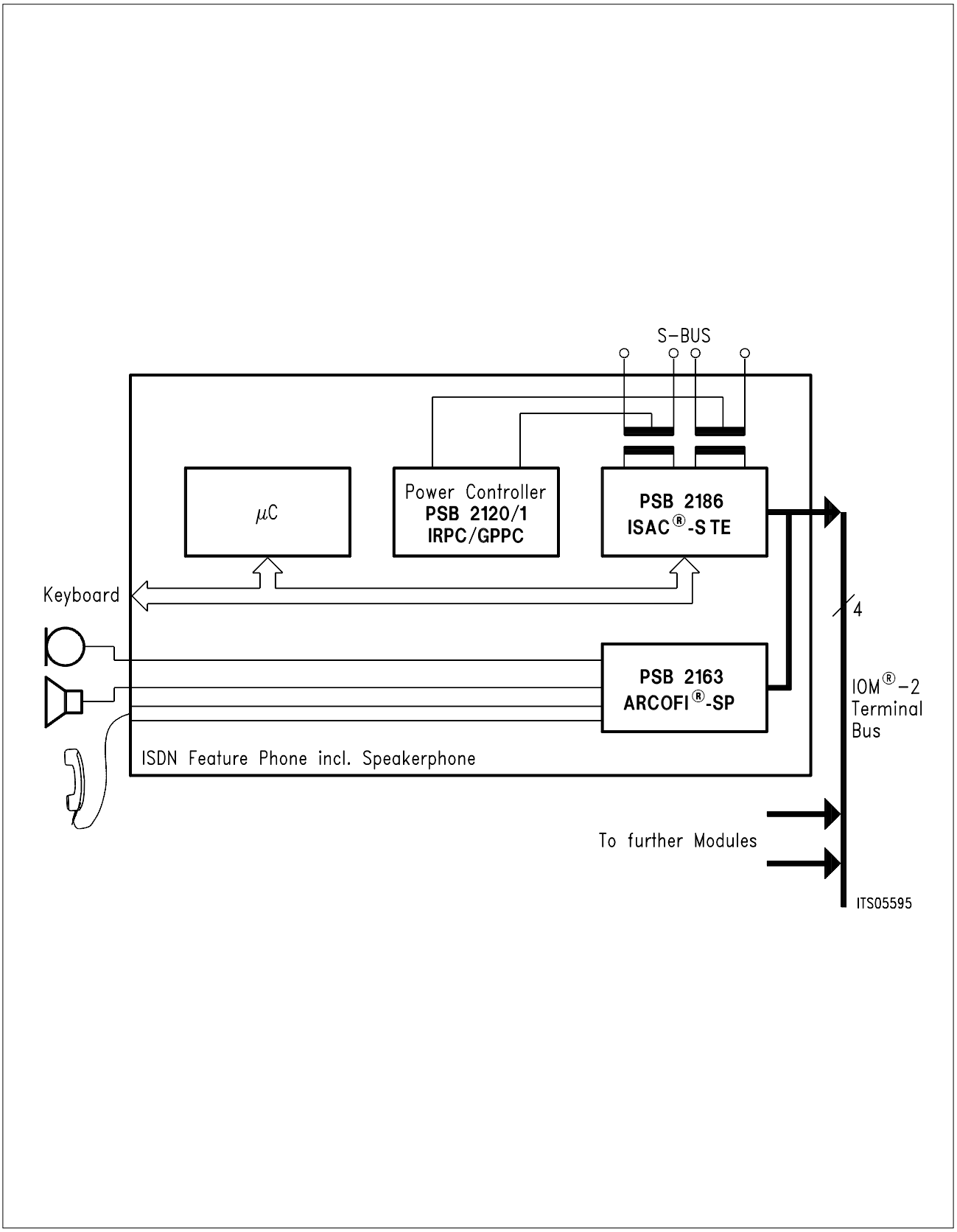
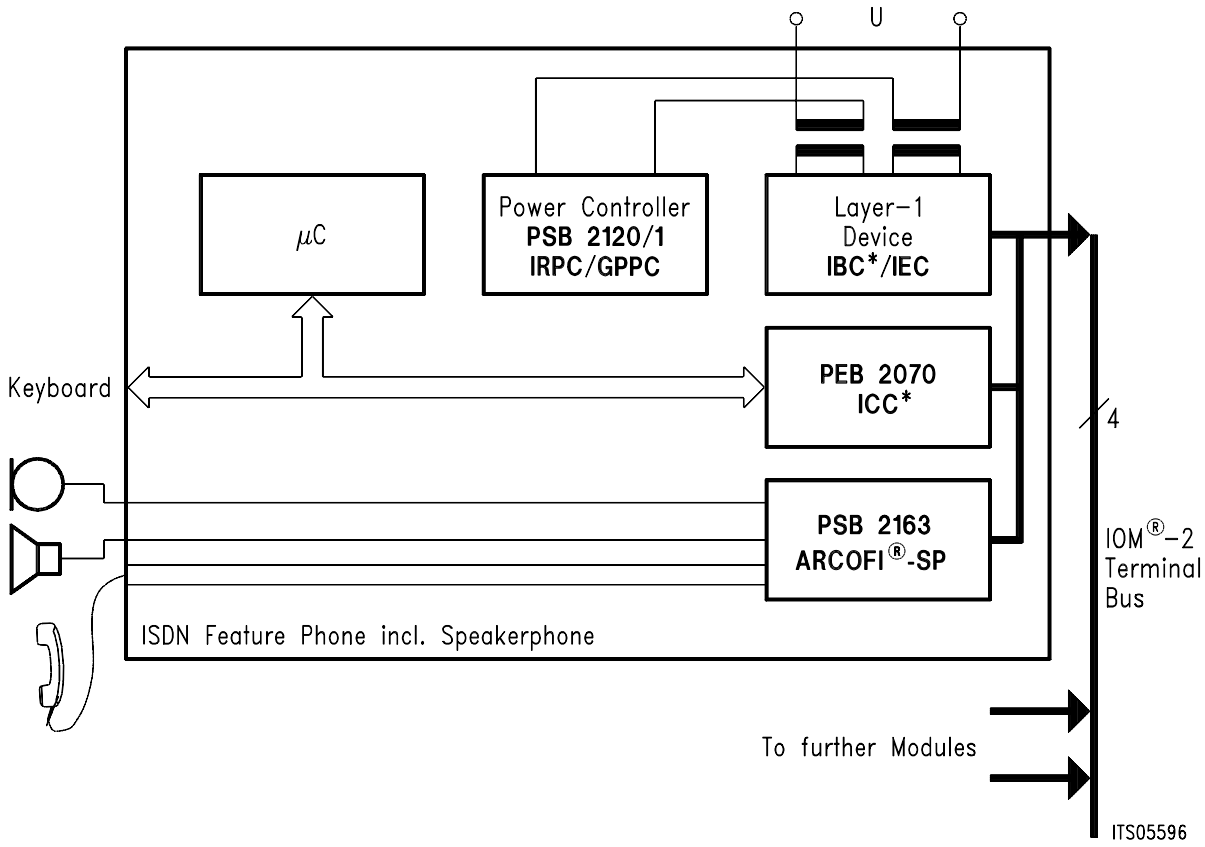


Figure 4
Basic ISDN S-Voice Terminal



*** ICC and IBC can be replaced by the ISAC®-P TE PSB 2196**

Figure 5
Basic ISDN U-Voice Terminal

1.4.2 Terminal Adapter a, b for Analog Telephones

Figure 6 shows how to implement a terminal adapter (a, b) connecting analog telephones to the ISDN-world. A SLIC can be connected to the ARCOFI.

The tip and ring information is transmitted transparently through the ARCOFI via the C/I-channel of the IOM-channel 1, through the ISAC-S TE to the µC.

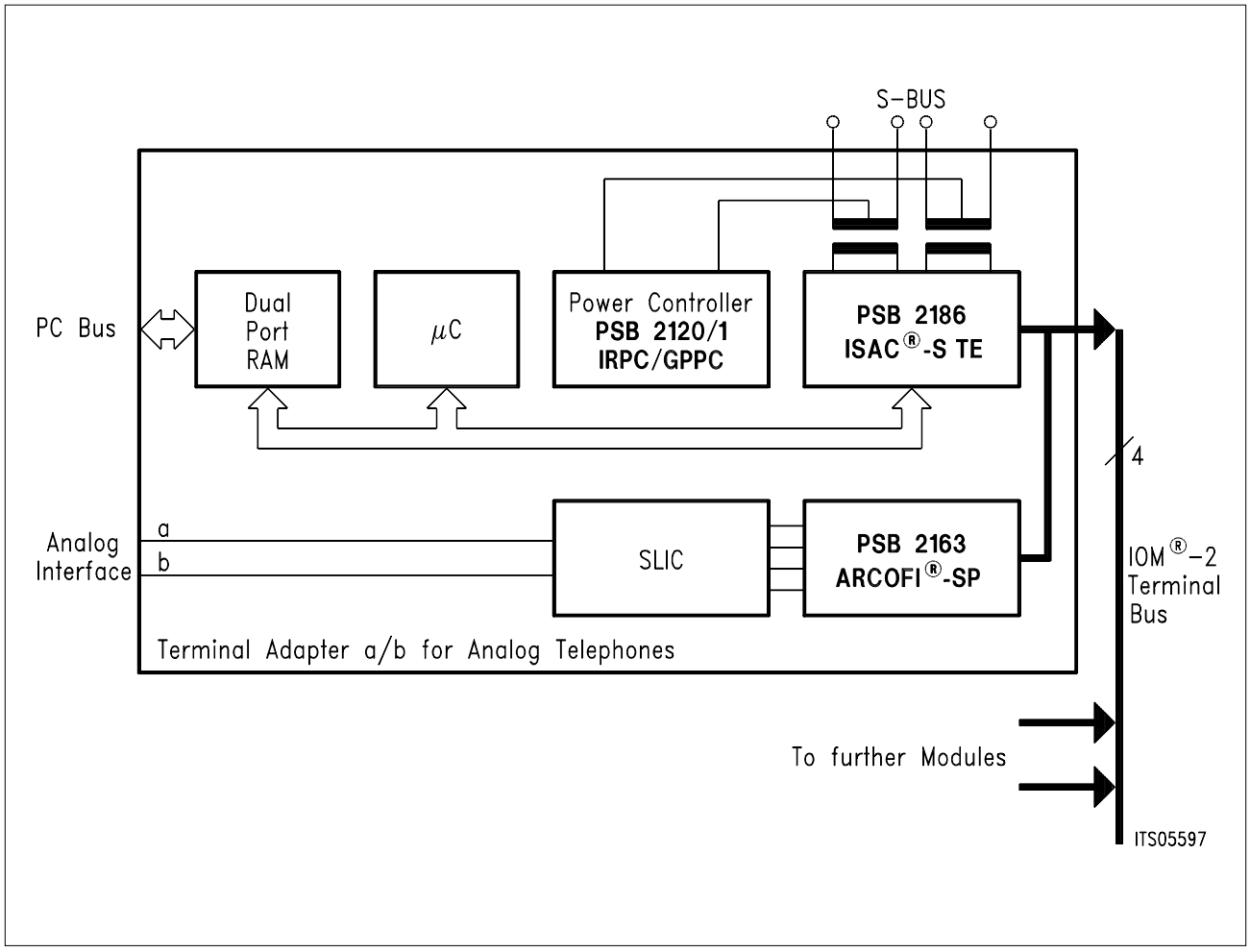


Figure 6
Terminal Adapter a, b for Analog Telephones

1.4.3 Voice/Data Terminal (PC-Card)

Figure 7 shows a voice/data terminal developed on a PC-card. The ITAC PSB 2110 (ITAC: ISDN-Terminal Adapter Circuit) ensures the bit rate adaptation necessary to connect a non ISDN-terminal (V.24) to the ISDN-world.

The COM-IC is an UART (type: 8250 or 16450) which is necessary for modem applications.

The Dual Port RAM is used for data transfer between the terminal processor and the PC.

The card is powered by the PC, and thus no power controller is necessary.

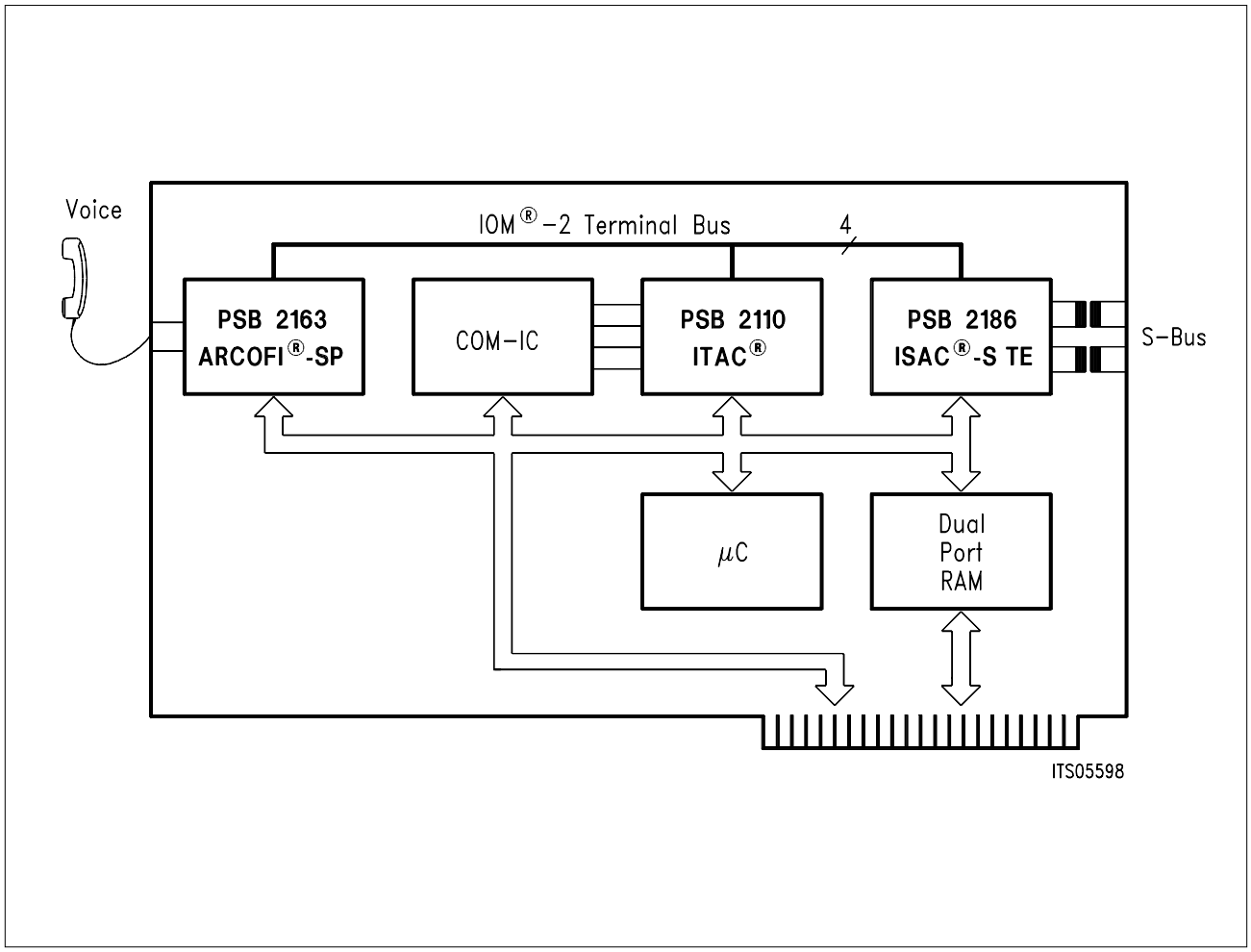


Figure 7
PC-Card as an ISDN-Voice/Data Terminal

1.4.4 Multifunctional ISDN-Terminal

Figure 8 gives an example of a multifunctional terminal. The HSCX SAB 82525 (HSCX: High-Level Serial Communications Controller Extended) simplifies the realization of an intelligent X.25 terminal adapter module whereas the ITAC PSB 2110 offers X.21, V.24, V.110 or V.120 interfaces for non ISDN-terminals.

The µC connected to the ISAC-S TE PSB 2186 is the system master. The two other µCs are the slaves. When a slave µC wants to intervene, it informs the master via the C/I-channel of IOM-2 channel 1.

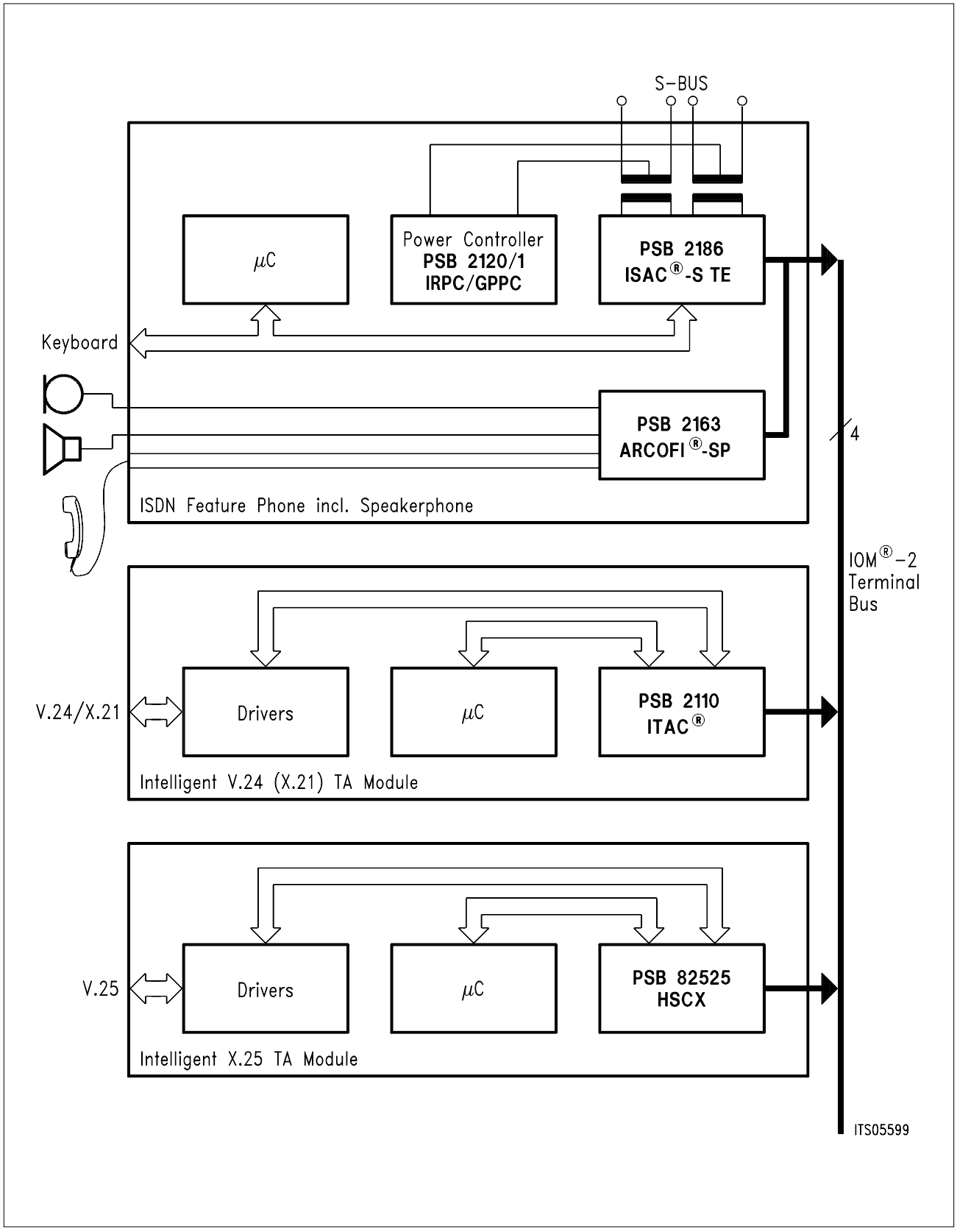


Figure 8
Multifunctional ISDN-Terminal