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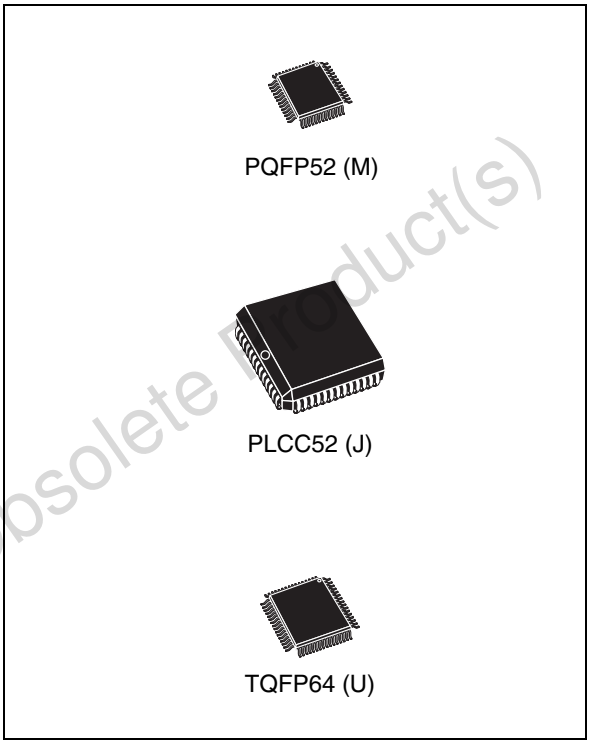
PSD8XXFX

Flash in-system programmable (ISP) peripherals for 8-bit MCUs, 5 V

Features

- Flash in-system programmable (ISP) peripheral for 8-bit MCUs
- Dual bank Flash memories
  - Up to 2 Mbit of primary Flash memory (8 uniform sectors, 32K x8)
  - Up to 256 Kbit secondary Flash memory (4 uniform sectors)
  - Concurrent operation: read from one memory while erasing and writing the other
- Up to 256 Kbit SRAM
- 27 reconfigurable I/Oports
- Enhanced JTAG serial port
- PLD with macrocells
  - Over 3000 gates of PLD: CPLD and DPLD
  - CPLD with 16 output macrocells (OMCs) and 24 input macrocells (IMCs)
  - DPLD - user defined internal chip select decoding
- 27 individually configurable I/O port pins
  They can be used for the following functions:
  - MCU I/Os
  - PLD I/Os
  - Latched MCU address output
  - Special function I/Os.
  - 16 of the I/O ports may be configured as open-drain outputs.
- In-system programming (ISP) with JTAG
  - Built-in JTAG compliant serial port allows full-chip in-system programmability
  - Efficient manufacturing allow easy product testing and programming
  - Use low cost FlashLINK cable with PC
- Page register
  - Internal page register that can be used to expand the microcontroller address space by a factor of 256



- Programmable power management
- Packages are ECOPACK®

Table 1. Device summary

Reference	Part number
PSD8XXFX	PSD813F2
	PSD813F4
	PSD813F5
	PSD833F2
	PSD834F2
	PSD853F2
	PSD854F2

Contents

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1 Summary description

The PSD8XXFX family of memory systems for microcontrollers (MCUs) brings in-system-programmability (ISP) to Flash memory and programmable logic. The result is a simple and flexible solution for embedded designs. PSD devices combine many of the peripheral functions found in MCU based applications.

Table 2 summarizes all the devices.

The CPLD in the PSD devices features an optimized macrocell logic architecture. The PSD macrocell was created to address the unique requirements of embedded system designs. It allows direct connection between the system address/data bus, and the internal PSD registers, to simplify communication between the MCU and other supporting devices.

The PSD device includes a JTAG serial programming interface, to allow in-system programming (ISP) of the entire device. This feature reduces development time, simplifies the manufacturing flow, and dramatically lowers the cost of field upgrades. Using ST's special Fast-JTAG programming, a design can be rapidly programmed into the PSD in as little as seven seconds.

The innovative PSD8XXFX family solves key problems faced by designers when managing discrete Flash memory devices, such as:

- First-time in-system programming (ISP)
- Complex address decoding
- Simultaneous read and write to the device.

The JTAG Serial Interface block allows in-system programming (ISP), and eliminates the need for an external Boot EPROM, or an external programmer. To simplify Flash memory updates, program execution is performed from a secondary Flash memory while the primary Flash memory is being updated. This solution avoids the complicated hardware and software overhead necessary to implement IAP.

ST makes available a software development tool, PSDsoft™ Express, that generates ANSI-C compliant code for use with your target MCU. This code allows you to manipulate the non-volatile memory (NVM) within the PSD. Code examples are also provided for:

- Flash memory IAP via the UART of the host MCU
- Memory paging to execute code across several PSD memory pages
- Loading, reading, and manipulation of PSD macrocells by the MCU.

Table 2. Product range

Part number[1]	Primary Flash memory (8 sectors)	Secondary Flash memory (4 sectors)	SRAM	I/O ports	Number of macrocells		Serial ISP JTAG/ISC port	Turbo mode
					Input	Output		
PSD813F2	1 Mbit	256 Kbit	16 Kbit	27	24	16	yes	yes
PSD813F4	1 Mbit	256 Kbit	none	27	24	16	yes	yes
PSD813F5	1 Mbit	none	none	27	24	16	yes	yes
PSD833F2	1 Mbit	256 Kbit	64 Kbit	27	24	16	yes	yes
PSD834F2	2 Mbit	256 Kbit	64 Kbit	27	24	16	yes	yes

Table 2. Product range (continued)

Part number(1)	Primary Flash memory (8 sectors)	Secondary Flash memory (4 sectors)	SRAM	I/O ports	Number of macrocells		Serial ISP JTAG/ISC port	Turbo mode
					Input	Output		
PSD853F2	1 Mbit	256 Kbit	256 Kbit	27	24	16	yes	yes
PSD854F2	2 Mbit	256 Kbit	256 Kbit	27	24	16	yes	yes

1. All products support: JTAG serial ISP, MCU parallel ISP, ISP Flash memory, ISP CPLD, Security features, Power Management Unit (PMU), Automatic Power-down (APD)

Figure 1. PQFP52 connections

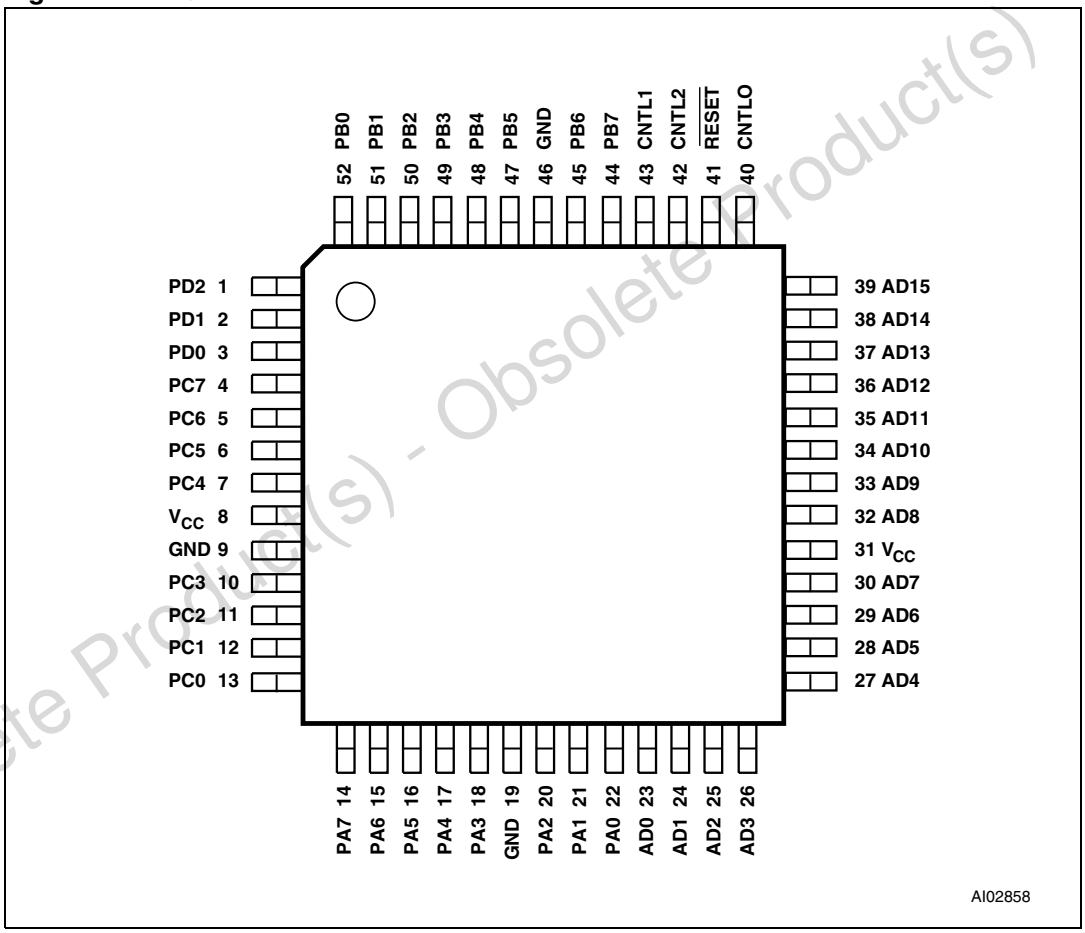


Figure 2. PLCC52 connections

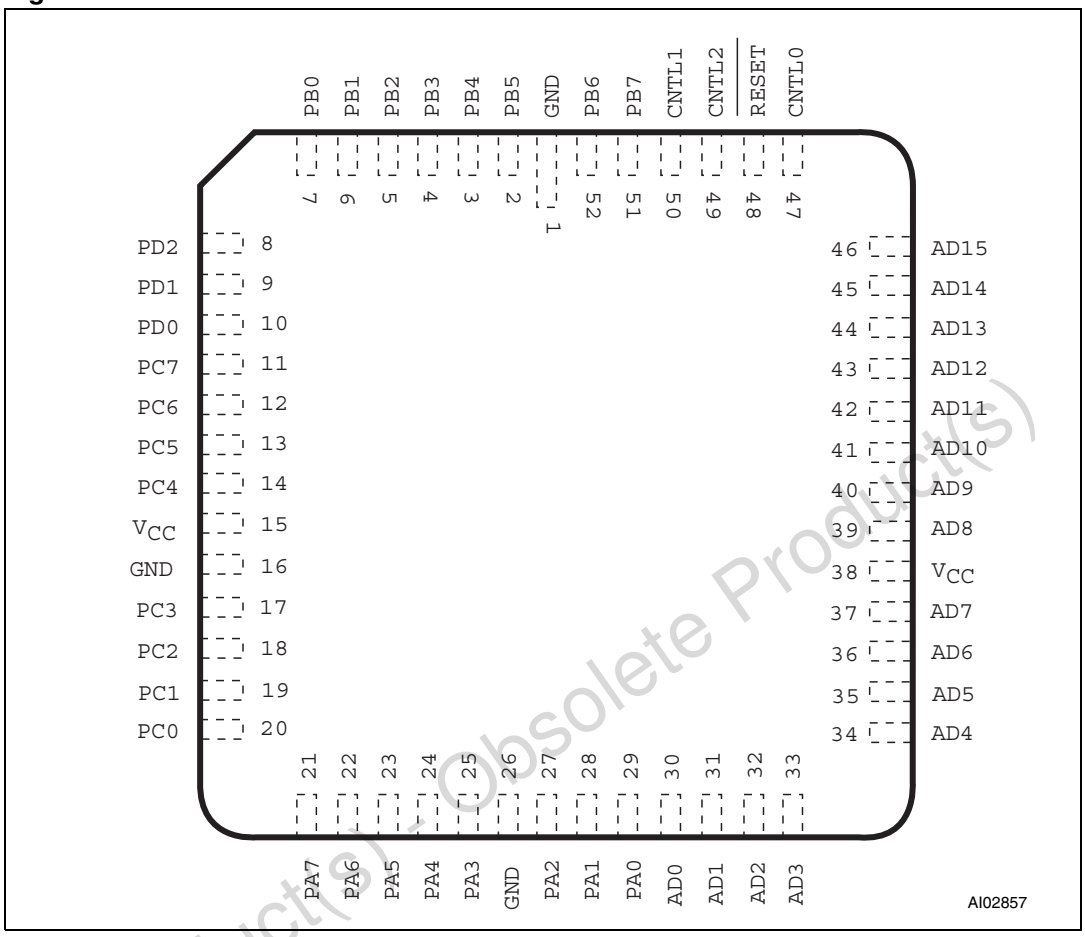
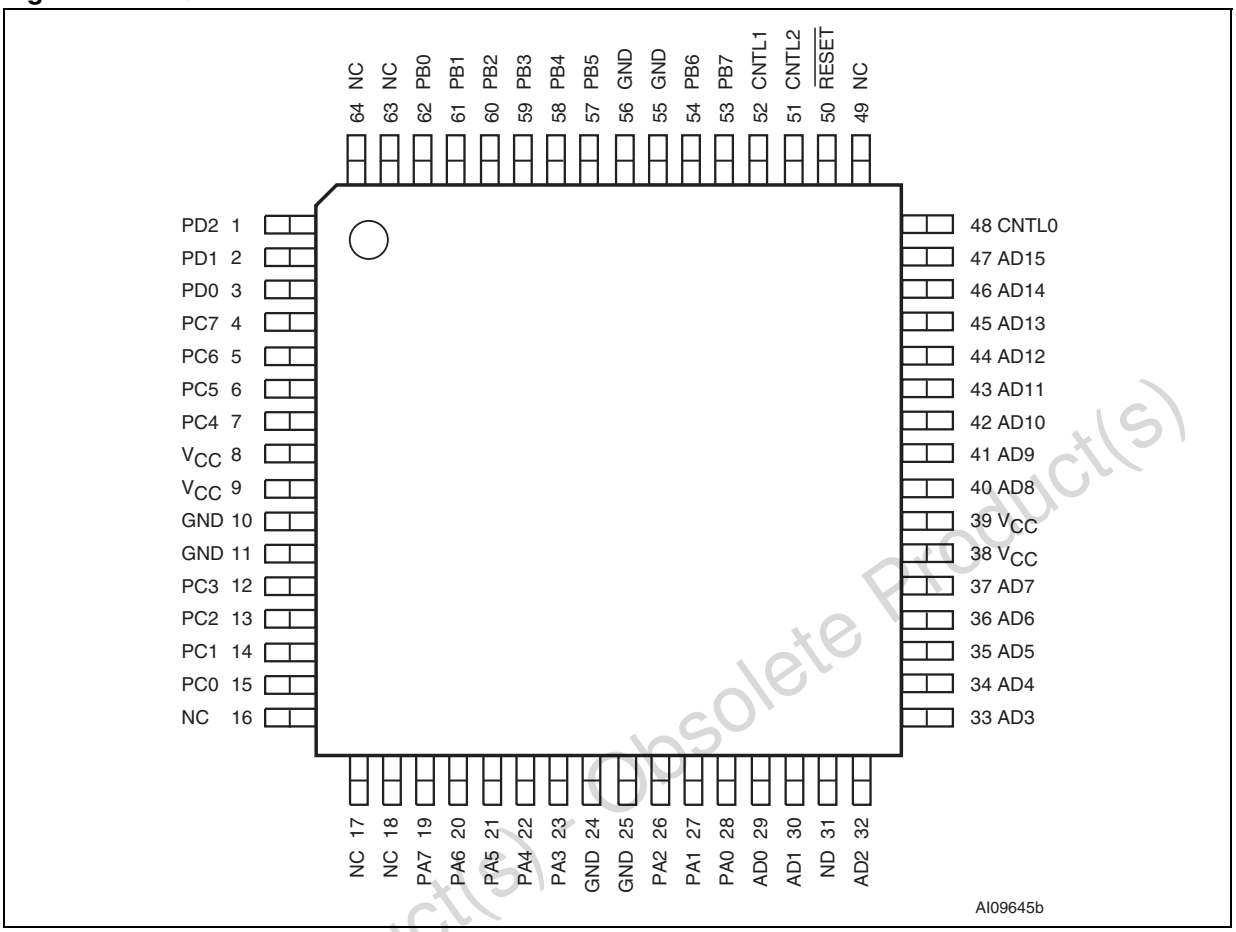


Figure 3. TQFP64 connections



2 Pin description

Table 3. PLCC52 pin description (1)

Pin name	Pin	Type	Description
ADIO0-7	30-37	I/O	This is the lower Address/Data port. Connect your MCU address or address/data bus according to the following rules: If your MCU has a multiplexed address/data bus where the data is multiplexed with the lower address bits, connect AD0-AD7 to this port. If your MCU does not have a multiplexed address/data bus, or you are using an 80C251 in page mode, connect A0-A7 to this port. If you are using an 80C51XA in burst mode, connect A4/D0 through A11/D7 to this port. ALE or AS latches the address. The PSD drives data out only if the READ signal is active and one of the PSD functional blocks was selected. The addresses on this port are passed to the PLDs.
ADIO8-15	39-46	I/O	This is the upper Address/Data port. Connect your MCU address or address/data bus according to the following rules: If your MCU has a multiplexed address/data bus where the data is multiplexed with the lower address bits, connect A8-A15 to this port. If your MCU does not have a multiplexed address/data bus, connect A8-A15 to this port. If you are using an 80C251 in page mode, connect AD8-AD15 to this port. If you are using an 80C51XA in burst mode, connect A12/D8 through A19/D15 to this port. ALE or AS latches the address. The PSD drives data out only if the READ signal is active and one of the PSD functional blocks was selected. The addresses on this port are passed to the PLDs.
CNTL0	47	I	The following control signals can be connected to this port, based on your MCU: $\overline{WR}$ – active low Write Strobe input. R_$\overline{W}$ – active high READ/active low write input. This port is connected to the PLDs. Therefore, these signals can be used in decode and other logic equations.
CNTL1	50	I	The following control signals can be connected to this port, based on your MCU: $\overline{RD}$ – active low Read Strobe input. E – E clock input. $\overline{DS}$ – active low Data Strobe input. $\overline{PSEN}$ – connect $\overline{PSEN}$ to this port when it is being used as an active low READ signal. For example, when the 80C251 outputs more than 16 address bits, $\overline{PSEN}$ is actually the READ signal. This port is connected to the PLDs. Therefore, these signals can be used in decode and other logic equations.
CNTL2	49	I	This port can be used to input the $\overline{PSEN}$ (Program Select Enable) signal from any MCU that uses this signal for code exclusively. If your MCU does not output a Program Select Enable signal, this port can be used as a generic input. This port is connected to the PLDs.
Reset	48	I	Resets I/O ports, PLD macrocells and some of the Configuration registers. Must be low at Power-up.

Table 3. PLCC52 pin description (1) (continued)

Pin name	Pin	Type	Description
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	29 28 27 25 24 23 22 21	I/O	These pins make up port A. These port pins are configurable and can have the following functions: MCU I/O – write to or read from a standard output or input port. CPLD macrocell (McellAB0-7) outputs. Inputs to the PLDs. Latched address outputs (see *Table 7*). Address inputs. For example, PA0-3 could be used for A0-A3 when using an 80C51XA in burst mode. As the data bus inputs D0-D7 for non-multiplexed address/data bus MCUs. D0/A16-D3/A19 in M37702M2 mode. Peripheral I/O mode. *Note: PA0-PA3 can only output CMOS signals with an option for high slew rate. However, PA4-PA7 can be configured as CMOS or Open Drain outputs.*
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7	7 6 5 4 3 2 52 51	I/O	These pins make up port B. These port pins are configurable and can have the following functions: MCU I/O – write to or read from a standard output or input port. CPLD macrocell (McellAB0-7 or McellBC0-7) outputs. Inputs to the PLDs. Latched address outputs (see *Table 7*). *Note: PB0-PB3 can only output CMOS signals with an option for high slew rate. However, PB4-PB7 can be configured as CMOS or Open Drain outputs.*
PC0	20	I/O	PC0 pin of port C. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. CPLD macrocell (McellBC0) output. Input to the PLDs. TMS input(2) for the JTAG Serial Interface. This pin can be configured as a CMOS or Open Drain output.
PC1	19	I/O	PC1 pin of port C. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. CPLD macrocell (McellBC1) output. Input to the PLDs. TCK input(2) for the JTAG Serial Interface. This pin can be configured as a CMOS or Open Drain output.
PC2	18	I/O	PC2 pin of port C. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. CPLD macrocell (McellBC2) output. Input to the PLDs. This pin can be configured as a CMOS or Open Drain output.

Table 3. PLCC52 pin description (1) (continued)

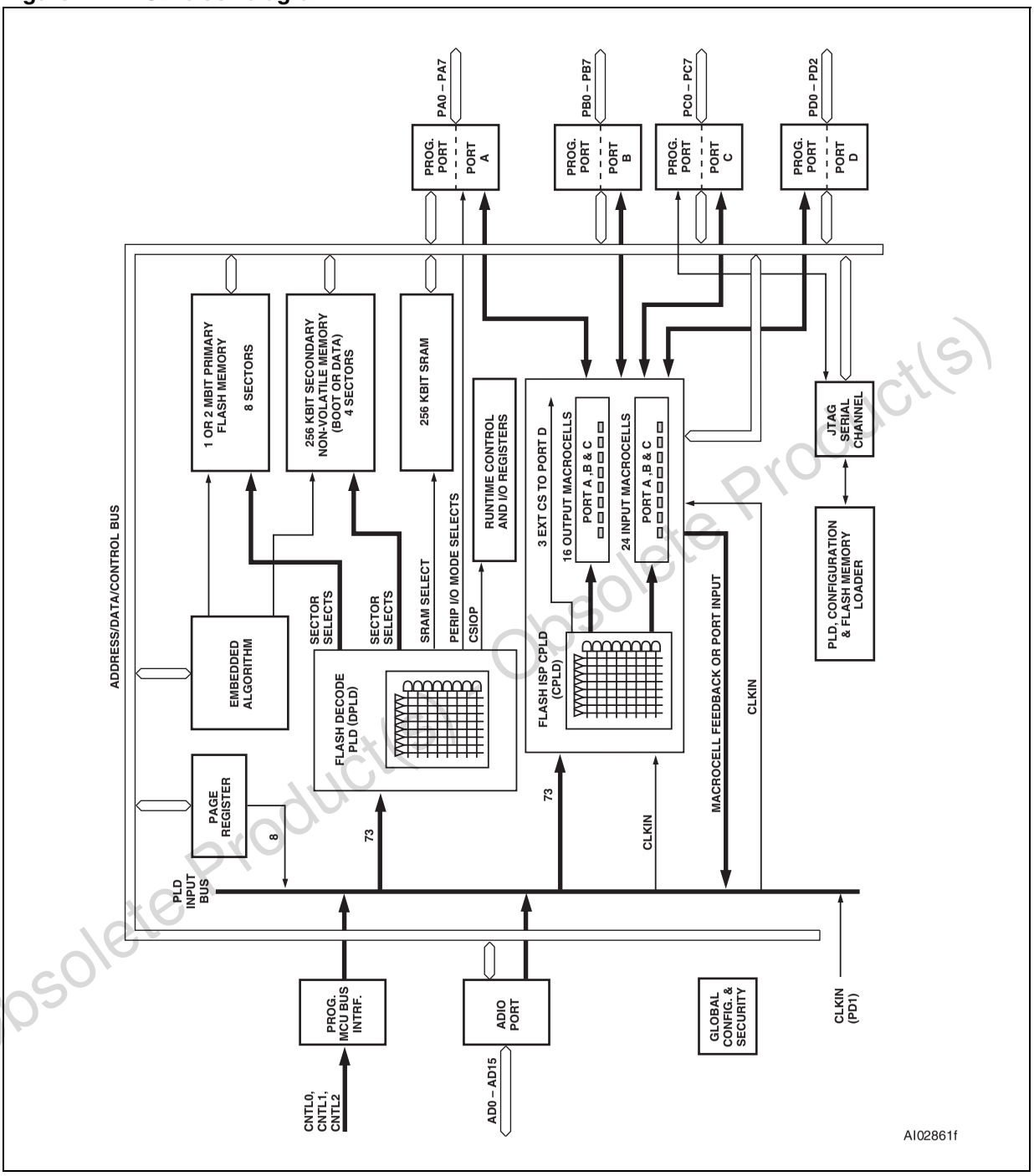
Pin name	Pin	Type	Description
PC3	17	I/O	PC3 pin of port C. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. CPLD macrocell (McellBC3) output. Input to the PLDs. $\overline{\text{TSTAT}}$ output(2) for the JTAG Serial Interface. Ready/$\overline{\text{Busy}}$ output for parallel in-system programming (ISP). This pin can be configured as a CMOS or Open Drain output.
PC4	14	I/O	PC4 pin of port C. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. CPLD macrocell (McellBC4) output. Input to the PLDs. $\overline{\text{TERR}}$ output(2) for the JTAG Serial Interface. This pin can be configured as a CMOS or Open Drain output.
PC5	13	I/O	PC5 pin of port C. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. CPLD macrocell (McellBC5) output. Input to the PLDs. TDI input(2) for the JTAG Serial Interface. This pin can be configured as a CMOS or Open Drain output.
PC6	12	I/O	PC6 pin of port C. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. CPLD macrocell (McellBC6) output. Input to the PLDs. TDO output(2) for the JTAG Serial Interface. This pin can be configured as a CMOS or Open Drain output.
PC7	11	I/O	PC7 pin of port C. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. CPLD macrocell (McellBC7) output. Input to the PLDs. DBE – active low Data Byte Enable input from 68HC912 type MCUs. This pin can be configured as a CMOS or Open Drain output.
PD0	10	I/O	PD0 pin of port D. This port pin can be configured to have the following functions: ALE/AS input latches address output from the MCU. MCU I/O – write or read from a standard output or input port. Input to the PLDs. CPLD output (External Chip Select).
PD1	9	I/O	PD1 pin of port D. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. Input to the PLDs. CPLD output (External Chip Select). CLKIN – clock input to the CPLD macrocells, the APD Unit's Power-down counter, and the CPLD AND Array.

Table 3. PLCC52 pin description (1) (continued)

Pin name	Pin	Type	Description
PD2	8	I/O	PD2 pin of port D. This port pin can be configured to have the following functions: MCU I/O - write to or read from a standard output or input port. Input to the PLDs. CPLD output (External Chip Select). PSD Chip Select input ($\overline{CSI}$). When low, the MCU can access the PSD memory and I/O. When high, the PSD memory blocks are disabled to conserve power.
V_{CC}	15, 38		Supply voltage
GND	1, 16, 26		Ground pins

1. The pin numbers in this table are for the PLCC package only. See the package information from *Table 73* onwards, for pin numbers on other package types.
2. These functions can be multiplexed with other functions.

Figure 4. PSD block diagram



3 PSD architectural overview

PSD devices contain several major functional blocks. *Figure 4* shows the architecture of the PSD device family. The functions of each block are described briefly in the following sections. Many of the blocks perform multiple functions and are user configurable.

3.1 Memory

Each of the memory blocks is briefly discussed in the following paragraphs. A more detailed discussion can be found in *Section 6.1: Memory blocks*.

The 1 Mbit or 2 Mbit (128K x 8, or 256K x 8) Flash memory is the primary memory of the PSD. It is divided into 8 equally-sized sectors that are individually selectable.

The optional 256 Kbit (32K x 8) secondary Flash memory is divided into 4 equally-sized sectors. Each sector is individually selectable.

The optional SRAM is intended for use as a scratch-pad memory or as an extension to the MCU SRAM.

Each sector of memory can be located in a different address space as defined by the user. The access times for all memory types includes the address latching and DPLD decoding time.

3.2 Page register

The 8-bit Page register expands the address range of the MCU by up to 256 times. The paged address can be used as part of the address space to access external memory and peripherals, or internal memory and I/O. The Page register can also be used to change the address mapping of sectors of the Flash memories into different memory spaces for IAP.

3.3 PLDs

The device contains two PLDs, the Decode PLD (DPLD) and the Complex PLD (CPLD), as shown in *Table 4*, each optimized for a different function. The functional partitioning of the PLDs reduces power consumption, optimizes cost/performance, and eases design entry.

The DPLD is used to decode addresses and to generate Sector Select signals for the PSD internal memory and registers. The DPLD has combinatorial outputs. The CPLD has 16 Output macrocells (OMC) and 3 combinatorial outputs. The PSD also has 24 input macrocells (IMC) that can be configured as inputs to the PLDs. The PLDs receive their inputs from the PLD input bus and are differentiated by their output destinations, number of product terms, and macrocells.

The PLDs consume minimal power. The speed and power consumption of the PLD is controlled by the Turbo Bit in PMMR0 and other bits in the PMMR2. These registers are set by the MCU at run-time. There is a slight penalty to PLD propagation time when invoking the power management features.

3.4 I/O ports

The PSD has 27 individually configurable I/O pins distributed over the four ports (Port A, B, C, and D). Each I/O pin can be individually configured for different functions. ports can be configured as standard MCU I/O ports, PLD I/O, or latched address outputs for MCUs using multiplexed address/data buses.

The JTAG pins can be enabled on port C for in-system programming (ISP).

Ports A and B can also be configured as a data port for a non-multiplexed bus.

3.5 MCU bus interface

PSD interfaces easily with most 8-bit MCUs that have either multiplexed or non-multiplexed address/data buses. The device is configured to respond to the MCU control signals, which are also used as inputs to the PLDs. For examples, please see *Section 15.4: MCU bus interface examples*.

Table 4. PLD I/O

Name	Inputs	Outputs	Product terms
Decode PLD (DPLD)	73	17	42
Complex PLD (CPLD)	73	19	140

3.6 JTAG port

In-system programming (ISP) can be performed through the JTAG signals on port C. This serial interface allows complete programming of the entire PSD device. A blank device can be completely programmed. The JTAG signals (TMS, TCK, $\overline{\text{TSTAT}}$, $\overline{\text{TERR}}$, TDI, TDO) can be multiplexed with other functions on port C. *Table 5* indicates the JTAG pin assignments.

3.7 In-system programming (ISP)

Using the JTAG signals on port C, the entire PSD device can be programmed or erased without the use of the MCU. The primary Flash memory can also be programmed in-system by the MCU executing the programming algorithms out of the secondary memory, or SRAM. The secondary memory can be programmed the same way by executing out of the primary Flash memory. The PLD or other PSD configuration blocks can be programmed through the JTAG port or a device programmer. *Table 6* indicates which programming methods can program different functional blocks of the PSD.

3.8 Power management unit (PMU)

The power management unit (PMU) gives the user control of the power consumption on selected functional blocks based on system requirements. The PMU includes an Automatic Power-down (APD) Unit that turns off device functions during MCU inactivity. The APD unit has a Power-down mode that helps reduce power consumption.

The PSD also has some bits that are configured at run-time by the MCU to reduce power consumption of the CPLD. The Turbo Bit in PMMR0 can be reset to '0' and the CPLD latches its outputs and goes to sleep until the next transition on its inputs.

Additionally, bits in PMMR2 can be set by the MCU to block signals from entering the CPLD to reduce power consumption. Please see *Section 17: Power management* for more details.

Table 5. JTAG SIgnals on port C

Port C pins	JTAG signal
PC0	TMS
PC1	TCK
PC3	$\overline{\text{TSTAT}}$
PC4	$\overline{\text{TERR}}$
PC5	TDI
PC6	TDO

Table 6. Methods for programming different functional blocks of the PSD

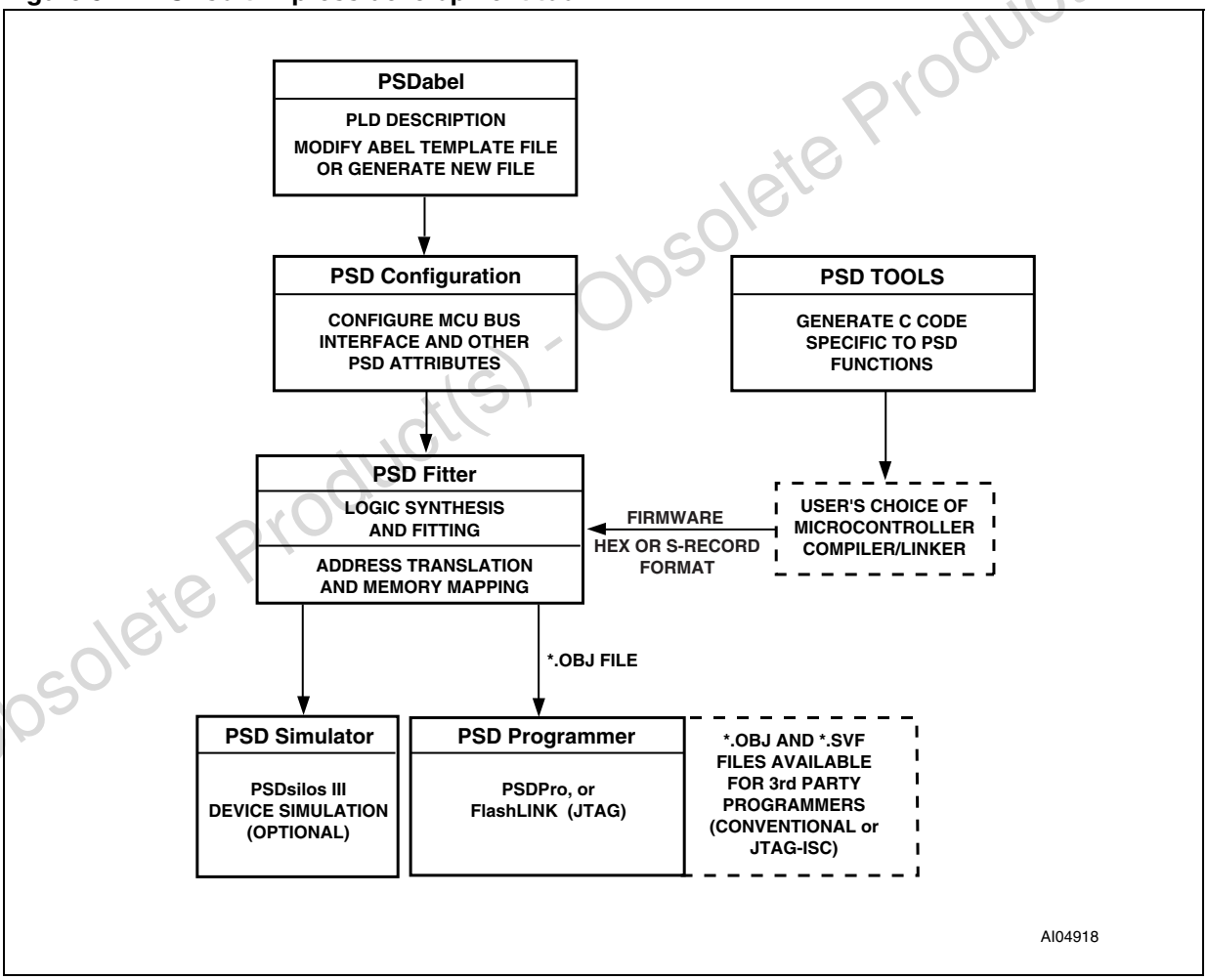
Functional block	JTAG programming	Device programmer	IAP
Primary Flash memory	Yes	Yes	Yes
Secondary Flash memory	Yes	Yes	Yes
PLD array (DPLD and CPLD)	Yes	Yes	No
PSD configuration	Yes	Yes	No

4 Development system

The PSD8XXFX family is supported by PSDsoft Express, a Windows-based software development tool. A PSD design is quickly and easily produced in a point and click environment. The designer does not need to enter Hardware Description Language (HDL) equations, unless desired, to define PSD pin functions and memory map information. The general design flow is shown in *Figure 5*. PSDsoft Express is available from our web site (the address is given on the back page of this data sheet) or other distribution channels.

PSDsoft Express directly supports two low cost device programmers form ST: PSDpro and FlashLINK (JTAG). Both of these programmers may be purchased through your local distributor/representative, or directly from our web site using a credit card. The PSD is also supported by third party device programmers. See our web site for the current list.

Figure 5. PSDsoft Express development tool



5 PSD register description and address offset

Table 7 shows the offset addresses to the PSD registers relative to the CSIOP base address. The CSIOP space is the 256 bytes of address that is allocated by the user to the internal PSD registers. *Table 8* provides brief descriptions of the registers in CSIOP space. The following section gives a more detailed description.

Table 7. I/O port latched address output assignments(1)(2)

MCU	Port A		Port B	
	Port A (3:0)	Port A (7:4)	Port B (3:0)	Port B (7:4)
8051XA (8-bit)	N/A	Address a7-a4	Address a11-a8	N/A
80C251 (page mode)	N/A	N/A	Address a11-a8	Address a15-a12
All other 8-bit multiplexed	Address a3-a0	Address a7-a4	Address a3-a0	Address a7-a4
8-bit non-multiplexed bus	N/A	N/A	Address a3-a0	Address a7-a4

1. See *Section 16: I/O ports*, on how to enable the Latched Address Output function.
2. N/A = Not Applicable

Table 8. Register address offset

Register name	Port A	Port B	Port C	Port D	Other (1)	Description
Data In	00	01	10	11		Reads port pin as input, MCU I/O input mode
Control	02	03				Selects mode between MCU I/O or Address Out
Data Out	04	05	12	13		Stores data for output to port pins, MCU I/O output mode
Direction	06	07	14	15		Configures port pin as input or output
Drive Select	08	09	16	17		Configures port pins as either CMOS or Open Drain on some pins, while selecting high slew rate on other pins.
Input macrocell	0A	0B	18			Reads input macrocells
Enable Out	0C	0D	1A	1B		Reads the status of the output enable to the I/O port driver
Output macrocells AB	20	20				READ – reads output of macrocells AB WRITE – loads macrocell flip-flops
Output macrocells BC		21	21			READ – reads output of macrocells BC WRITE – loads macrocell flip-flops

Table 8. Register address offset (continued)

Register name	Port A	Port B	Port C	Port D	Other (1)	Description
Mask macrocells AB	22	22				Blocks writing to the Output macrocells AB
Mask macrocells BC		23	23			Blocks writing to the Output macrocells BC
Primary Flash Protection					C0	Read only – Primary Flash Sector Protection
Secondary Flash memory Protection					C2	Read only – PSD Security and Secondary Flash memory Sector Protection
JTAG Enable					C7	Enables JTAG port
PMMR0					B0	Power Management register 0
PMMR2					B4	Power Management register 2
Page					E0	Page register
VM					E2	Places PSD memory areas in program and/or data space on an individual basis.

1. Other registers that are not part of the I/O ports.