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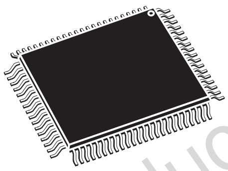
PSD835G2V

Flash PSD, 3 V supply, for 8-bit MCUs
4 Mbit + 256 Kbit dual Flash memories and 64 Kbit SRAM

Features

- Flash in-system programmable (ISP) peripheral for 8-bit MCUs
- Dual bank Flash memories
  - 4 Mbits of primary Flash memory (8 uniform sectors, 64 Kbytes)
  - 256 Kbits of secondary Flash memory with 4 sectors
  - Concurrent operation: READ from one memory while erasing and writing the other
- 64 Kbit of SRAM
- 52 reconfigurable I/O ports
- Enhanced JTAG serial port
- PLD with macrocells
  - Over 3000 gates of PLD: CPLD and DPLD
  - CPLD with 16 output macrocells (OMCs) and 24 macrocells (IMCs)
  - DPLD - user defined internal chip select decoding
- 52 individually configurable I/O port pins
  They can be used for the following functions:
  - MCU I/Os
  - PLD I/Os
  - Latched MCU address output
  - Special function I/Os.
  - I/O ports may be configured as open-drain outputs.
- In-system programming (ISP) with JTAG
  - Built-in JTAG compliant serial port allows full-chip in-system programmability
  - Efficient manufacturing allow easy product testing and programming
  - Use low cost FlashLINK cable with PC
- Page register
  - Internal page register that can be used to expand the microcontroller address space by a factor of 256



LQFP80 (U)

- Programmable power management
- High endurance
  - 100,000 erase/write cycles of Flash memory
  - 1,000 erase/write cycles of PLD
  - 15 year data retention
- 3 V±10% single supply voltage
- Standby current as low as 25 µA
- Memory speed
  - 90 ns Flash memory and SRAM access time for V_{CC} = 3.0 to 3.6 V
  - 120 ns Flash memory and SRAM access time for V_{CC} = 3.0 to 3.6 V
- ECOPACK® package

Contents

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1 Description

The PSD family of memory systems for microcontrollers (MCUs) brings in-system-programmability (ISP) to Flash memory and programmable logic. The result is a simple and flexible solution for embedded designs. PSD devices combine many of the peripheral functions found in MCU based applications.

The CPLD in the PSD devices features an optimized macrocell logic architecture. The PSD macrocell was created to address the unique requirements of embedded system designs. It allows direct connection between the system address/data bus, and the internal PSD registers, to simplify communication between the MCU and other supporting devices.

The PSD family offers two methods to program the PSD Flash memory while the PSD is soldered to the circuit board: In-System Programming (ISP) via JTAG, and In-Application Programming (IAP).

1.1 In-system programming (ISP) via JTAG

An IEEE 1149.1 compliant JTAG In-system programming (ISP) interface is included on the PSD enabling the entire device (Flash memories, PLD, configuration) to be rapidly programmed while soldered to the circuit board. This requires no MCU participation, which means the PSD can be programmed anytime, even when completely blank.

The innovative JTAG interface to Flash memories is an industry first, solving key problems faced by designers and manufacturing houses, such as:

- First time programming
- Inventory buid-up of preprogrammed devices
- Expendsive sockets

1.1.1 First time programming

How do I get firmware into the Flash memory the very first time? JTAG is the answer. Program the blank PSD with no MCU involvement.

1.1.2 Inventory build-up of preprogrammed devices

How do I maintain an accurate count of pre-programmed Flash memory and PLD devices based on customer demand? How many and what version? JTAG is the answer. Build your hardware with blank PSDs soldered directly to the board and then custom program just before they are shipped to the customer. No more labels on chips, and no more wasted inventory.

1.1.3 Expensive sockets

How do I eliminate the need for expensive and unreliable sockets? JTAG is the answer. Solder the PSD directly to the circuit board. Program first time and subsequent times with JTAG. No need to handle devices and bend the fragile leads.

1.2 In-application programming (IAP)

Two independent Flash memory arrays are included so that the MCU can execute code from one while erasing and programming the other. Robust product firmware updates in the field are possible over any communications channel (CAN, Ethernet, UART, J1850, etc.) using this unique architecture. Designers are relieved of the following problems:

- Simultaneous READ and WRITE to Flash memory
- Complex memory mapping
- Sepcarate program and data space

1.2.1 Simultaneous READ and WRITE to Flash memory

How can the MCU program the same memory from which it is executing code? It cannot. The PSD allows the MCU to operate the two Flash memory blocks concurrently, reading code from one while erasing and programming the other during IAP.

1.2.2 Complex memory mapping

How can I map these two memories efficiently? A programmable Decode PLD (DPLD) is embedded in the PSD. The concurrent PSD memories can be mapped anywhere in MCU address space, segment by segment with extremely high address resolution. As an option, the secondary Flash memory can be swapped out of the system memory map when IAP is complete. A built-in page register breaks the MCU address limit.

1.2.3 Separate program and data space

How can I write to Flash memory while it resides in Program space during field firmware updates? My 80C51 will not allow it. The PSD provides means to reclassify Flash memory as Data space during IAP, then back to Program space when complete.

1.3 PSDsoft™

PSDsoft, a software development tool from ST, guides you through the design process step-by-step making it possible to complete an embedded MCU design capable of ISP/IAP in just hours. Select your MCU and PSDsoft takes you through the remainder of the design with point and click entry, covering PSD selection, pin definitions, programmable logic inputs and outputs, MCU memory map definition, ANSI-C code generation for your MCU, and merging your MCU firmware with the PSD design. When complete, two different device programmers are supported directly from PSDsoft: FlashLINK (JTAG) and PSDpro.

Figure 1. LQFP80 connections

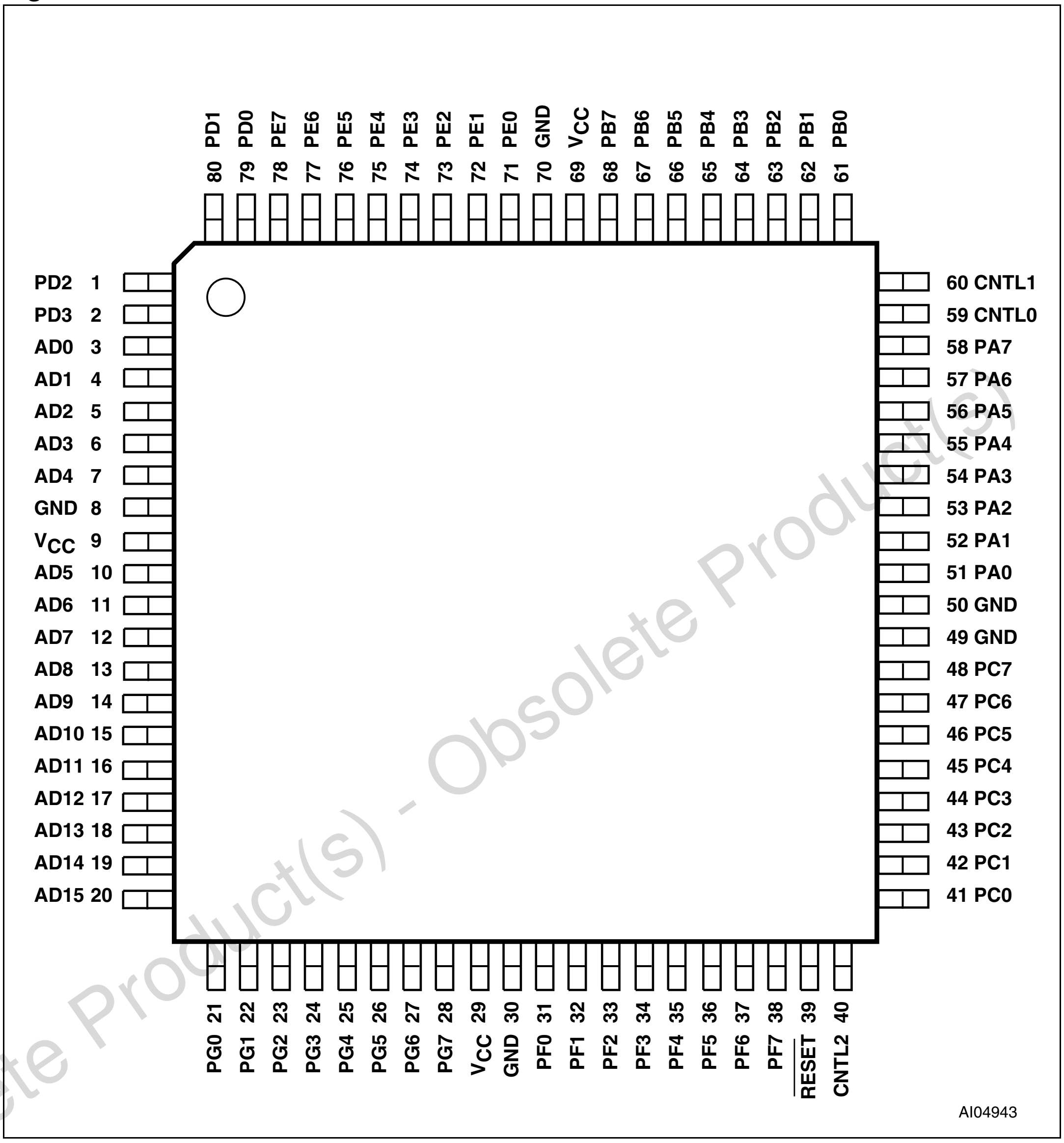


Table 1. Pin description

Pin name	Pin	Type	Description
ADIO0-7	3-7-10-12	I/O	This is the lower Address/Data port. Connect your MCU address or address/data bus according to the following rules: If your MCU has a multiplexed address/data bus where the data is multiplexed with the lower address bits, connect AD0-AD7 to this port. If your MCU does not have a multiplexed address/data bus, connect A0-A7 to this port. If you are using an 80C51XA in burst mode, connect A4/D0 through A11/D7 to this port. ALE or AS latches the address. The PSD drives data out only if the READ signal is active and one of the PSD functional blocks was selected. The addresses on this port are passed to the PLDs.
ADIO8-15	13-20	I/O	This is the upper Address/Data port. Connect your MCU address or address/data bus according to the following rules: If your MCU has a multiplexed address/data bus where the data is multiplexed with the lower address bits, connect A8-A15 to this port. If your MCU does not have a multiplexed address/data bus, connect A8-A15 to this port. If you are using an 80C251 in page mode, connect AD8-AD15 to this port. If you are using an 80C51XA in burst mode, connect A12-A19 to this port. ALE or AS latches the address. The PSD drives data out only if the READ signal is active and one of the PSD functional blocks was selected. The addresses on this port are passed to the PLDs.
CNTL0	59	I	The following control signals can be connected to this port, based on your MCU: $\overline{WR}$ – active low Write Strobe input. R_$\overline{W}$ – active high READ/active low WRITE input. This port is connected to the PLDs. Therefore, these signals can be used in decode and other logic equations.
CNTL1	60	I	The following control signals can be connected to this port, based on your MCU: $\overline{RD}$ – active low Read Strobe input. E – E clock input. $\overline{DS}$ – active low Data Strobe input. $\overline{PSEN}$ – connect $\overline{PSEN}$ to this port when it is being used as an active low READ signal. For example, when the 80C251 outputs more than 16 address bits, $\overline{PSEN}$ is actually the READ signal. This port is connected to the PLDs. Therefore, these signals can be used in decode and other logic equations.
CNTL2	40	I	This port can be used to input the $\overline{PSEN}$ (Program Select Enable) signal from any MCU that uses this signal for code exclusively. If your MCU does not output a Program Select Enable signal, this port can be used as a generic input. This port is connected to the PLDs as input.
Reset	39	I	Active low input. Resets I/O ports, PLD macrocells and some of the Configuration registers and JTAG registers. Must be low at Power-up. Reset also aborts the Flash programming/erase cycle that is in progress.

Table 1. Pin description (continued)

Pin name	Pin	Type	Description
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	58 57 56 55 54 53 52 51	I/O CMOS or Open Drain	These pins make up port A. These port pins are configurable and can have the following functions: MCU I/O – write to or read from a standard output or input port. CPLD macrocell (McellA0-7) outputs. Inputs to the PLDs. Latched, transparent or registered PLD input.
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7	68 67 66 65 64 63 62 61	I/O CMOS or Open Drain	These pins make up port B. These port pins are configurable and can have the following functions: MCU I/O – write to or read from a standard output or input port. CPLD macrocell (McellB0-7) output. Inputs to the PLDs. Latched, transparent or registered PLD input.
PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7	48 47 46 45 44 43 42 41	I/O CMOS or Open Drain	These pins make up port C. These port pins are configurable and can have the following functions: MCU I/O – write to or read from a standard output or input port. External Chip Select (ECS0-7) output. Latched, transparent or registered PLD input.
PD0	79	I/O CMOS or Open Drain	PD0 pin of port D. This port pin can be configured to have the following functions: ALE/AS input latches addresses on ADIO0-ADIO15 pins. AS input latches addresses on ADIO0-ADIO15 pins on the rising edge. Input to the PLDs. Transparent PLD input.
PD1	80	I/O CMOS or Open Drain	PD1 pin of port D. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. Input to the PLDs. CLKIN – clock input to the CPLD macrocells, the APD Unit's Power-down counter, and the CPLD AND Array.
PD2	1	I/O CMOS or Open Drain	PD2 pin of port D. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. Input to the PLDs. PSD Chip Select Input (CSI). When low, the MCU can access the PSD memory and I/O. When high, the PSD memory blocks are disabled to conserve power. The trailing edge of CSI can be used to get the PSD out of power-down mode.

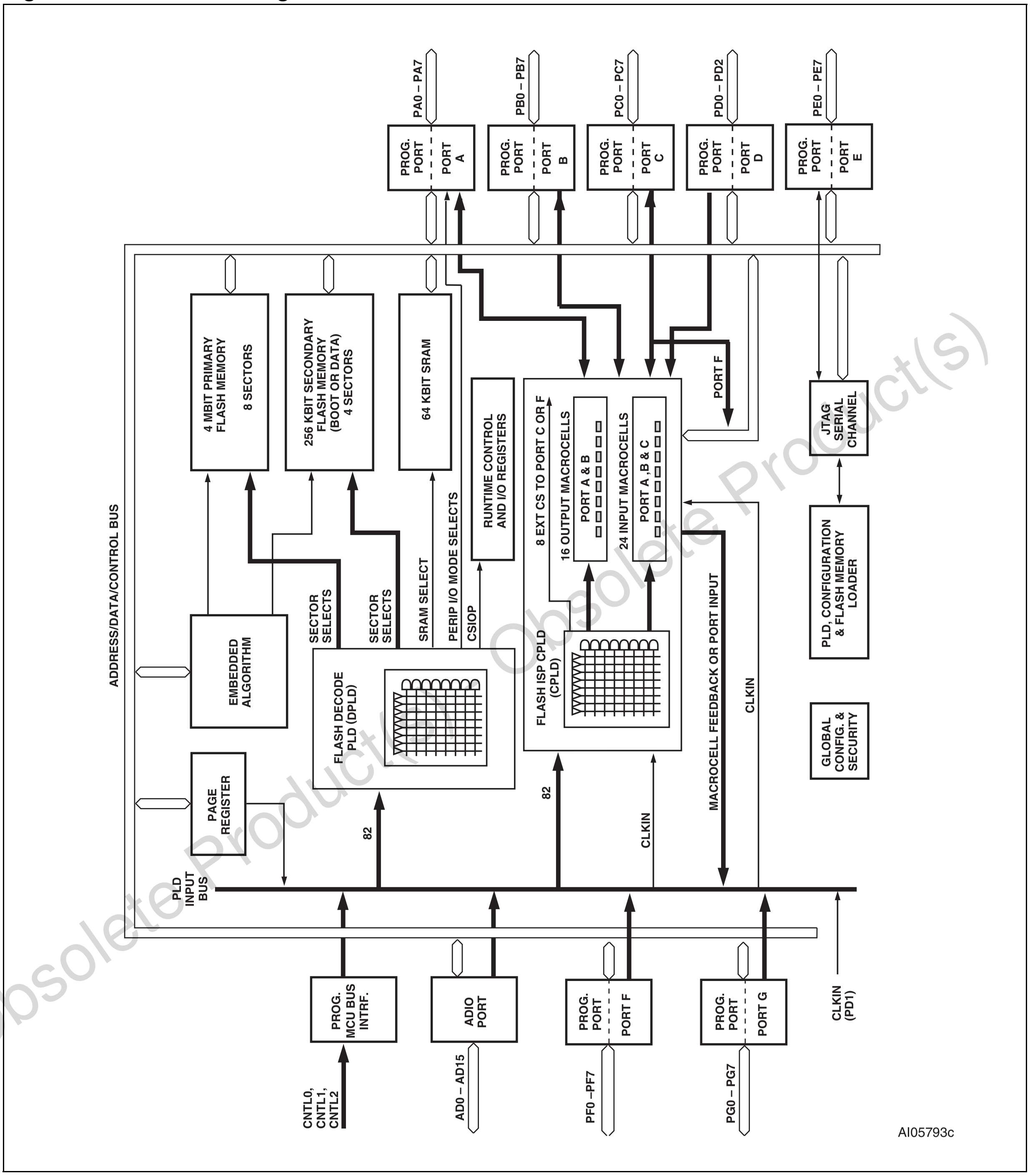
Table 1. Pin description (continued)

Pin name	Pin	Type	Description
PD3	2	I/O CMOS or Open Drain	PD3 pin of port D. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. Input to the PLDs.
PE0	71	I/O CMOS or Open Drain	PE0 pin of port E. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. Latched address output. TMS input for JTAG/ISP interface.
PE1	72	I/O CMOS or Open Drain	PE1 pin of port E. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. Latched address output. TCK input for JTAG/ISP interface (Schmidt Trigger).
PE2	73	I/O CMOS or Open Drain	PE2 pin of port E. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. Latched address output. TDI input for JTAG/ISP interface.
PE3	74	I/O CMOS or Open Drain	PE3 pin of port E. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. Latched address output. TDO input for JTAG/ISP interface.
PE4	75	I/O CMOS or Open Drain	PE4 pin of port E. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. Latched address output. TSTAT input for the ISP interface. Ready/Busy for in-circuit Parallel Programming.
PE5	76	I/O CMOS or Open Drain	PE5 pin of port E. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. Latched address output. TERR active low input for ISP interface.
PE6	77	I/O CMOS or Open Drain	PE6 pin of port E. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. Latched address output.
PE7	78	I/O CMOS or Open Drain	PE7 pin of port E. This port pin can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. Latched address output.
PF0-PF7	31-38	I/O CMOS or Open Drain	PF0 through PF7 pins of port F. This port pins can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. Input to the PLDs. Latched address outputs. As address A0-A3 inputs in 80C51XA mode. As data bus port (D07) in non-multiplexed bus configuration.

Table 1. **Pin description (continued)**

Pin name	Pin	Type	Description
PG0-PG7	8, 30, 49, 50, 70	I/O CMOS or Open Drain	PG0 through PG7 pins of port G. This port pins can be configured to have the following functions: MCU I/O – write to or read from a standard output or input port. Latched address outputs.
V_{CC}	9, 29, 69		Supply voltage
GND	8, 30, 49, 50, 70		Ground pins

Figure 2. PSD block diagram



2 PSD architectural overview

PSD devices contain several major functional blocks. *Figure 2: PSD block diagram* shows the architecture of the PSD device family. The functions of each block are described briefly in the following sections. Many of the blocks perform multiple functions and are user configurable.

2.1 Memory

Each of the memory blocks is briefly discussed in the following paragraphs. A more detailed discussion can be found in the section entitled *Section 6.1: Memory blocks on page 32*. The 4 Mbit (512K x 8) Flash memory is the primary memory of the PSD. It is divided into 8 equally-sized sectors that are individually selectable.

The 256 Kbit (32K x 8) secondary Flash memory is divided into 4 equally-sized sectors. Each sector is individually selectable.

The 64 Kbit SRAM is intended for use as a scratch-pad memory or as an extension to the MCU SRAM.

Each sector of memory can be located in a different address space as defined by the user. The access times for all memory types includes the address latching and DPLD decoding time.

2.2 Page register

The 8-bit Page register expands the address range of the MCU by up to 256 times. The paged address can be used as part of the address space to access external memory and peripherals, or internal memory and I/O. The Page register can also be used to change the address mapping of sectors of the Flash memories into different memory spaces for IAP.

2.3 PLDs

The device contains two PLDs, the Decode PLD (DPLD) and the Complex PLD (CPLD), as shown in *Table 2*, each optimized for a different function. The functional partitioning of the PLDs reduces power consumption, optimizes cost/performance, and eases design entry.

The DPLD is used to decode addresses and to generate Sector Select signals for the PSD internal memory and registers. The CPLD can implement user-defined logic functions. The DPLD has combinatorial outputs. The CPLD has 16 output macrocells (OMC) and 8 combinatorial outputs. The PSD also has 24 input macrocells (IMC) that can be configured as inputs to the PLDs. The PLDs receive their inputs from the PLD Input Bus and are differentiated by their output destinations, number of product terms, and macrocells.

The PLDs consume minimal power by using power-management design techniques. The speed and power consumption of the PLD is controlled by the Turbo bit in PMMR0 and other bits in the PMMR2. These registers are set by the MCU at run-time. There is a slight penalty to PLD propagation time when invoking the power management features.

2.4 I/O ports

The PSD has 52 I/O pins distributed over the seven ports (Port A, B, C, D, E, F and G). Each I/O pin can be individually configured for different functions. ports can be configured as standard MCU I/O ports, PLD I/O, or latched address outputs for MCUs using multiplexed address/data buses.

The JTAG pins can be enabled on port E for in-system programming (ISP). ports F and G can also be configured as data ports for a non-multiplexed bus.

Ports A and B can also be configured as a data port for a non-multiplexed bus.

2.5 MCU bus interface

PSD interfaces easily with most 8-bit MCUs that have either multiplexed or non-multiplexed address/data buses. The device is configured to respond to the MCU's control signals, which are also used as inputs to the PLDs. For examples, please see .

Table 2. PLD I/O

Name	Inputs	Outputs	Product terms
Decode PLD (DPLD)	82	17	43
Complex PLD (CPLD)	82	24	150

Table 3. JTAG signals on port E

Port E pins	JTAG signal
PE0	TMS
PE1	TCK
PE2	TDI
PE3	TDO
PE4	TSTAT
PE5	TERR

2.6 JTAG port

In-system programming (ISP) can be performed through the JTAG signals on port E. This serial interface allows complete programming of the entire PSD device. A blank device can be completely programmed. The JTAG signals (TMS, TCK, TSTAT, $\overline{\text{TERR}}$, TDI, TDO) can be multiplexed with other functions on port E. *Table 3: JTAG signals on port E* indicates the JTAG pin assignments.

2.7 In-system programming (ISP)

Using the JTAG signals on port E, the entire PSD device (memory, logic, configuration) can be programmed or erased without the use of the MCU.

2.8 In-application reprogramming (IAP)

The primary Flash memory can also be programmed in-system by the MCU executing the programming algorithms out of the secondary memory, or SRAM. Since this is a sizable separate block, the application can also continue to operate. The secondary memory can be programmed the same way by executing out of the primary Flash memory. The PLD or other PSD Configuration blocks can be programmed through the JTAG port or a device programmer. *Table 4* indicates which programming methods can program different functional blocks of the PSD.

2.9 Power management unit (PMU)

The power management unit (PMU) gives the user control of the power consumption on selected functional blocks based on system requirements. The PMU includes an Automatic Power-down (APD) Unit that turns off device functions during MCU inactivity. The APD Unit has a Power-down mode that helps reduce power consumption.

The PSD also has some bits that are configured at run-time by the MCU to reduce power consumption of the CPLD. The Turbo bit in PMMR0 can be reset to '0' and the CPLD latches its outputs and goes to sleep until the next transition on its inputs.

Additionally, bits in PMMR2 can be set by the MCU to block signals from entering the CPLD to reduce power consumption. Please see *Section 18: Power management on page 88* for more details.

Table 4. Methods for programming different functional blocks of the PSD

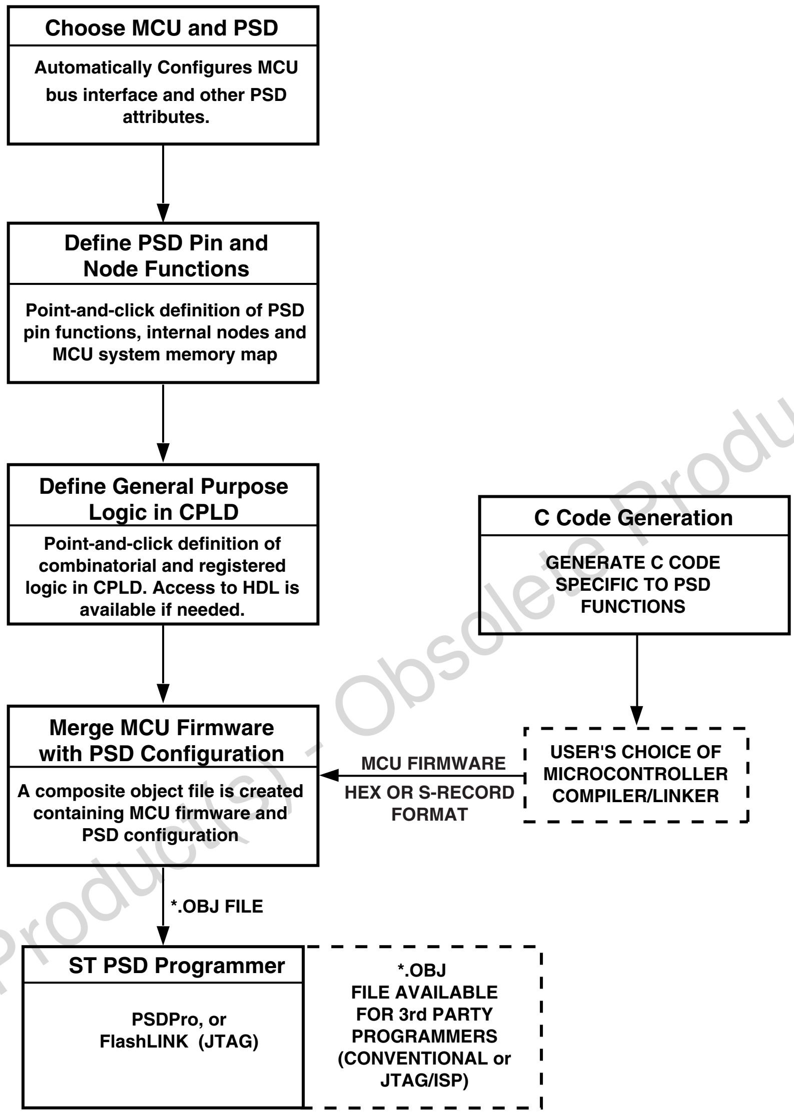
Functional block	JTAG/ISP	Device programmer	IAP
Primary Flash memory	Yes	Yes	Yes
Secondary Flash memory	Yes	Yes	Yes
PLD Array (DPLD and CPLD)	Yes	Yes	No
PSD configuration	Yes	Yes	No

3 Development system

The PSD family is supported by PSDsoft, a Windows-based (95, 98, NT) software development tool. A PSD design is quickly and easily produced in a point-and-click environment. The designer does not need to enter Hardware Description Language (HDL) equations, unless desired, to define PSD pin functions and memory map information. The general design flow is shown in *Figure 3*. PSDsoft is available from our web site (the address is given on the back page of this data sheet) or other distribution channels.

PSDsoft directly supports two low cost device programmers form ST: PSDpro and FlashLINK (JTAG). Both of these programmers may be purchased through your local distributor/representative, or directly from our web site using a credit card. The PSD is also supported by third party device programmers. See our web site for the current list.

Figure 3. PSDsoft development tool



4 PSD register description and address offset

Table 5 shows the offset addresses to the PSD registers relative to the CSIOP base address. The CSIOP space is the 256 bytes of address that is allocated by the user to the internal PSD registers. *Table 5* provides brief descriptions of the registers in CSIOP space. The following section gives a more detailed description.

Table 5. Register address offset

Register name	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Other (1)	Description
Data In	00	01	10	11	30	40	41		Reads port pin as input, MCU I/O input mode
Control					32	42	43		Selects mode between MCU I/O or Address Out
Data Out	04	05	14	15	34	44	45		Stores data for output to port pins, MCU I/O output mode
Direction	06	07	14	15	36	46	47		Configures port pin as input or output
Drive Select	08	09	18	19	38	48	49		Configures port pins as either CMOS or Open Drain on some pins, while selecting high slew rate on other pins.
Input macrocell	0A	0B		1A					Reads input macrocells
Enable Out	0C	0D	1C	1B		4C			Reads the status of the output enable to the I/O port driver
Output macrocells A	20								READ – reads output of macrocells A WRITE – loads macrocell flip-flops
Output macrocells B		21							READ – reads output of macrocells B WRITE – loads macrocell flip-flops
Mask macrocells A	22								Blocks writing to the output macrocells A
Mask macrocells B		23							Blocks writing to the output macrocells B
Primary Flash Protection								C0	Read only – Primary Flash Sector Protection
Secondary Flash Memory Protection								C2	Read only – PSD Security and secondary Flash memory Sector Protection
JTAG Enable								C7	Enables JTAG port
PMMR0								B0	Power Management register 0
PMMR2								B4	Power Management register 2

Table 5. Register address offset (continued)

Register name	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Other (1)	Description
Page								E0	Page register
VM								E2	Places PSD memory areas in Program and/or Data space on an individual basis.
Memory_ID0								F0	Read only – Primary Flash memory and SRAM size
Memory_ID1								F1	Read only – secondary Flash memory type and size

1. Other registers that are not part of the I/O ports.